High-Bandwidth, Low Voltage, Dual SPDT Analog Switches

DESCRIPTION

The DG2519E is monolithic CMOS dual single-pole / double-throw (SPDT) analog switches. It is specifically designed for low-voltage, high bandwidth applications.

The DG2519E on-resistance, matching and flatness are guaranteed over the entire analog voltage range. Wide dynamic performance is achieved with typical at -61 dB for both cross-talk and off-isolation at 1 MHz.

Both SPDT's operate with independent control logic, conduct equally well in both directions and block signals up to the power supply level when off. Break-before-make is guaranteed.

With fast switching speeds, low on-resistance, high bandwidth, and low charge injection, the DG2519E are ideally suited for audio and video switching with high linearity.

Built on Vishay Siliconix's low voltage CMOS technology, the DG2519E contain an epitaxial layer which prevents latch-up

FEATURES

- Single supply (1.8 V to 5.5 V)
- Low on-resistance - R_{ON}: 2.5 Ω
- Crosstalk and off isolation: -61 dB at 1 MHz
- MSOP-10 and DFN-10 package
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

HALOGEN FREE

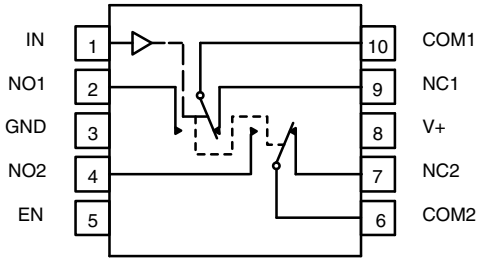
BENEFITS

- Reduced power consumption
- High accuracy
- Reduce board space
- Low-voltage logic compatible
- High bandwidth

APPLICATIONS

- Cellular phones
- Speaker headset switching
- Audio and video signal routing
- PCMCIA cards
- Low-voltage data acquisition
- ATE

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Top view

TRUTH TABLE

LOGIC	EN	NC1 and NC2	NO1 and NO2
0	1	ON	OFF
1	1	OFF	ON
0	0	OFF	OFF
1	0	OFF	OFF

ORDERING INFORMATION

TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	MSOP-10	DG2519EDQ-T1-GE3
	DFN-10	DG2519EDN-T1-GE4

ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
Reference V+ to GND		-0.3 to +6	V
IN, COM, NC, NO [a]		-0.3 to (V+ + 0.3)	
Continuous current (any terminal)		± 50	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage temperature (D suffix)		-65 to +150	°C
Power dissipation (packages) [b]	MSOP-10 [c]	320	mW
	DFN-10 [d]	1191	
ESD / HBM	EIA / JESD22-A114-A	7.5k	V
ESD / CDM	EIA / JESD22-C101-A	1.5k	
Latch up	JESD78	300	mA

Notes

a. Signals on NC, NO, COM, IN, or EN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 4 mW/°C above 70 °C
d. Derate 14.9 mW/°C above 70 °C

SPECIFICATIONS (V+ = 3 V)

PARAMETER	SYMBOL	TEST CONDITIONS OTHERWISE UNLESS SPECIFIED V+ = 3 V, ± 10 %, $V_{IN/ENL}$ = 0.4 V, $V_{IN/ENH}$ = 1.5 V [e]	TEMP. [a]	LIMITS -40 °C to +85 °C MIN. [c]	TYP. [b]	MAX. [c]	UNIT
Analog Switch							
Analog signal range [d]	V_{ANALOG}		Full	0	-	V+	V
Drain-source on-resistance	$R_{DS(on)}$	V+ = 1.8 V, $V_{NC/NO}$ = 0.4 V / V+, $I_{NC/NO}$ = 8 mA	Room	-	7	11	Ω
			Full	-	-	13	
		V+ = 2.7 V, V_{COM} = 0.8 V / 1.8 V, I_{COM} = 10 mA	Room	-	4.6	5.5	
			Full	-	-	6.5	
On-resistance matching	$\Delta R_{DS(on)}$	V+ = 2.7 V, V_{COM} = 0.8 V / 1.4 V / 1.8 V, I_{COM} = 10 mA	Room	-	0.02	0.3	
			Full	-	-	0.6	
On-resistance flatness [d, f]	$R_{flat(on)}$		Room	-	0.62	1.1	
			Full	-	-	1.5	
Off leakage current [g]	$I_{NC/NO(off)}$	V+ = 3.6 V, $V_{NC/NO}$ = 1 V / 3.2 V, V_{COM} = 3.2 V / 1 V, V_{EN} = 0 V	Room	-1	0.01	1	nA
			Full	-5	-	5	
COM off leakage current [g]	$I_{COM(off)}$		Room	-1	0.01	1	
			Full	-5	-	5	
Channel-on leakage current [g]	$I_{COM(on)}$	V+ = 3.3 V, V_{COM} = $V_{NC/NO}$ = 1 V / 3.2 V	Room	-1	0.01	1	
			Full	-5	-	5	
Digital Control							
Input current [d]	I_{INL} or I_{INH}		Full	-1	-	1	µA
Input high voltage [d]	V_{INH}		Full	1.5	-	-	V
Input low voltage [d]	V_{INL}		Full	-	-	0.4	
Digital input capacitance [d]	C_{IN}		Room	-	3	-	pF
Dynamic Characteristics							
Turn-on time	t_{ON}	$V_{NC/NO}$ = 3 V, C_L = 35 pf, R_L = 300 Ω	Room	-	21	45	ns
			Full	-	-	50	
Turn-off time	t_{OFF}		Room	-	11	35	
			Full	-	-	45	
Break-before-make time [d]	t_{BBM}		Room	3	13	-	
			Full	2	-	-	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{gen}= 1.5 V, R_{gen}= 0 Ω	Room	-	-10.2	-	pC
Bandwidth [d]	BW	C_L = 5 pF (set up capacitance)	Room	-	222	-	MHz
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-58	-	dB
		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room	-	-47	-	
Channel-to-channel crosstalk [d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-57	-	
		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room	-	-47	-	
NO, NC Off capacitance [d]	$C_{NO(off)}$	V+ = 2.7 V, f = 1 MHz	Room	-	7	-	pF
	$C_{NC(off)}$		Room	-	7	-	
Channel-on capacitance [d]	$C_{NO(on)}$		Room	-	24	-	
	$C_{NC(on)}$		Room	-	24	-	
Power Supply							
Power supply range	V+			2.7	-	3.3	V
Power supply current [d]	I+	V+ = 2.7 V, V_{IN} = 0 V or 2.7 V	Full	-	-	1	µA

Notes

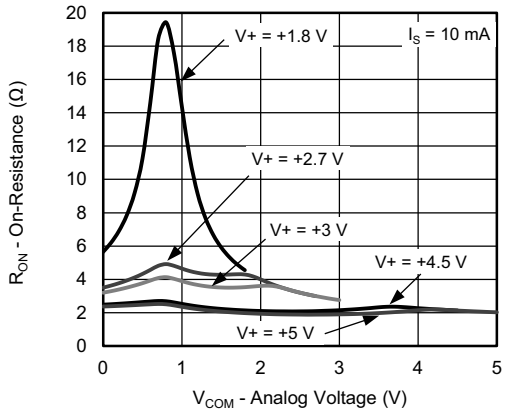
a. Room = 25 °C, Full = as determined by the operating suffix
b. Typical values are for design aid only, not guaranteed nor subject to production testing
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
d. Guarantee by design, not subjected to production test
e. V_{IN} = V+ voltage to perform proper function
f. Crosstalk measured between channels
g. Guarantee by 5 V testing

SPECIFICATIONS (V+ = 5 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS OTHERWISE UNLESS SPECIFIED V+ = 5 V, ± 10 %, $V_{IN/ENL}$ = 0.5 V, $V_{IN/ENH}$ = 2 V [e]**	**TEMP. [a]**	**LIMITS -40 °C to +85 °C**			**UNIT**
				MIN. [c]	**TYP. [b]**	**MAX. [c]**	
Analog Switch							
Analog signal ranged	V_{ANALOG}		Full	0	-	V+	V
Drain-source on-resistance	$R_{DS(on)}$	V+ = 4.5 V, V_{COM} = 0.8 V / 3.5 V; I_{COM} = 10 mA	Room	-	2.5	3.1	Ω
			Full	-	-	4	
On-resistance matching	$\Delta R_{DS(on)}$	V+ = 4.5 V, V_{COM} = 0.8 V / 2.5 V / 3.5 V, I_{COM} = 10 mA	Room	-	0.01	0.4	
			Full	-	-	0.5	
On-resistance flatness [d, f]	$R_{flat(on)}$		Room	-	0.61	1	
			Full	-	-	1.5	
Off leakage current [g]	$I_{NC/NO(off)}$	V+ = 5.5 V, $V_{NC/NO}$ = 1 V / 4.5 V, V_{COM} = 4.5 V / 1 V, V_{EN} = 0 V	Room	-2	0.16	2	nA
			Full	-10	-	10	
COM off leakage current [g]	$I_{COM(off)}$		Room	-2	0.20	2	
			Full	-10	-	10	
Channel-on leakage current [g]	$I_{COM(on)}$	V+ = 5.5 V, V_{COM} = $V_{NC/NO}$ = 1 V / 4.5 V	Room	-2	0.20	2	
			Full	-10	-	10	
Power down leakage [d]	I_{PD}	V+ = 0 V, V_{COM} = 5.5 V, NC/NO open	Full	-	0.01	5	µA
		V+ = 0 V, $V_{NC/NO}$ = 5.5 V, COM, open	Full	-	0.01	3	mA
Digital Control							
Input current [d]	I_{INL} or I_{INH}		Full	-1	-	1	µA
Input high voltage [d]	V_{INH}		Full	2	-	-	V
Input low voltage [d]	V_{INL}		Full	-	-	0.5	
Digital input capacitance [d]	C_{IN}		Room	-	3	-	pF
Dynamic Characteristics							
Turn-on time	t_{ON}	$V_{NC/NO}$ = 3 V, C_L = 35 pf, R_L = 300 Ω	Room	-	14	40	ns
			Full	-	-	43	
Turn-off time	t_{OFF}		Room	-	7	33	
			Full	-	-	35	
Break-before-make time [d]	t_{BBM}		Room	3	8	-	
			Full	2	-	-	
Propagation delay [d]	tpd	V+ = 5 V, no R_L	Room	-	325	-	ps
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{gen} = 2.5 V, R_{gen} = 0 Ω	Room	-	-14	-	pC
Bandwidth [d]	BW	C_L = 5 pF (set up capacitance)	Room	-	217	-	MHz
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-61	-	dB
		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room	-	-48	-	
Channel-to-channel crosstalk [d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-61	-	
		R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room	-	-48	-	
NO, NC Off capacitance [d]	$C_{NO(off)}$	V+ = 5 V, f = 1 MHz	Room	-	7	-	pF
	$C_{NC(off)}$		Room	-	7	-	
Channel-On capacitance [d]	$C_{NO(on)}$		Room	-	24	-	
	$C_{NC(on)}$		Room	-	24	-	
Power Supply							
Power supply range	V+			4.5	-	5.5	V
Power supply current [d]	I+	V+ = 5.5 V, V_{IN} = 0 V or 5.5 V	Full	-	-	1	µA

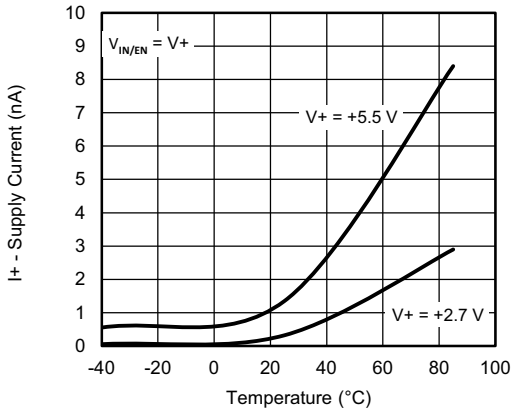
Notes
a. Room = 25 °C, Full = as determined by the operating suffix
b. Typical values are for design aid only, not guaranteed nor subject to production testing
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
d. Guarantee by design, not subjected to production test
e. V_{IN} = input voltage to perform proper function
f. Difference of min and max values
g. Guaranteed by 5 V testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

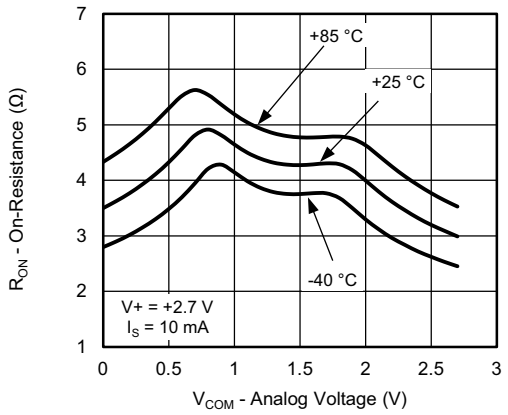
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



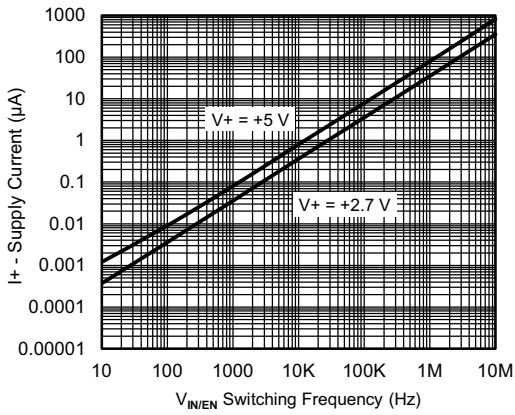
R_{ON} vs. V_{COM} and Single Supply Voltage



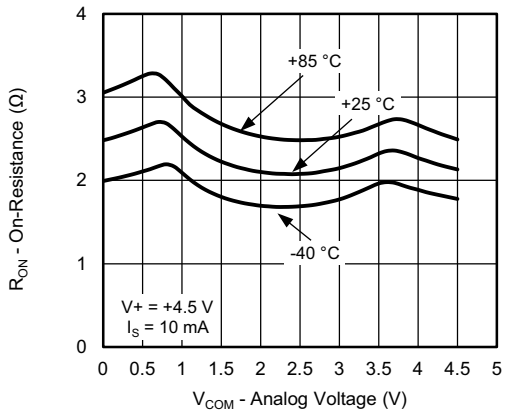
Supply Current vs. Temperature



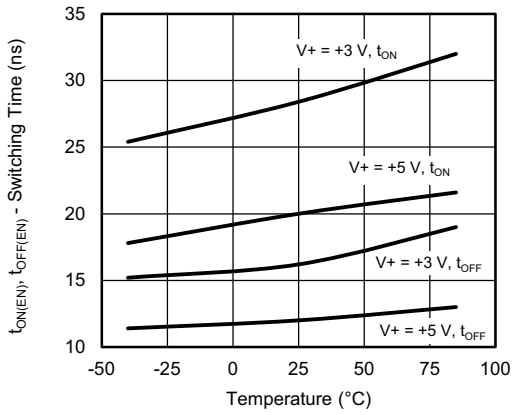
R_{ON} vs. Analog Voltage and Temperature



Positive Supply Current vs. Switching Frequency

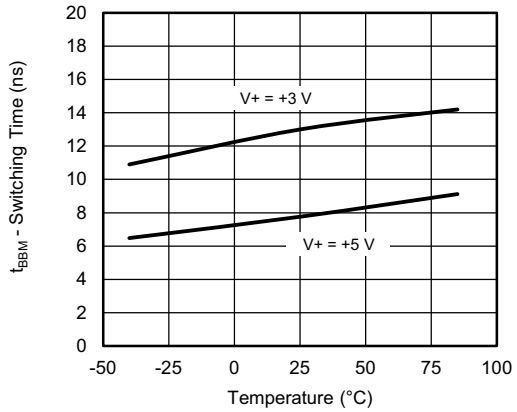


R_{ON} vs. Analog Voltage and Temperature

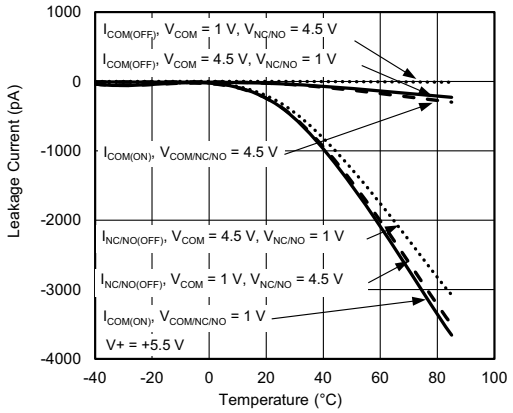


Switching Time vs. Temperature

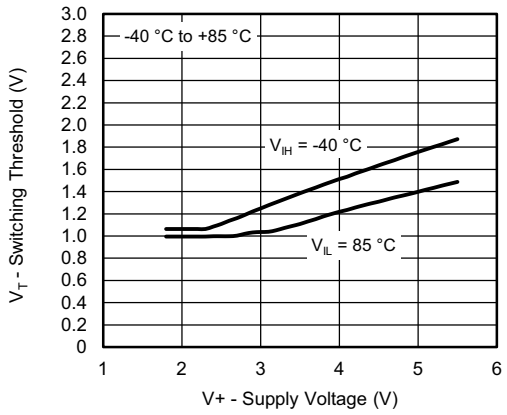
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



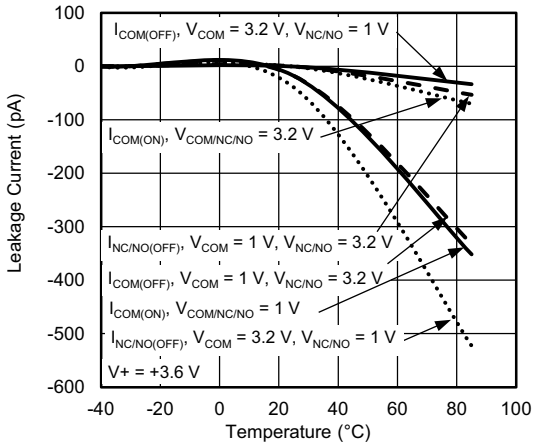
Switching Time vs. Temperature



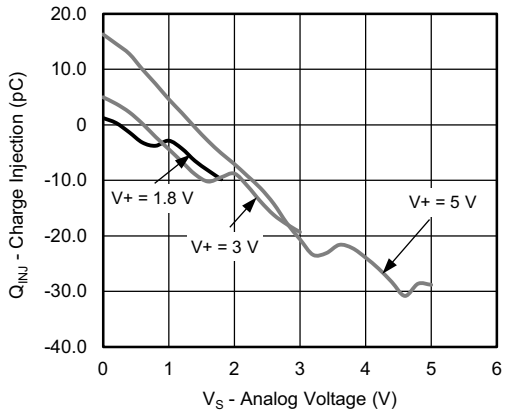
Leakage Current vs. Temperature



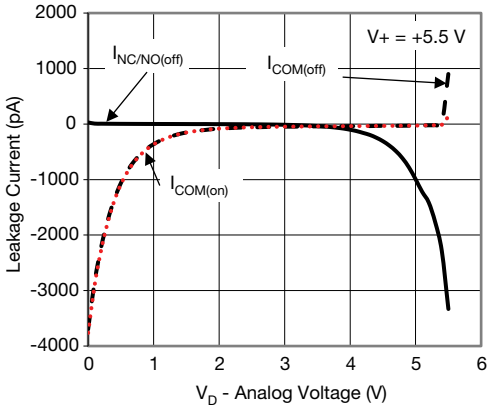
Switching Threshold vs. Supply Voltage



Leakage Current vs. Temperature

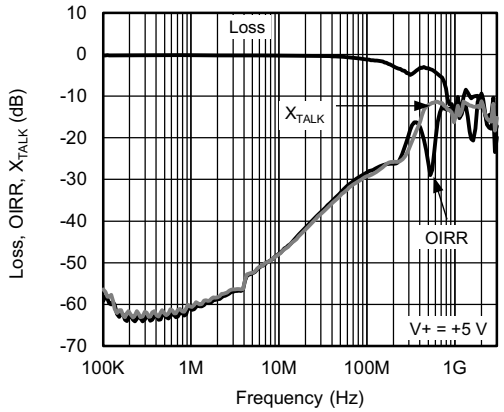


Charge Injection vs. Source Voltage

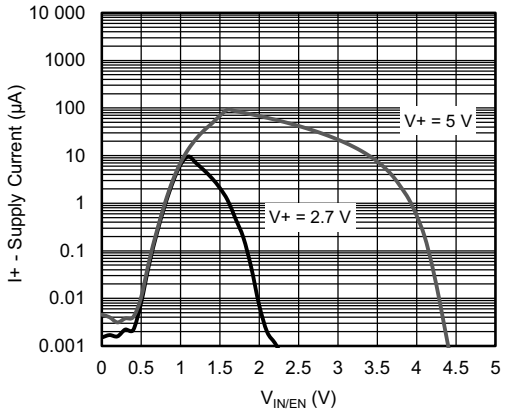


Leakage Current vs. Analog Voltage

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

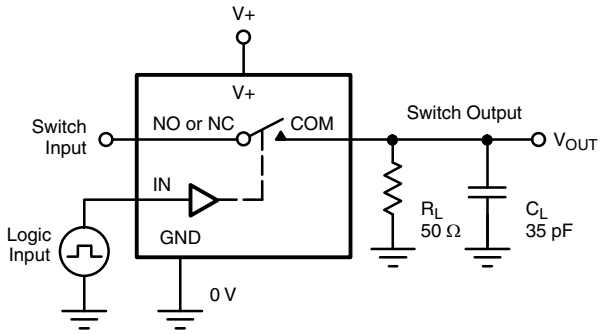


Loss, OIRR, X_{TALK} vs. Frequency



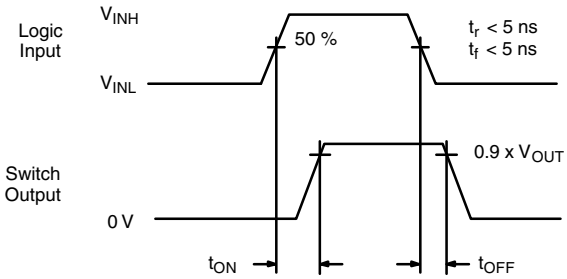
Positive Supply Current vs. Logic Voltage

TEST CIRCUITS



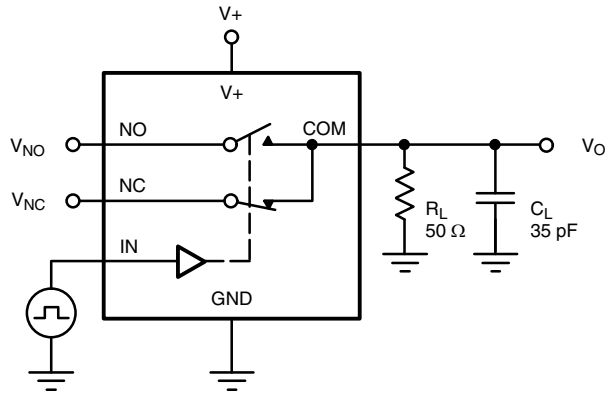
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Fig. 1 - Switching Time



C_L (includes fixture and stray capacitance)

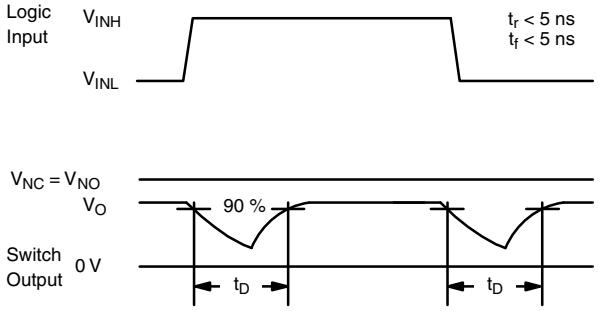
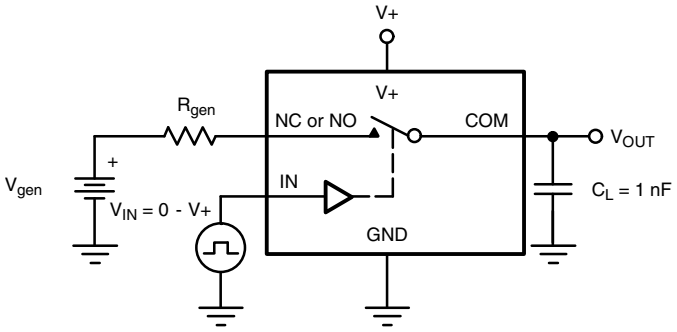
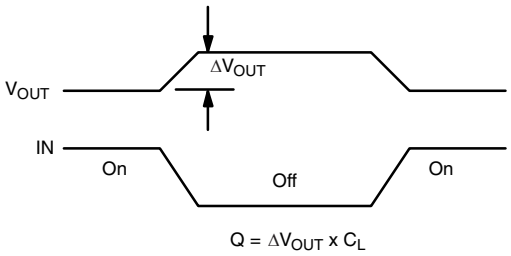


Fig. 2 - Break-Before-Make Interval

TEST CIRCUITS





IN depends on switch configuration: input polarity determined by sense of switch.

Fig. 3 - Charge Injection

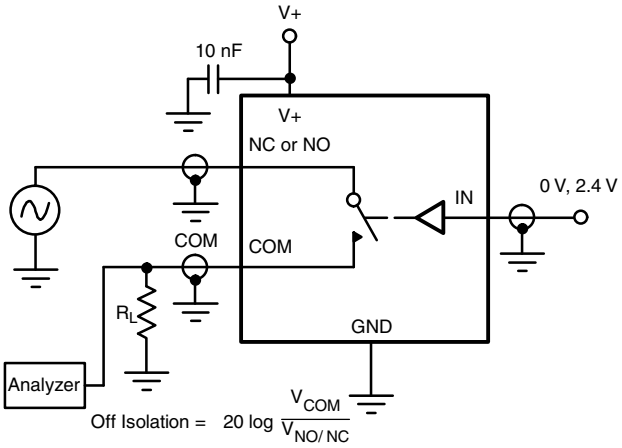


Fig. 4 - Off-Isolation

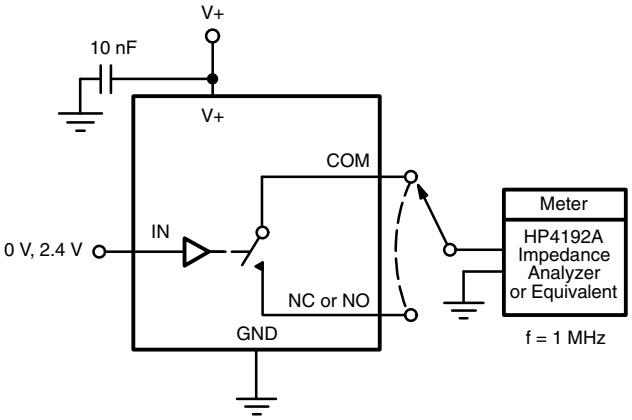


Fig. 5 - Channel Off/On Capacitance

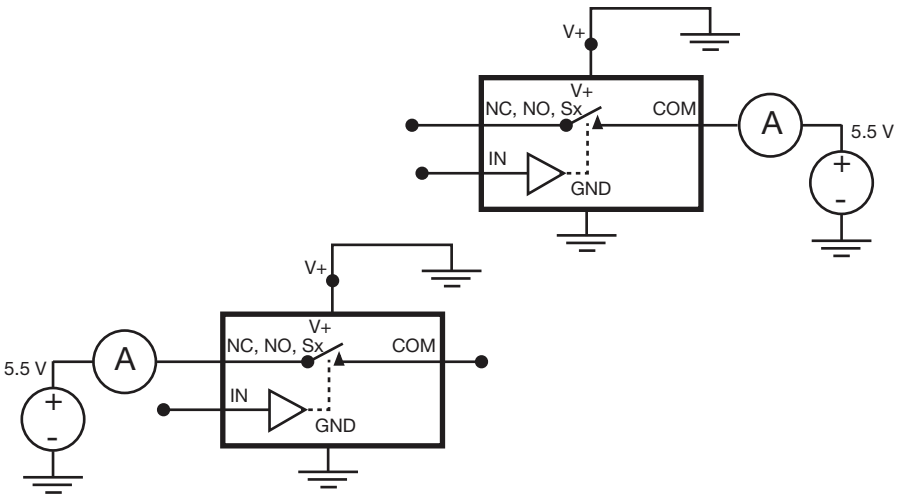
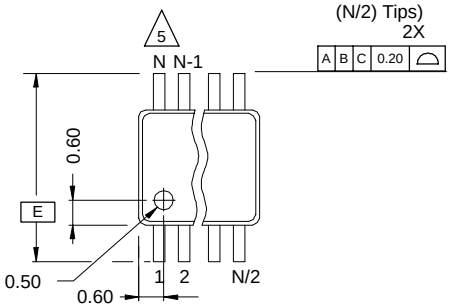


Fig. 6 - Source / Drain Power Down Leakage

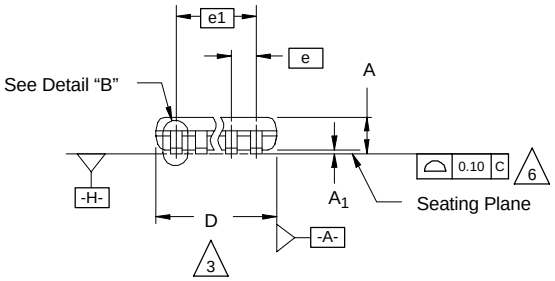
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?78595.

MSOP: 10-LEADS

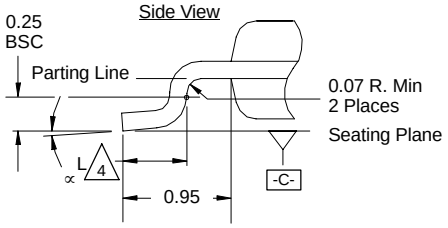
JEDEC Part Number: MO-187, (Variation AA and BA)



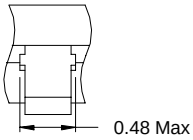
Top View



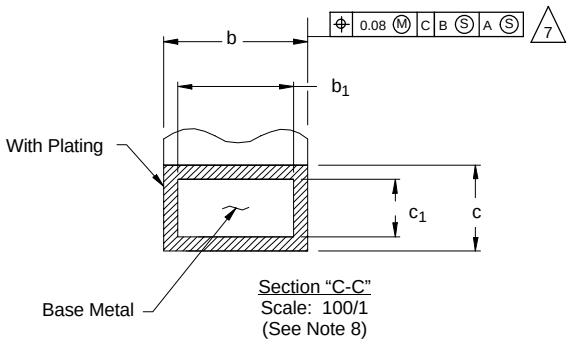
Side View



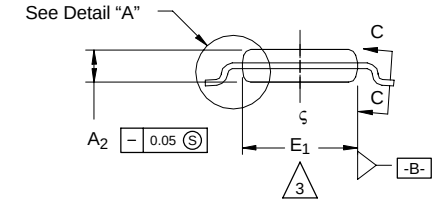
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

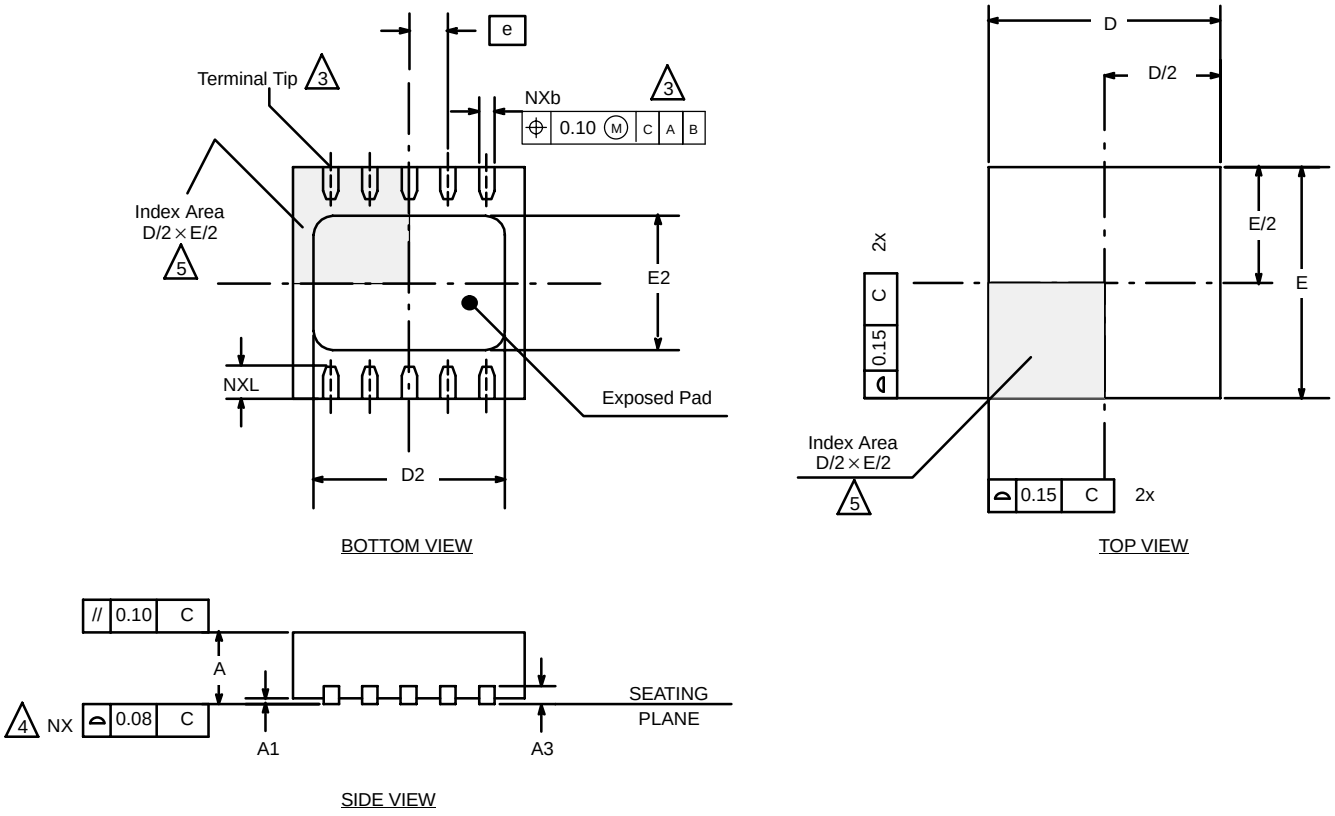
1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 10L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.17	-	0.27	8
b_1	0.17	0.20	0.23	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.50 BSC			
e_1	2.00 BSC			
L	0.40	0.55	0.70	4
N	10			5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

DFN-10 LEAD (3 X 3)



NOTES:

1. All dimensions are in millimeters and inches.
2. N is the total number of terminals.
3. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30 mm from terminal tip.
4. Coplanarity applies to the exposed heat sink slug as well as the terminal.
5. The pin #1 identifier may be either a mold or marked feature, it must be located within the zone iindicated.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.90	1.00	0.031	0.035	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 BSC			0.008 BSC	
b	0.18	0.23	0.30	0.007	0.009	0.012
D		3.00 BSC			0.118 BSC	
D2	2.20	2.38	2.48	0.087	0.094	0.098
E		3.00 BSC			0.118 BSC	
E2	1.49	1.64	1.74	0.059	0.065	0.069
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

*Use millimeters as the primary measurement.

ECN: S-42134—Rev. A, 29-Nov-04
DWG: 5943

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