# 700 MHz, -3 dB Bandwidth; Dual SPDT Analog Switch

## DESCRIPTION

DG2723 is a low $R_{ON}$, high bandwidth analog switch configured in dual SPDT. It achieves 5.5 Ω switch on resistance, greater than 700 MHz -3 dB bandwidth with 5 pF load, and a channel to channel crosstalk at -36 dB and isolation at -29 dB. Fabricated with high density sub micro CMOS process, the DG2723 provides low parasitic capacitance, handles bidirectional signal flow with minimized phase distortion. Guaranteed 1.3 V logic high threshold makes it possible to interface directly with low voltage MCUs. The DG2723 is designed for a wide range of operating voltages from 2.7 V to 5.5 V that can be driven directly from one cell Li-ion battery. On-chip protection circuit protects again fault events when signals at “com” pins goes beyond V+.

Latch up current is 500 mA, as per JESD78, and its ESD tolerance exceeds 5 kV. Packaged in ultra small miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm), it is ideal for portable high speed mix signal switching application.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device termination. The miniQFN-10 package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free “-E4” suffix to the ordering part number. The nickel-palladium-gold device terminations meet all JEDEC® standards for reflow and MSL rating. As a further sign of Vishay Siliconix's commitment, the DG2723 is fully RoHS complaint.

## FEATURES

Pb-free

RoHS COMPLIANT

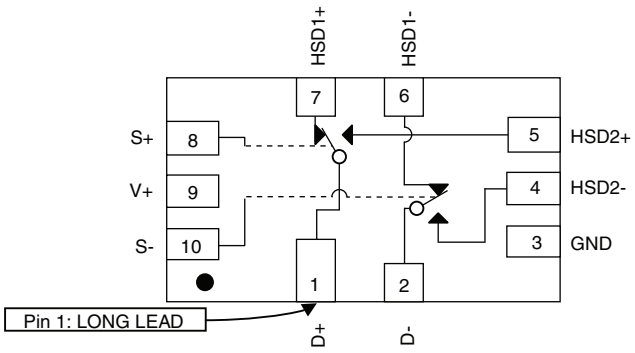
- Wide operation voltage range
- Low on-resistance, 5.5 Ω (typical at 3 V)
- Low capacitance, 5.6 pF (typical)
- -3 dB high bandwidth with 5pF load: 700 MHz (typical)
- Low bit to bit skew: 40 pS (typical)
- Low power consumption
- Low logic threshold: V
- Power down protection: D+/D- pins can tolerate up to 5.5 V when V+ = 0 V
- Logic (S+ and S-) above V+ tolerance
- 5 kV ESD protection (HBM)
- Latch-up current 500 mA per JESD78
- Lead (Pb)-free low profile miniQFN-10 (1.4 mm x 1.8 mm x 0.55 mm)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

## APPLICATIONS

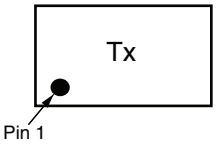
- Cellular phones
- Portable media players
- PDA
- Digital camera
- GPS
- Notebook computer
- TV, monitor, and set top box

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

**miniQFN-10L**




Top View




Device marking: Tx for DG2723
x = Date/Lot traceability code

## ORDERING INFORMATION

| TEMP. RANGE | PACKAGE | PART NUMBER |
|---|---|---|
| -40 °C to 85 °C | miniQFN-10 | DG2723DN-T1-E4 |

## TRUTH TABLE

| S+ (PIN 8) | S- (PIN 10) | FUNCTION |
|---|---|---|
| X | 0 | D- = HSD1- |
| X | 1 | D- = HSD2- |
| 0 | X | D+ = HSD1+ |
| 1 | X | D+ = HSD2+ |

## PIN DESCRIPTIONS

| PIN NAME | DESCRIPTION |
|---|---|
| S+ | Select Input for D+ |
| S- | Select Input for D- |
| HSD±, HSD2±, D± | Data Port |

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25 °C, unless otherwise noted)

| PARAMETER | | LIMIT | UNIT |
|---|---|---|---|
| Reference to GND | V+ | -0.3 to 6 | V |
| | S+, S-, D±, HSD1±, HSD2± [a] | -0.3 to (V+ + 0.3) | |
| Current (Any Terminal except S+, S-, D±, HSD1±, HSD2±) | | 30 | mA |
| Continuous Current (S+, S-, D±, HSD1±, HSD2±) | | ± 250 | |
| Peak Current (Pulsed at 1 ms, 10 % Duty Cycle) | | ± 500 | |
| Storage Temperature (D Suffix) | | -65 to 150 | °C |
| Power Dissipation (Packages) [b] | miniQFN-10 [c] | 208 | mW |
| ESD (Human Body Model) | | 5 | kV |
| Latch-up (Current Injection) | | 500 | mA |

**Notes**

a. Signals on S+, S-, D±, HSD1±, HSD2± exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 2.6 mW/°C above 70 °C.

## SPECIFICATIONS (V+ = 3 V)

| PARAMETER | SYMBOL | TEST CONDITIONS OTHERWISE UNLESS SPECIFIED | TEMP.[a] | LIMITS -40 °C to 85 °C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN. [b] | TYP. [c] | MAX. [b] | |
| **Analog Switch** | | | | | | | |
| Analog Signal Range [d] | $V_{ANALOG}$ | $R_{DS(on)}$ | Full | 0 | - | V+ | V |
| On-Resistance | $R_{DS(on)}$ | V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0.4 V | Room | - | 5.5 | 8 | Ω |
| | | | Full | - | - | 9 | |
| On-Resistance Match [d] | $\Delta R_{ON}$ | V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0.4 V | Room | - | 0.8 | - | |
| On-Resistance Resistance Flatness [d] | $R_{ON}$ Flatness | V+ = 3 V, $I_{D±}$ = 8 mA, $V_{HSD1/2±}$ = 0 V, 1 V | Room | - | 2 | - | |
| Switch Off Leakage Current | $I_{(off)}$ | V+ = 4.3 V, $V_{HSD1/2±}$ = 0.3 V, 3 V, $V_{D±}$ = 3 V, 0.3 V | Full | -100 | - | 100 | nA |
| Channel On Leakage Current | $I_{(on)}$ | V+ = 4.3 V, $V_{HSD1/2±}$ = 0.3 V, 4 V, $V_{D±}$ = 4 V, 0.3 V | Full | -200 | - | 200 | |
| **Digital Control** | | | | | | | |
| Input Voltage High | $V_{INH}$ | V+ = 3 V to 3.6 V | Full | 1.3 | - | - | V |
| | | V+ = 4.3 V | Full | 1.5 | - | - | |
| Input Voltage Low | $V_{INL}$ | V+ = 3 V to 4.3 V | Full | - | - | 0.5 | |
| Input Capacitance | $C_{IN}$ | | Full | - | 6.5 | - | pF |
| Input Current | $I_{INL}$ or $I_{INH}$ | $V_{IN}$ = 0 or V+ | Full | -1 | - | 1 | µA |

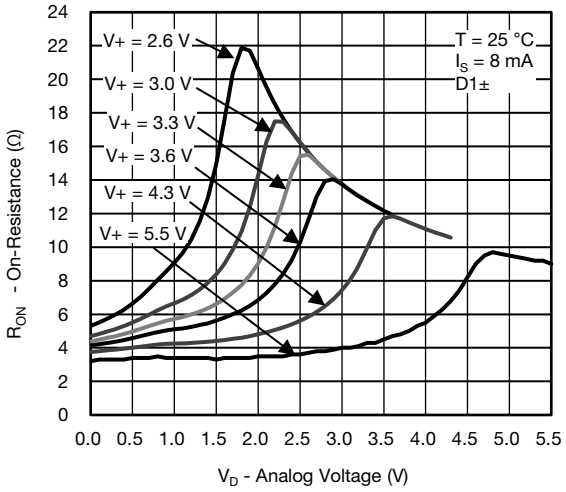
| **SPECIFICATIONS** (V+ = 3 V) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS OTHERWISE UNLESS SPECIFIED** | **TEMP.[a]** | **LIMITS -40 °C to 85 °C** | | | **UNIT** |
| | | | | **MIN. [b]** | **TYP. [c]** | **MAX. [b]** | |
| **Dynamic Characteristics** | | | | | | | |
| Break-Before-Make Time [e, d] | $t_{BBM}$ | V+ = 3 V, $V_{D1/2±}$ = 1.5 V, $R_L$ = 50 Ω, $C_L$ = 35 pF | Room | - | 5 | - | ns |
| | | | Full | | | | |
| S-, S+ Turn-On Time [e, d] | $t_{ON}$ | | Room | - | - | 30 | |
| | | | Full | | | | |
| S-, S+ Turn-Off Time [e, d] | $t_{OFF}$ | | Room | - | - | 25 | |
| | | | Full | | | | |
| Charge Injection [d] | $Q_{INJ}$ | $C_L$ = 1 nF, $R_{GEN}$ = 0 Ω, $V_{GEN}$ = 0 V | Room | - | 3 | - | pC |
| Off-Isolation [d] | OIRR | V+ = 3 V to 3.6 V, $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 240 MHz | | - | -29 | - | dB |
| Crosstalk [d] | $X_{TALK}$ | | | - | -36 | - | |
| Bandwidth [d] | BW | V+ = 3 V to 3.6 V, $C_L$ = 5 pF, $R_L$ = 50 Ω, -3 dB | | - | 700 | - | MHz |
| Channel-Off Capacitance [d] | $C_{D1± (off)}$ | V+ = 3.3 V, f = 1 MHz | | - | 2.5 | - | pF |
| | $C_{D2± (off)}$ | | | - | 2.5 | - | |
| Channel-On Capacitance [d] | $C_{D± (off)}$ | | | - | 2.5 | - | |
| | $C_{D± (on)}$ | | | - | 6.5 | - | |
| Channel-to-Channel Skew [d] | $t_{SK(O)}$ | V+ = 3 V to 3.6 V, $R_L$ = 50 Ω, $C_L$ = 5 pF | | - | 50 | - | ps |
| Skew Off Opposite Transitions of the Same Output [d] | $t_{SK(p)}$ | | | - | 20 | - | |
| Total Jitter [d] | $t_J$ | | | - | 200 | - | |
| **Power Supply** | | | | | | | |
| Power Supply Range | V+ | | | 2.6 | - | 5.5 | V |
| Power Supply Current | I+ | $V_{IN}$ = 0 V, or V+ | Full | - | - | 2 | µA |

**Notes**

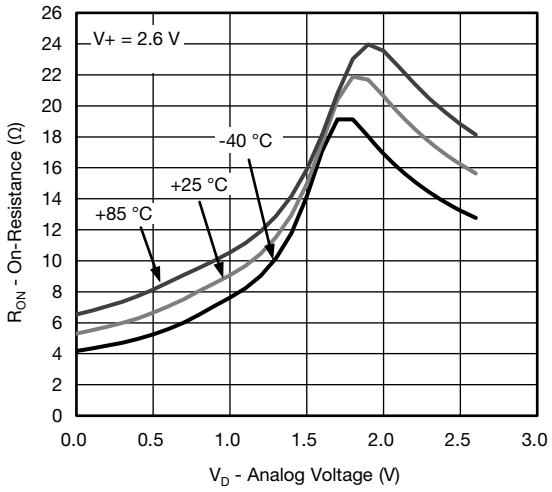
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, not subjected to production test.
e. $V_{IN}$ = input voltage to perform proper function.
f. Crosstalk measured between channels.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

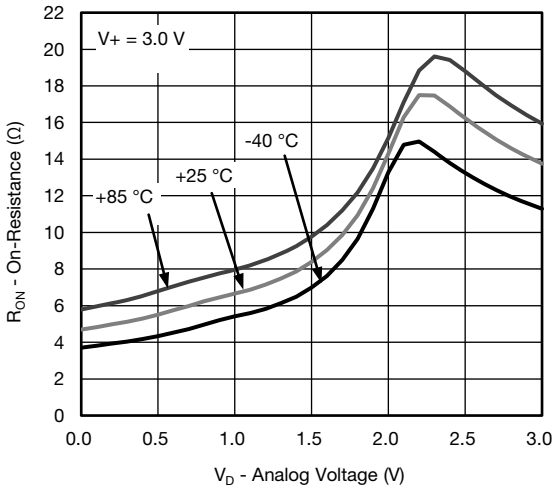
## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



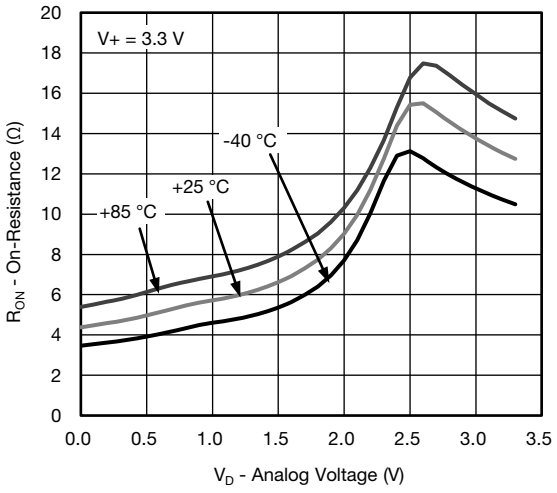

**$R_{ON}$ vs. $V_D$ and Single Supply Voltage**



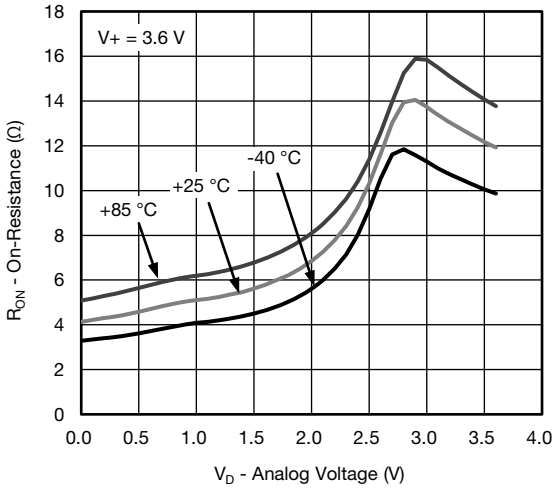

**$R_{ON}$ vs. Analog Voltage and Temperature**



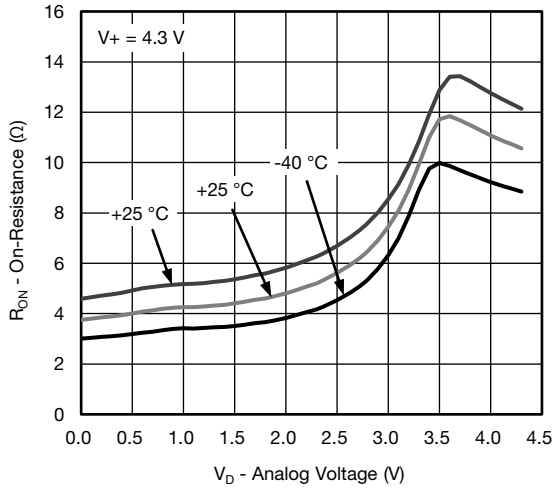

**$R_{ON}$ vs. Analog Voltage and Temperature**




**$R_{ON}$ vs. Analog Voltage and Temperature**

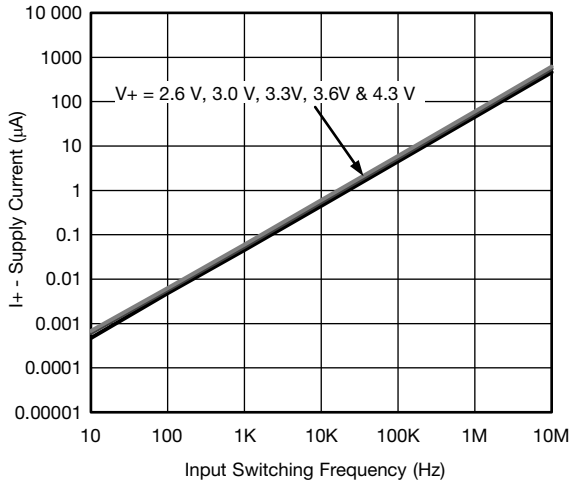



**$R_{ON}$ vs. Analog Voltage and Temperature**

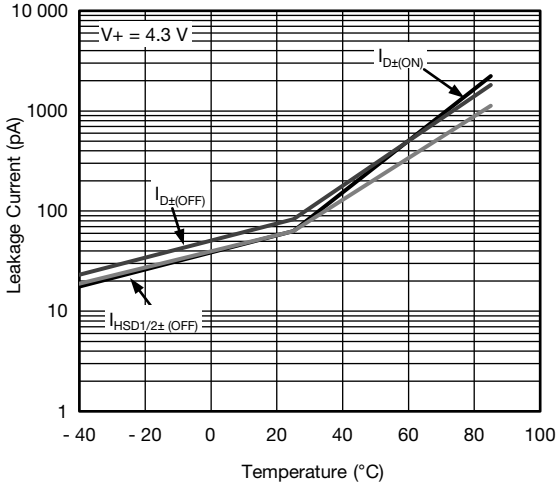



**$R_{ON}$ vs. Analog Voltage and Temperature**

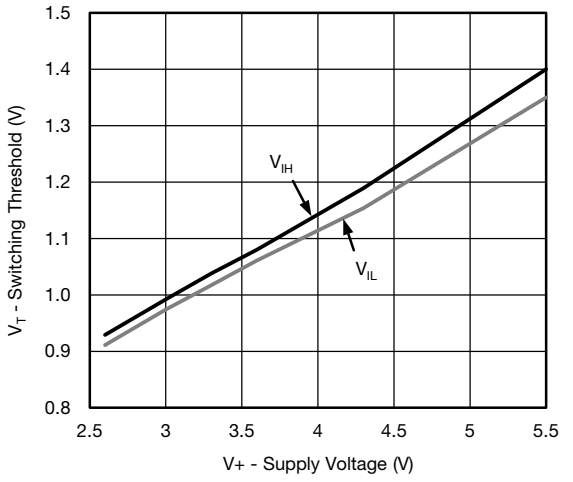
## TYPICAL CHARACTERISTICS ($T_A$ = 25 °C, unless otherwise noted)



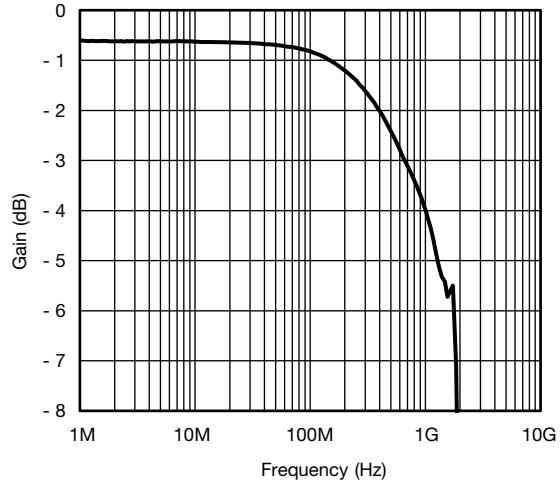

**Supply Current vs. Input Switching Frequency**



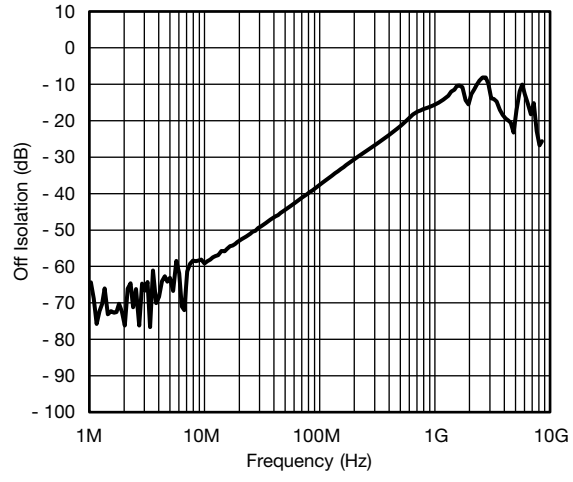

**Leakage Current vs. Temperature**



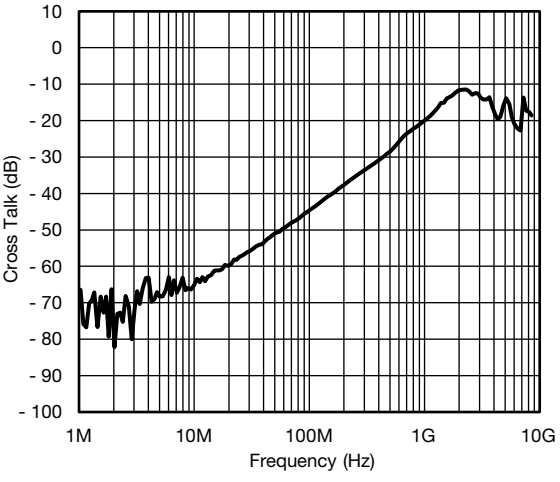

**Switching Threshold vs. Supply Voltage**




**Gain vs. Frequency, V+ = 3.3 V**

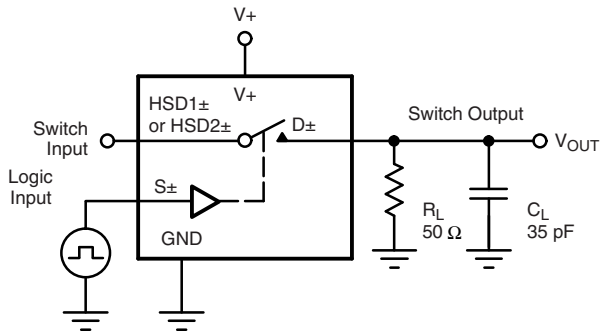



**Off-Isolation, V+ = 3.3 V**



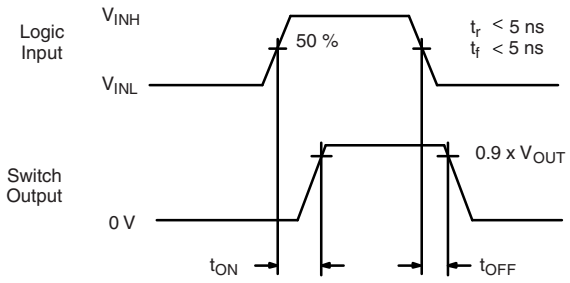

**Crosstalk, V+ = 3.3 V**

## TEST CIRCUITS



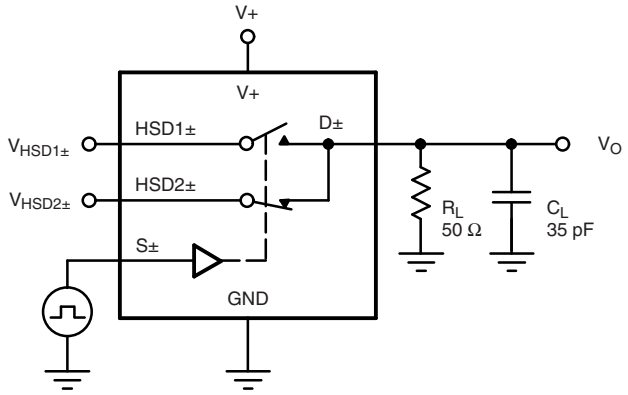

$C_L$ (includes fixture and stray capacitance)

$$V_{OUT} = D\pm \left(\frac{R_L}{R_L + R_{ON}}\right)$$




Logic "1" = Switch on
Logic input waveforms inverted for switches that have the opposite logic sense.

**Fig. 1 - Switching Time**




$C_L$ (includes fixture and stray capacitance)

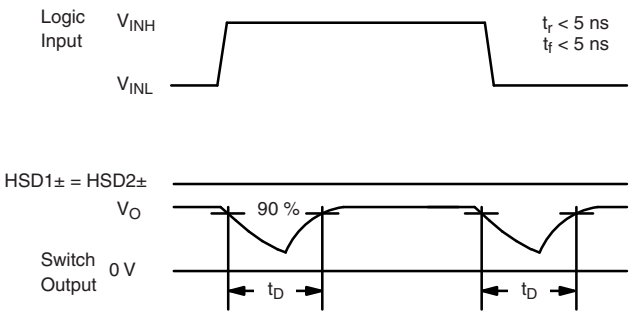
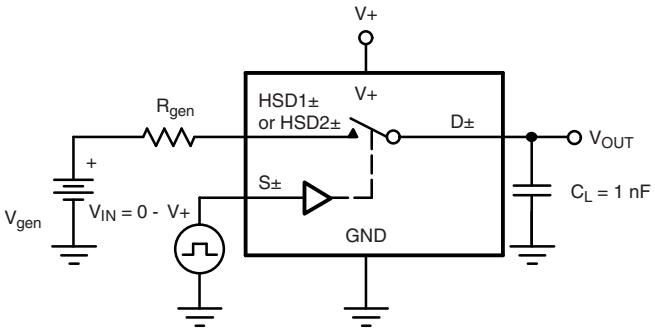
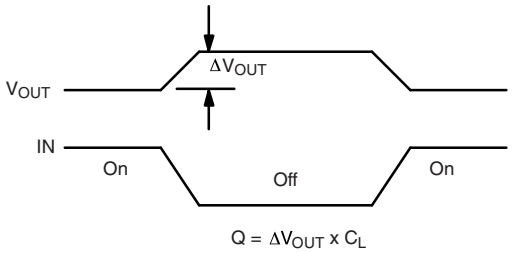



**Fig. 2 - Break-Before-Make Interval**




$Q = \Delta V_{OUT} \times C_L$

IN depends on switch configuration: input polarity determined by sense of switch.

**Fig. 3 - Charge Injection**

## TEST CIRCUITS

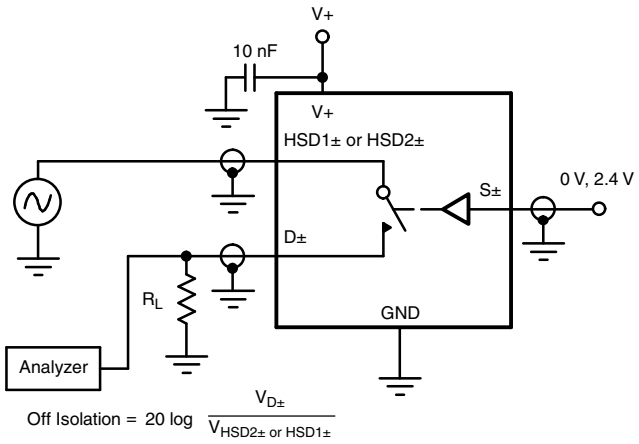



**Fig. 4 - Off-Isolation**

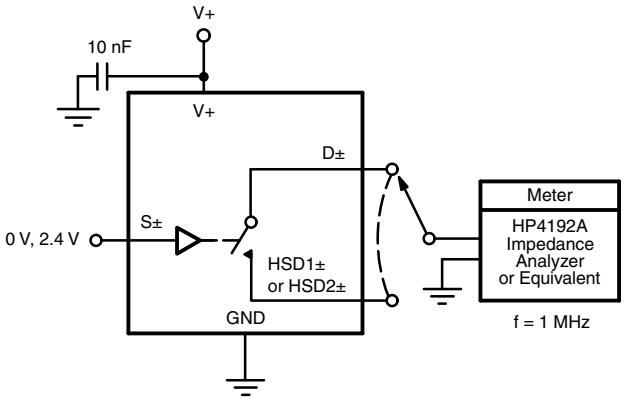
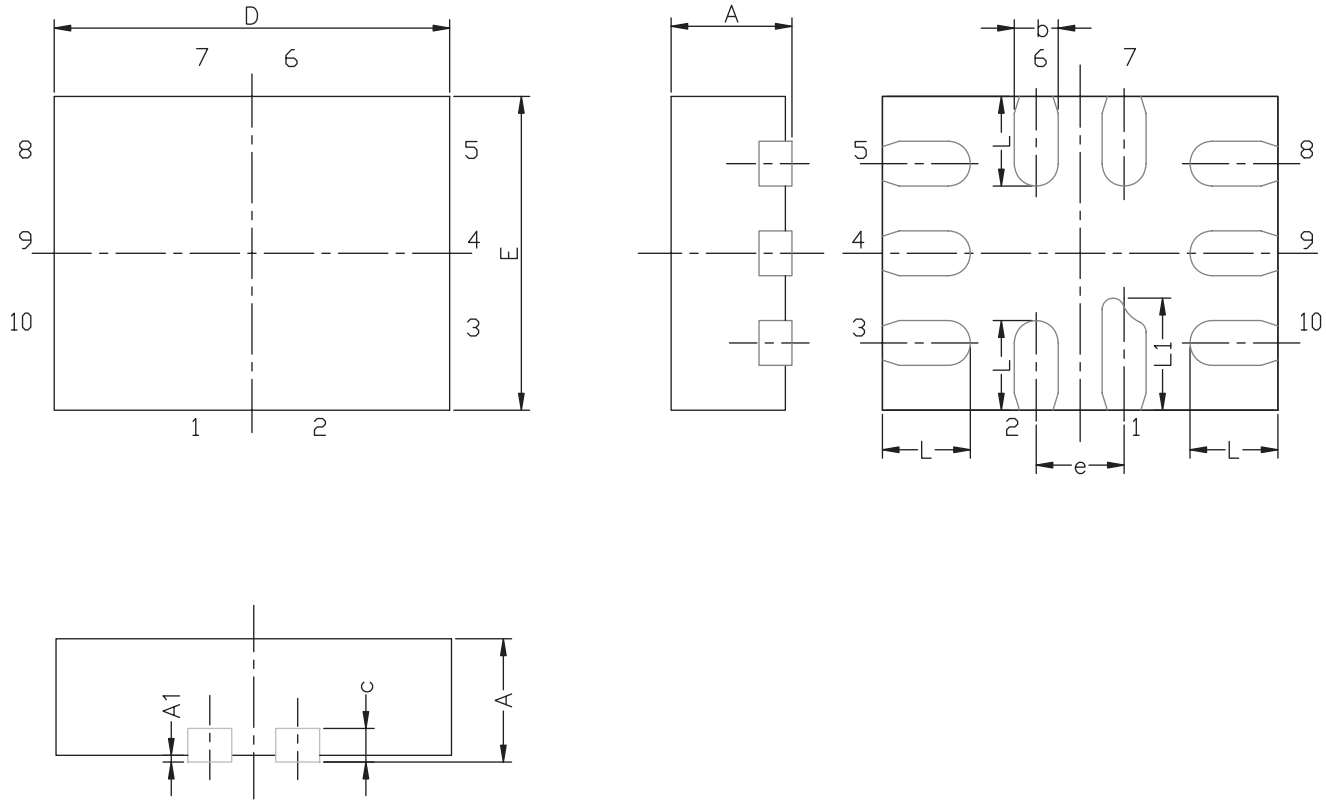



**Fig. 5 - Channel Off/On Capacitance**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68767.*

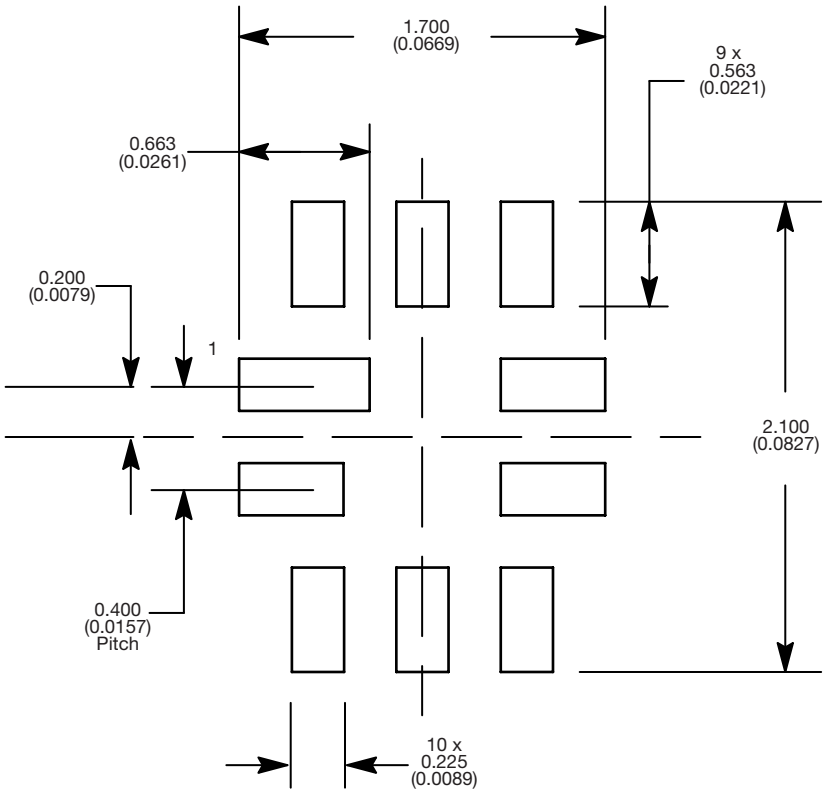
## MINI QFN-10L CASE OUTLINE




| DIM | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NAM. | MAX. | MIN. | NAM. | MAX. |
| A | 0.50 | 0.55 | 0.60 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.00 | - | 0.05 | 0.000 | - | 0.002 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| c | 0.15 REF | | | 0.006 REF | | |
| D | 1.75 | 1.80 | 1.85 | 0.069 | 0.071 | 0.073 |
| E | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| e | 0.40 BSC | | | 0.016 BSC | | |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| L1 | 0.45 | 0.50 | 0.55 | 0.0177 | 0.0197 | 0.0217 |

ECN T-07039-Rev. A, 12-Feb-07
DWG: 5957

**RECOMMENDED MINIMUM PADS FOR MINI QFN 10L**




Mounting Footprint
Dimensions in mm (inch)

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**

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