Low-Power, High-Speed CMOS Analog Switches

DESCRIPTION

The DG401B, DG403B, DG405B monolithic analog switches are replacements for the popular DG401/403/405 analog switches and provide improved performance, combining high speed (t_{ON}: 100 ns, typ) with low power consumption make the DG401B series ideal for portable and battery powered applications.

Built on the Vishay Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ± 15 V analog range. The DG401B has two independent SPST switches. The DG403B has four SPST switches in NO/NC combinations. The DG405B has four switches in two SPST pairs (see Functional Block Diagrams and Pin Configurations on pages 1 and 2.)

The DG401B, DG403B, DG405B is available in both 16-pin plastic dip and 16-pin SOIC packages.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100 % matte tin device terminations, the lead (Pb)-free "-E3" suffix is being used as a designator.

FEATURES

- 44 V supply max rating
- ± 15 V analog signal range
- On-resistance - $R_{DS(on)}$: 23 Ω
- Low leakage - $I_{D(on)}$: 40 pA
- Fast switching - t_{ON}: 100 ns
- Upgrade to DG401B, DG403B, DG405B
- TTL, CMOS compatible
- Single supply capability

BENEFITS

- Wide dynamic range
- Break-before-make switching action (DG403B only)
- Simple interfacing

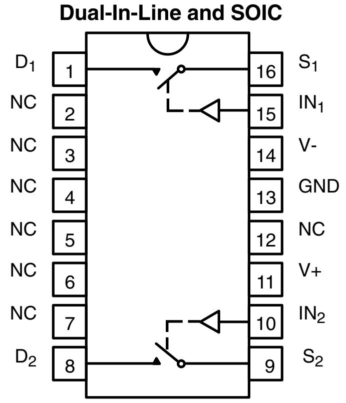
APPLICATIONS

- Audio and video switching
- Sample-and-hold circuits
- Test equipment
- PBX, PABX

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG401B

Dual-In-Line and SOIC



Top View

Two SPST Switches per Package

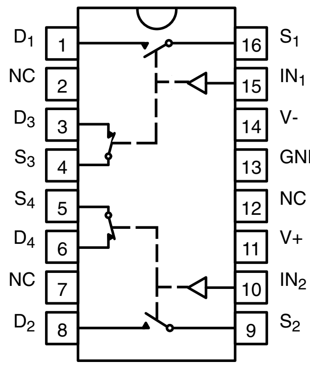
TRUTH TABLE	
Logic	**Switch**
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG403B

Dual-In-Line and SOIC



Top View

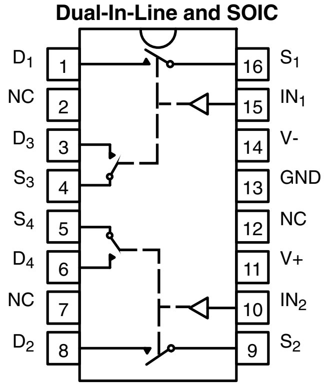
Four SPST Switches in Two Pairs per Package

TRUTH TABLE		
Logic	**SW_1, SW_2**	**SW_3, SW_4**
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

DG405B

Dual-In-Line and SOIC



Top View

Four SPST Switches in Two Pairs per Package

TRUTH TABLE	
Logic	**Switch**
0	OFF
1	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION			
Standard Commercial Part Number	**Lead (Pb)-free Commercial Part Number**	**Package**	**Temperature Range**
DG401BDJ	DG401BDJ-E3	16-Pin Plastic Dip	- 40 to 85 °C
DG403BDJ	DG403BDJ-E3		
DG405BDJ	DG405BDJ-E3		
DG401BDY	DG401BDY-E3	16-Pin Narrow SOIC	
DG403BDY	DG403BDY-E3		
DG405BDY	DG405BDY-E3		
DG401BDY-T1	DG401BDY-T1-E3	16-Pin Narrow SOIC With Tape and Reel	
DG403BDY-T1	DG403BDY-T1-E3		
DG405BDY-T1	DG405BDY-T1-E3		

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Limit	Unit
V+ to V-			44	V
GND to V-			25	
Digital Inputs[a], V_S, V_D			(V-) - 0.3 V to (V+) + 0.3 V or 30 mA, whichever occurs first	
Current (Any Terminal) Continuous			30	mA
Current, S or D (Pulsed 1 ms 10 % duty)			100	
Storage Temperature	(DJ, DY Suffix)		- 65 to 125	°C
Power Dissipation (Package)[b]	16-Pin Plastic DIP[c]		450	mW
	16-Pin SOIC[d]		600	

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 6 mW/°C above 75 °C.
d. Derate 7.6 mW/°C above 75 °C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

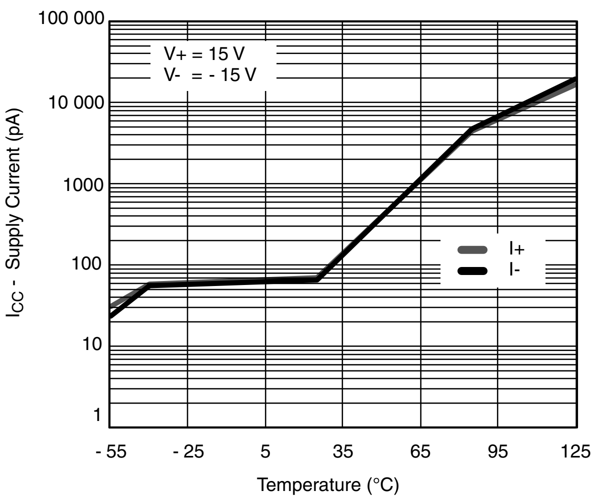
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V- = - 15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp.[b]	Limits - 40 °C to 85 °C Min.[d]	Typ.[c]	Max.[d]	Unit
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	-15		15	V
Drain-Source On-Resistance	$R_{DS(on)}$	I_S = - 10 mA, V_D = ± 10 V V+ = 13.5 V, V- = - 13.5 V	Room Full		23	45 55	Ω
Δ Drain-Source On-Resistance	$\Delta R_{DS(on)}$	I_S = - 10 mA, V_D = ± 5 V, 0 V V+ = 16.5 V, V- = - 16.5 V	Room Full		0.72	3 5	
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5, V- = - 16.5 V V_D = ± 15.5 V, V_S = ± 15.5 V	Room Hot	- 0.5 - 5	- 0.01	0.5 5	nA
	$I_{D(off)}$		Room Hot	- 0.5 - 5	- 0.01	0.5 5	
Channel On Leakage Current	$I_{D(on)}$	V+ = 16.5 V, V- = - 16.5 V V_S = V_D = ± 15.5 V	Room Hot	- 1 - 10	- 0.04	1 10	
Digital Control							
Input Current V_{IN} Low	I_{IL}	V_{IN} under test = 0.8 V, all other = 2.4 V	Full	- 1	0.005	1	µA
Input Current V_{IN} High	I_{IH}	V_{IN} under test = 2.4 V, all other = 0.8 V	Full	- 1	0.005	1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF see figure 2	Room		100	150	ns
Turn-Off Time	t_{OFF}		Room		60	100	
Break-Before-Make Time Delay (DG403B)	t_D	R_L = 300 Ω, C_L = 35 pF	Room	5	12		
Charge Injection	Q	C_L = 10 000 pF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		60		pC
Off Isolation Reject Ratio	OIRR	R_L = 100 Ω, C_L = 5 pF, f =1 MHz	Room		- 81.7		dB
Channel-to-Channel Crosstalk	X_{TALK}		Room		- 94.8		
Source Off Capacitance	$C_{S(off)}$	f = 1 MHz, V_S = 0 V	Room		12		pF
Drain Off Capacitance	$C_{D(off)}$		Room		12		
Channel On Capacitance	C_D, $C_{S(on)}$		Room		39		

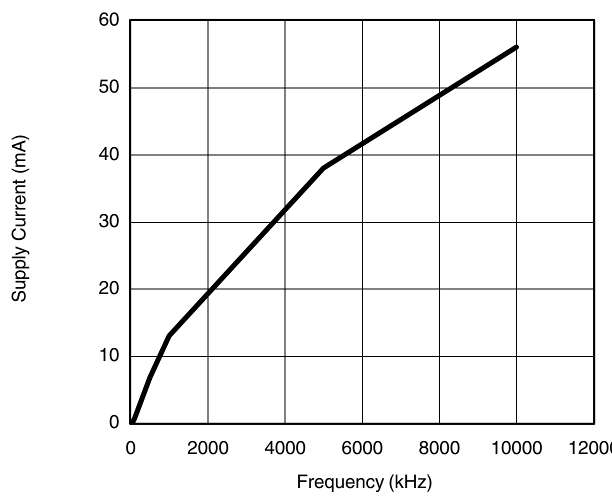
SPECIFICATIONS[a]							
Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V- = - 15 V V_{IN} = 2.4 V, 0.8 V[f]	Temp. b	Limits - 40 °C to 85 °C Min.[d]	Typ.[c]	Max.[d]	Unit
Power Supplies							
Positive Supply Current	I+	V+ = 16.5 V, V- = - 16.5 V V_{IN} = 0 or 5 V	Room Full		0.250	0.5 1	mA
Negative Supply Current	I-		Room Full	- 0.5 - 1	0.25		
Ground Current	I_{GND}		Room Full	- 0.5 - 1	0.25		

Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

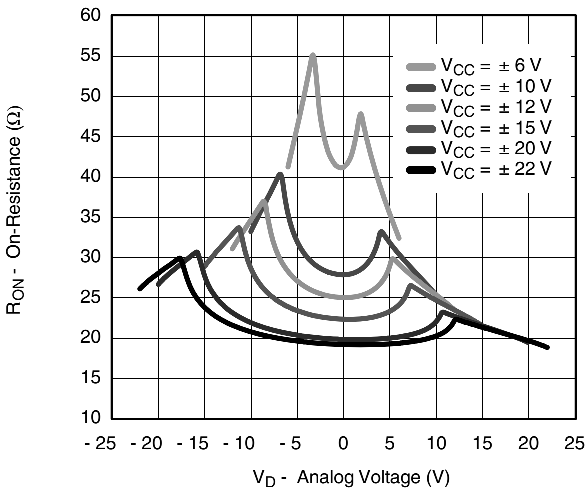


Supply Current vs. Temperature

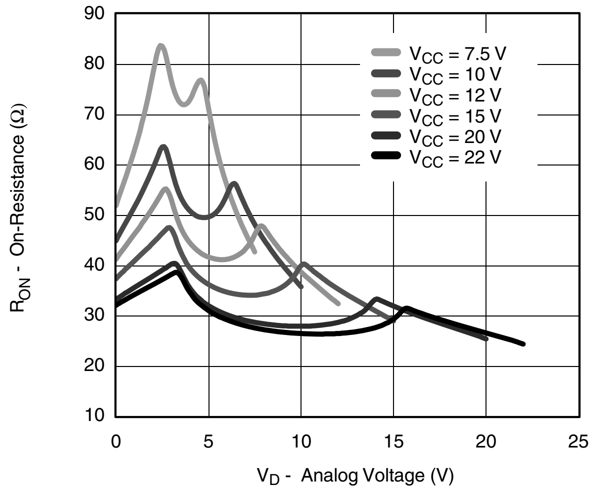


Supply Current vs. Switching Frequency

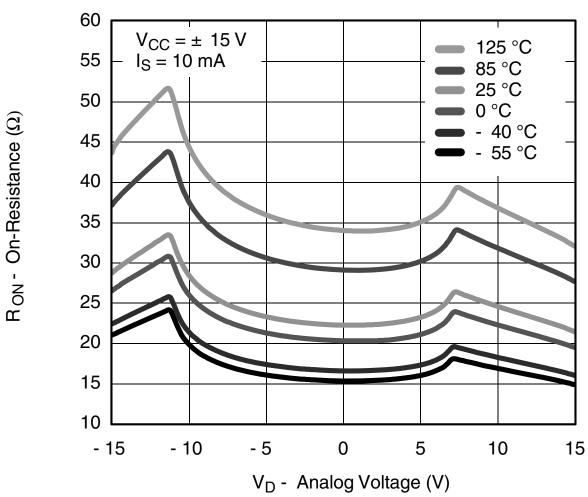
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



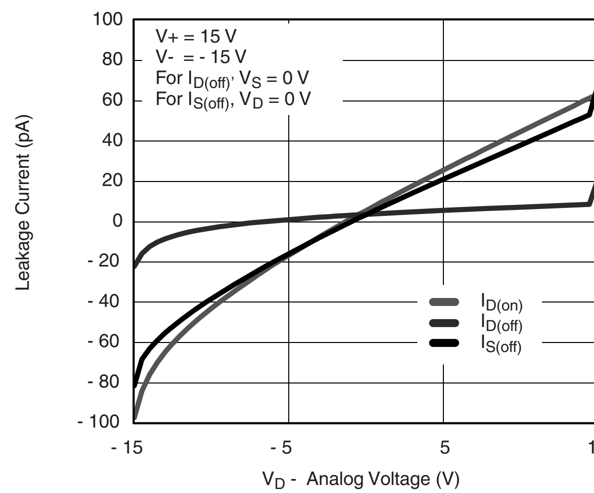
R_{ON} vs. Analog Voltage and Supply Voltage



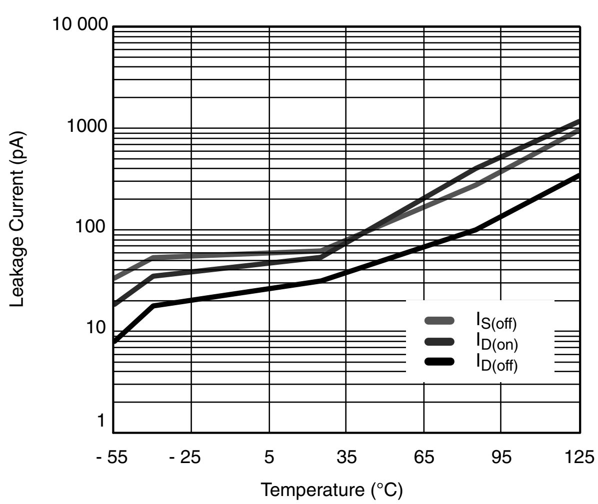
R_{ON} vs. Analog Voltage and Single Supply Voltage



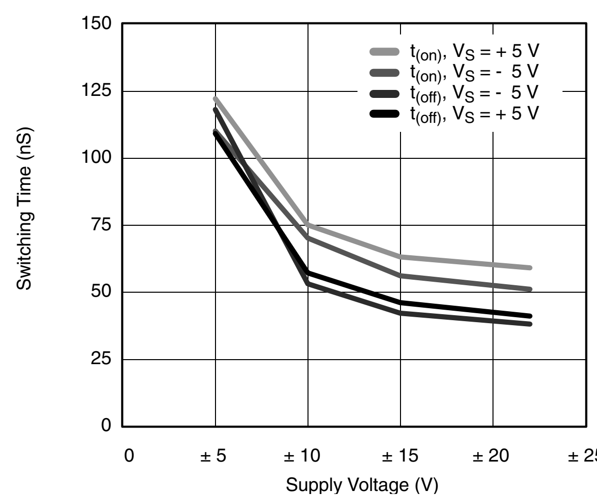
R_{ON} vs. Analog Voltage and Temperature



Leakage Current vs. Analog Voltage

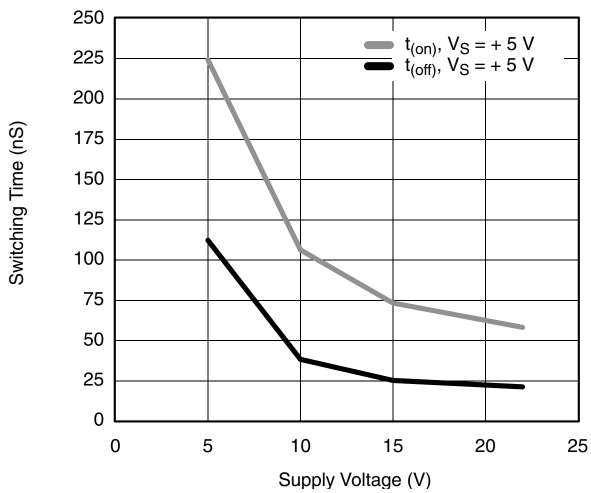


Leakage Current vs. Temperature

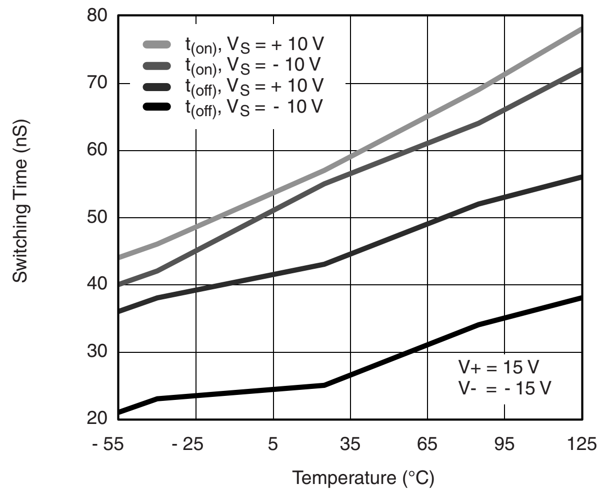


Switching Time vs. Supply Voltage

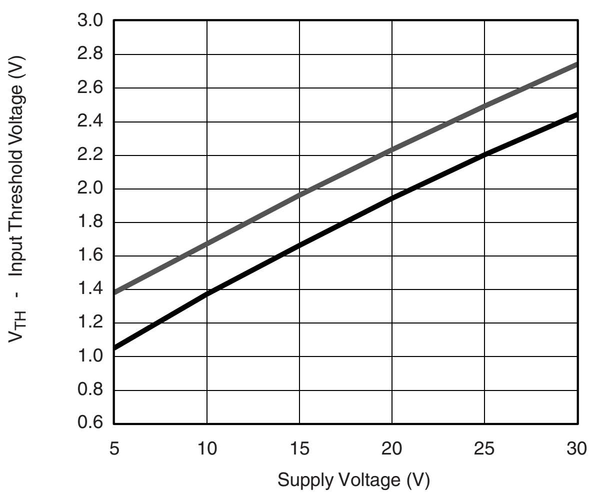
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



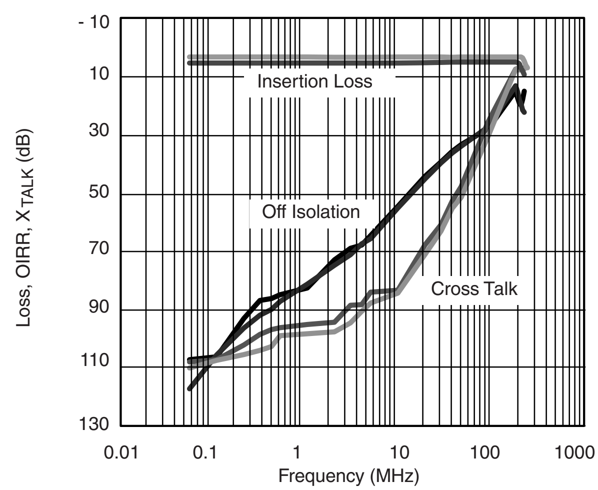
Switching Time vs. Single Supply Voltage



Switching Time vs. Temperature



Input Switching Threshold vs. Supply Voltage



Insertion Loss, Off -Isolation Crosstalk vs. Frequency

SCHEMATIC DIAGRAM (Typical Channel)

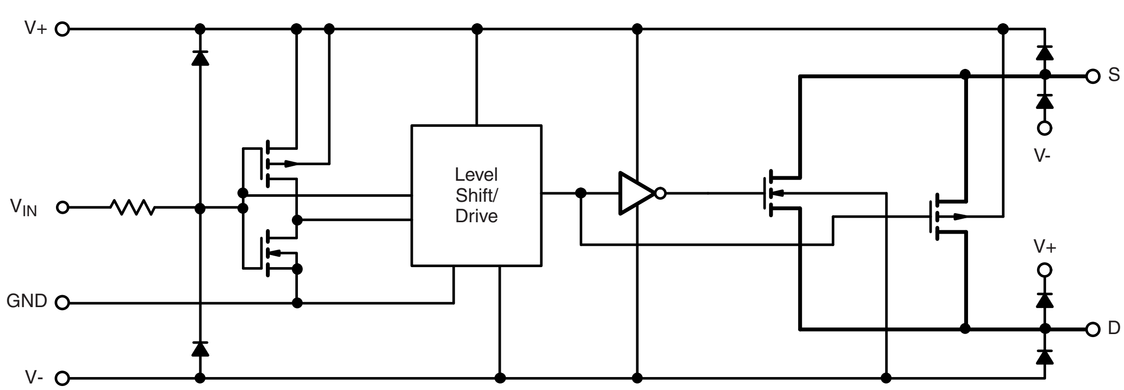


Figure 1.

TEST CIRCUITS

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

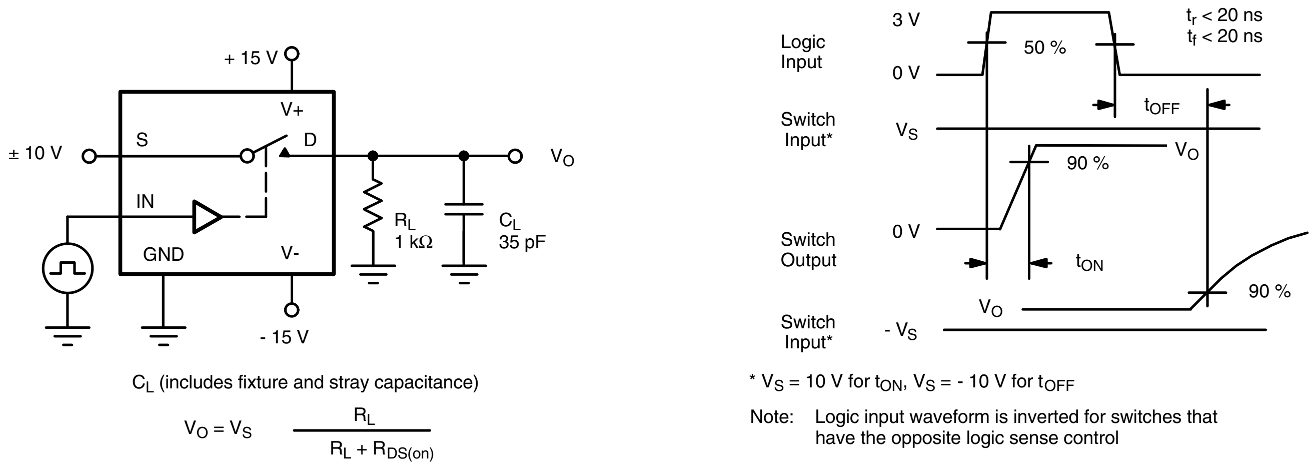


Figure 2. Switching Time

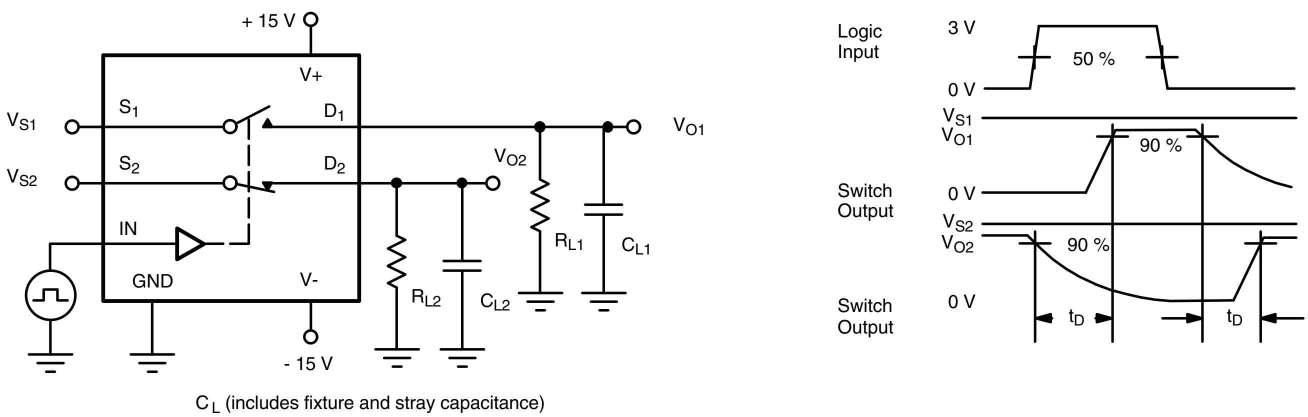


Figure 3. Break-Before-Make

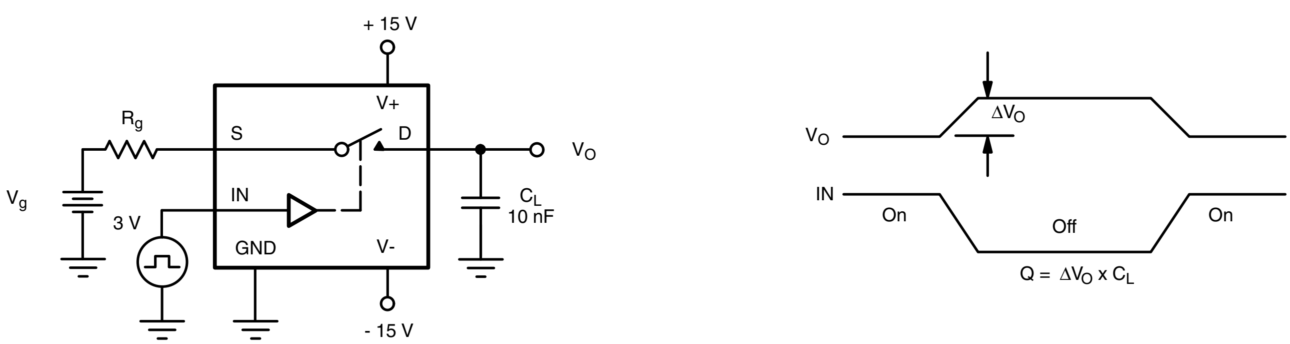
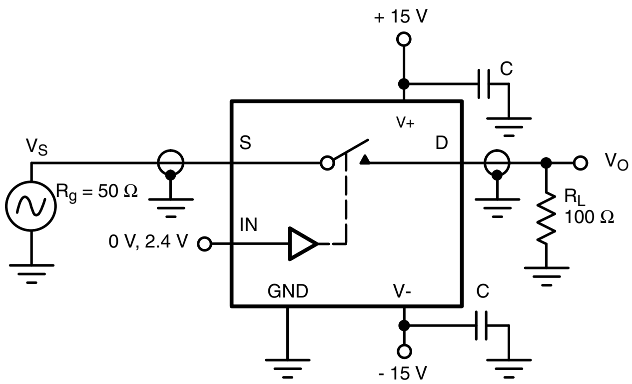


Figure 4. Charge Injection

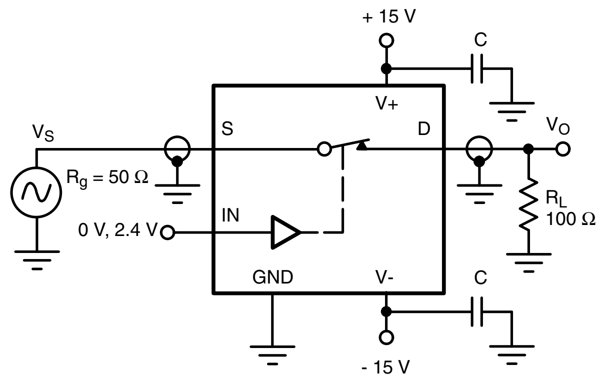
TEST CIRCUITS



$$\text{Off Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

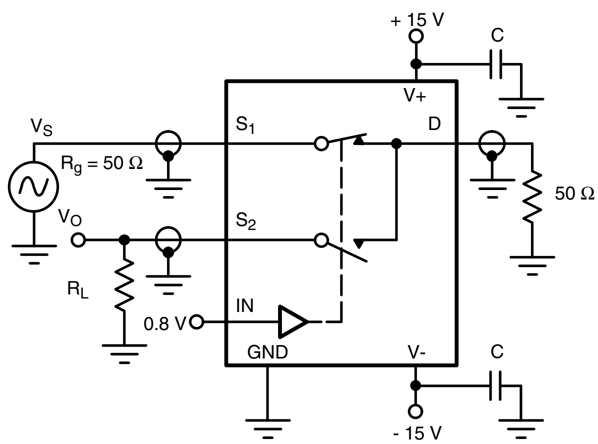
C = RF bypass

Figure 5. Off Isolation



C = RF bypass

Figure 6. Insertion Loss



$$X_{TALK} \text{ Isolation} = 20 \log \left| \frac{V_S}{V_O} \right|$$

C = RF bypass

Figure 7. Crosstalk

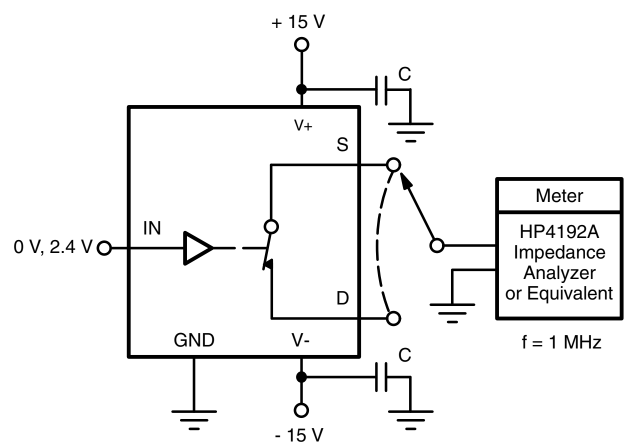


Figure 8. Capacitances

APPLICATIONS

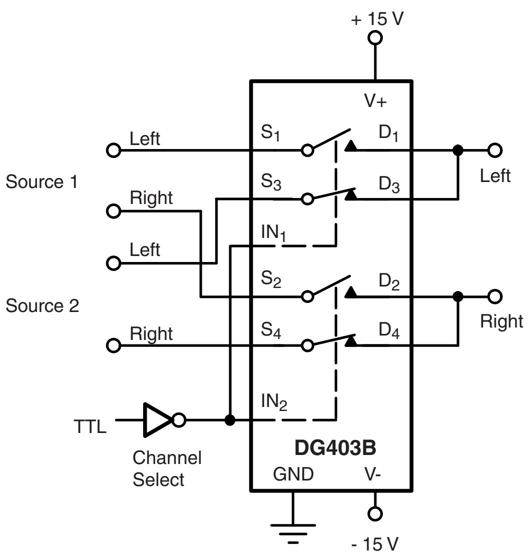


Figure 9. Stereo Source Selector

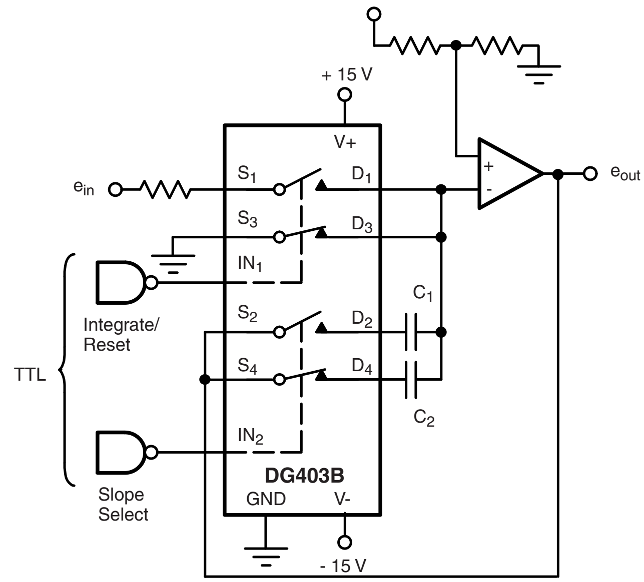


Figure 10. Dual Slope Integrator

Dual Slope Integrators

The DG403B is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{in} or discharges the capacitor in preparation for the next integration cycle.

Band-Pass Switched Capacitor Filter

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403B allow for higher clock rates and consequently higher filter operating frequencies.

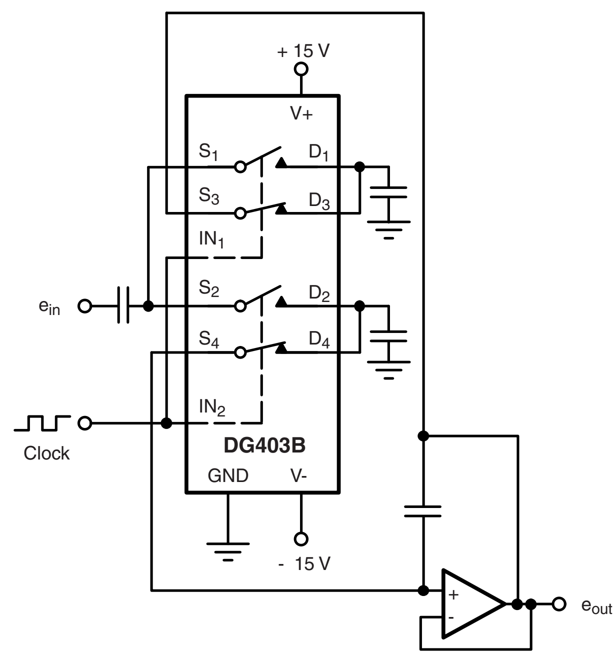


Figure 11. Band-Pass Switched Capacitor Filter

APPLICATIONS

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1. The output of A_2 is fed back to A_3 and compared to the analog input ein. If $e_{in} > e_{out}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{in} goes below e_{out} A_3 goes negative, turning SW_1 off. The system will therefore store the most positive analog input experienced.

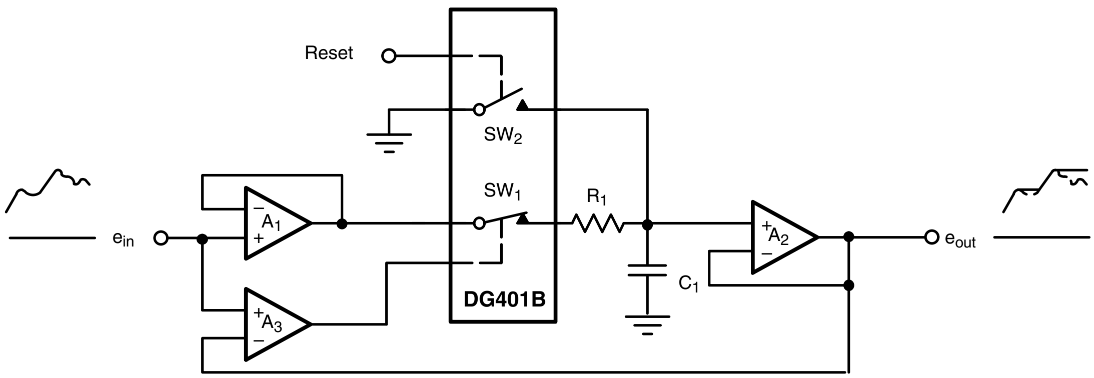
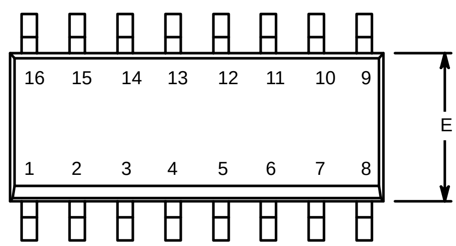


Figure 12. Positive Peak Detector

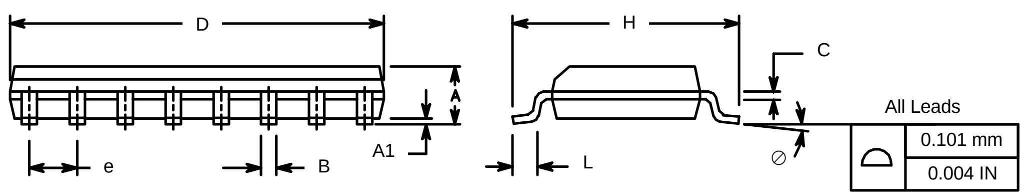
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73069.

SOIC (NARROW): 16-LEAD

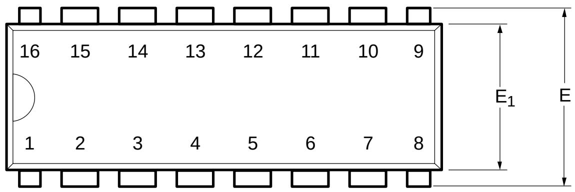
JEDEC Part Number: MS-012

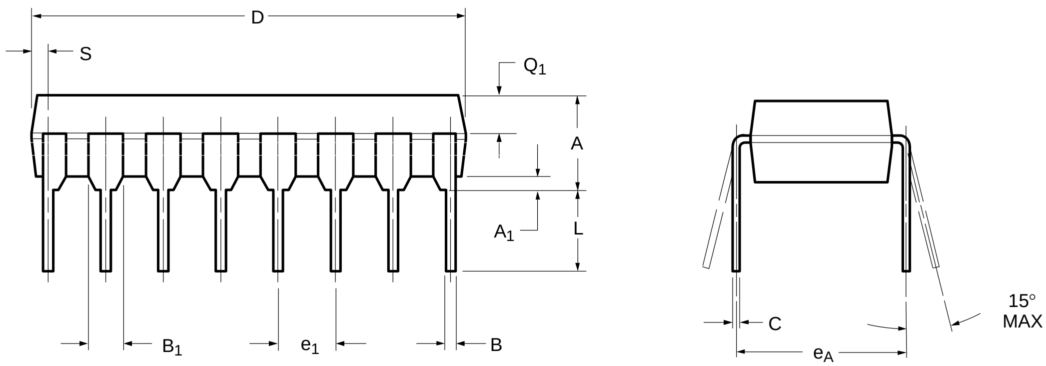


Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
∅	0°	8°	0°	8°
ECN: S-03946—Rev. F, 09-Jul-01 DWG: 5300				



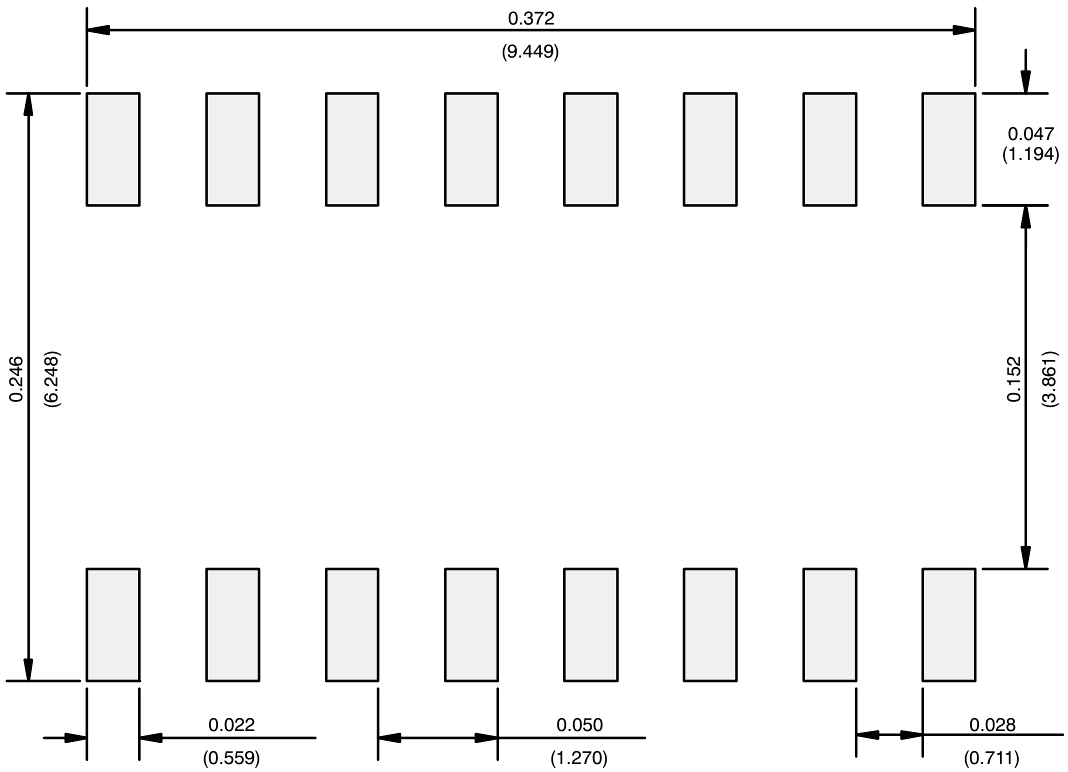
PDIP: 16-LEAD





Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	3.81	5.08	0.150	0.200
A_1	0.38	1.27	0.015	0.050
B	0.38	0.51	0.015	0.020
B_1	0.89	1.65	0.035	0.065
C	0.20	0.30	0.008	0.012
D	18.93	21.33	0.745	0.840
E	7.62	8.26	0.300	0.325
E_1	5.59	7.11	0.220	0.280
e_1	2.29	2.79	0.090	0.110
e_A	7.37	7.87	0.290	0.310
L	2.79	3.81	0.110	0.150
Q_1	1.27	2.03	0.050	0.080
S	0.38	1.52	.015	0.060
ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482				

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.