

## 16-Ch/Dual 8-Ch High-Performance CMOS Analog Multiplexers

### DESCRIPTION

The DG406B is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407B selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address ( $A_x$ ) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG406B, DG407B include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 volts, allowing operation with  $\pm 20$  V supplies. Additionally single (12 V) supply operation is allowed. An epitaxial layer prevents latchup.

### FEATURES

- Low on-resistance -  $R_{DS(on)}$ : 45  $\Omega$
- Low charge injection - Q: 11 pC
- Fast transition time -  $t_{TRANS}$ : 115 ns
- Low power: 0.2 mW
- Single supply capability



**RoHS\***  
COMPLIANT

### BENEFITS

- Higher accuracy
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges:  $\pm 5$  V to  $\pm 20$  V

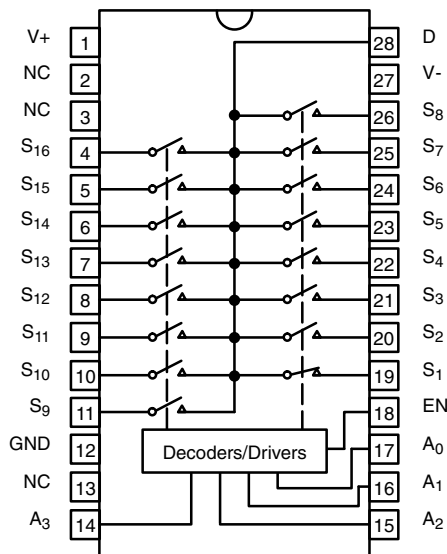
### APPLICATIONS

- Data acquisition systems
- Audio signal routing
- Medical instrumentation
- ATE systems
- Battery powered systems
- High-rel systems
- Single supply systems

### FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406B

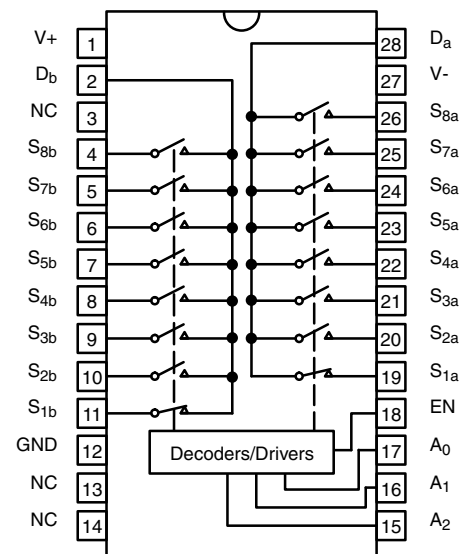
Dual-In-Line and SOIC Wide-Body



Top View

DG407B

Dual-In-Line and SOIC Wide-Body



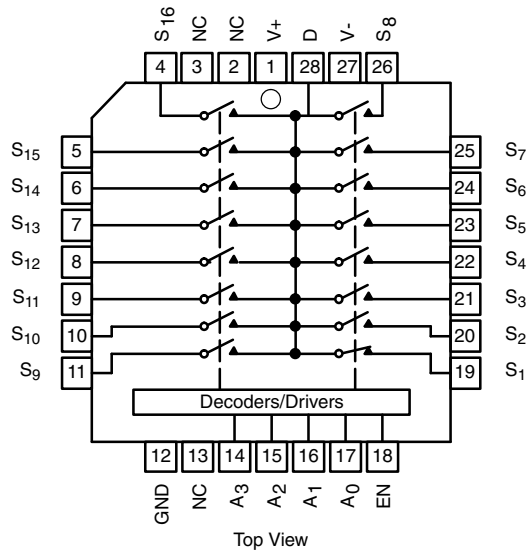
Top View

\* Pb containing terminations are not RoHS compliant, exemptions may apply

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

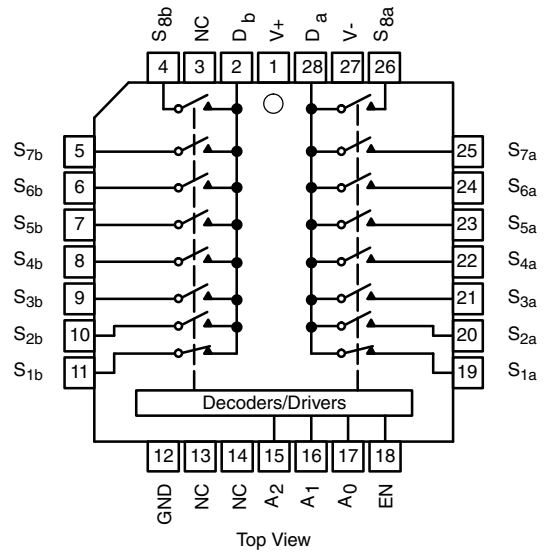
DG406B

PLCC and LCC



DG407B

PLCC and LCC



### TRUTH TABLE (DG406B)

A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

### TRUTH TABLE (DG407B)

A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V<sub>AL</sub> ≤ 0.8 V  
 Logic "1" = V<sub>AH</sub> ≥ 2.4 V  
 X = Do not Care

### ORDERING INFORMATION (DG406B)

Temp. Range	Package	Part Number
- 40 °C to 85 °C	28-Pin Plastic DIP	DG406BDJ DG406BDJ-E3
	28-Pin PLCC	DG406BDN DG406BDN-T1-E3
	28-Pin Widebody SOIC	DG406BDW DG406BDW-E3

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ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs <sup>a</sup> , V <sub>S</sub> , V <sub>D</sub>		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature		- 65 to 150	°C
Power Dissipation (Package) <sup>b</sup>	28-Pin Plastic DIP <sup>c</sup>	625	mW
	28-Pin CerDIP <sup>d</sup>	1.2	W
	28-Pin Plastic PLCC <sup>c</sup>	450	mW
	LCC-28 <sup>e</sup>	1.35	W
	28-Pin Widebody SOIC <sup>f</sup>	450	mW

Notes:

- a. Signals on S<sub>X</sub>, D<sub>X</sub> or I<sub>NX</sub> exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads soldered or welded to PC board.
- c. Derate 8.3 mW/°C above 75 °C.
- d. Derate 16 mW/°C above 75 °C.
- e. Derate 18 mW/°C above 75 °C.
- f. Derate 6 mW/°C above 75 °C.

SPECIFICATIONS										
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$ , $V_- = -15\text{ V}$ $V_{AL} = 0.8\text{ V}$ , $V_{AH} = 2.4\text{ V}^f$	Temp. <sup>b</sup>	Typ. <sup>c</sup>	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit	
					Min. <sup>d</sup>	Max. <sup>d</sup>	Min. <sup>d</sup>	Max. <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		- 15	15	- 15	15	V	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_D = \pm 10\text{ V}$ , $I_S = -10\text{ mA}$ sequence each switch on	Room Full	45		60 87		60 74	$\Omega$	
$r_{DS(on)}$ Matching Between Channels <sup>g</sup>	$\Delta R_{DS(on)}$	$V_D = \pm 10\text{ V}$	Room	5					%	
Source Off Leakage Current	$I_{S(off)}$	$V_{EN} = 0\text{ V}$ $V_D = \pm 10\text{ V}$ $V_S = \pm 10\text{ V}$	Room Full		- 0.5 - 50	0.5 50	- 0.5 - 5	0.5 5	nA	
Drain Off Leakage Current	$I_{D(off)}$		DG406B	Room Full		- 1 - 200	1 200	- 1 - 40		1 40
			DG407B	Room Full		- 1 - 100	1 100	- 1 - 20		1 20
Drain On Leakage Current	$I_{D(on)}$		DG406B	Room Full		- 1 - 200	1 200	- 1 - 40		1 40
		DG407B	Room Full		- 1 - 100	1 100	- 1 - 20	1 20		
<b>Digital Control</b>										
Logic High Input Voltage	$V_{INH}$		Full		2.4		2.4		V	
Logic Low Input Voltage	$V_{INL}$		Full			0.8		0.8	V	
Logic High Input Current	$I_{AH}$	$V_A = 2.4\text{ V}$ , 15 V	Full		- 1	1	- 1	1	$\mu\text{A}$	
Logic Low Input Current	$I_{AL}$	$V_{EN} = 0\text{ V}$ , 2.4 V, $V_A = 0\text{ V}$	Full		- 1	1	- 1	1	$\mu\text{A}$	
Logic Input Capacitance	$C_{in}$	$f = 1\text{ MHz}$	Room	6					pF	
<b>Dynamic Characteristics</b>										
Transition Time	$t_{TRANS}$	see figure 2	Room Full	115		148 170		148 161	ns	
Break-Before-Make Interval	$t_{OPEN}$	see figure 4	Room Full	39	10 29		10 21			
Enable Turn-On Time	$t_{ON(EN)}$	see figure 3	Room Full	75		107 134		107 123		
Enable Turn-Off Time	$t_{OFF(EN)}$		Room Full	50		88 98		88 94		
Charge Injection	Q	$C_L = 1\text{ nF}$ , $V_S = 0\text{ V}$ , $R_S = 0\ \Omega$	Room	11					pC	
Off Isolation <sup>h</sup>	OIRR	$V_{EN} = 0\text{ V}$ , $R_L = 50\ \Omega$ $f = 1\text{ MHz}$	Room	- 86					dB	
Source Off Capacitance	$C_{S(off)}$	$V_{EN} = 0\text{ V}$ , $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	Room	6					pF	
Drain Off Capacitance	$C_{D(off)}$	$V_{EN} = 0\text{ V}$ $V_D = 0\text{ V}$ $f = 1\text{ MHz}$	Room	108						
			DG407B	Room	54					
Drain On Capacitance	$C_{D(on)}$		DG406B	Room	114					
			DG407B	Room	57					
<b>Power Supplies</b>										
Positive Supply Current	I+	$V_{EN} = V_A = 0\text{ or }5\text{ V}$	Room Full	23		30 75		30 75	$\mu\text{A}$	
Negative Supply Current	I-		Room Full	- 0.02	- 1 - 10		- 1 - 10			
Positive Supply Current	I+	$V_{EN} = 2.4\text{ V}$ , $V_A = 0\text{ V}$	Room Full	28		500 900		500 700		
Negative Supply Current	I-		Room Full	- 0.01	- 20 - 20		- 20 - 20			



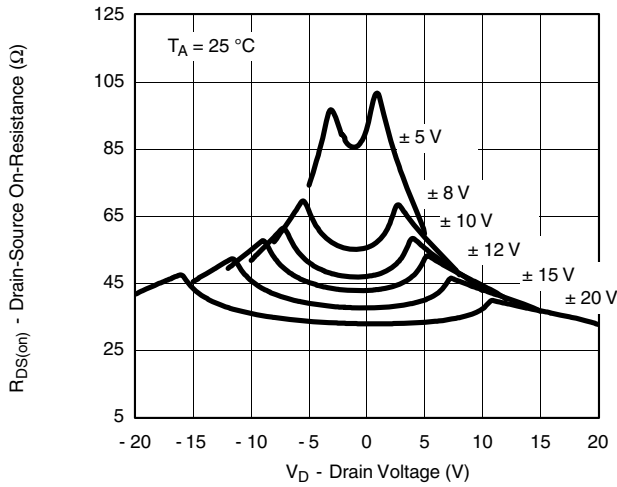
SPECIFICATIONS FOR SINGLE SUPPLY										
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$ , $V_- = 0\text{ V}$ $V_{AL} = 0.8\text{ V}$ , $V_{AH} = 2.4\text{ V}^f$	Temp. <sup>b</sup>	Typ. <sup>c</sup>	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit	
					Min. <sup>d</sup>	Max. <sup>d</sup>	Min. <sup>d</sup>	Max. <sup>d</sup>		
<b>Analog Switch</b>										
Analog Signal Range <sup>e</sup>	$V_{ANALOG}$		Full		0	12	0	12	V	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_D = 3\text{ V}$ , $I_S = -1\text{ mA}$ sequence each switch on	Room	78		100		100	$\Omega$	
$r_{DS(on)}$ Matching Between Channels <sup>g</sup>	$\Delta R_{DS(on)}$		Room	5					%	
Source Off Leakage Current <sup>a</sup>	$I_{S(off)}$	$V_{EN} = 0\text{ V}$ $V_D = 10\text{ V}$ or $0.5\text{ V}$ $V_S = 0.5\text{ V}$ or $10\text{ V}$ $V_S = V_D = \pm 10\text{ V}$ sequence each switch on	Room		-0.5	0.5	-0.5	0.5	nA	
Drain Off Leakage Current <sup>a</sup>	$I_{D(off)}$		DG406B	Room		-1	1	-1		1
			DG407B	Room		-1	1	-1		1
Drain On Leakage Current <sup>a</sup>	$I_{D(on)}$		DG406B	Room		-1	1	-1		1
		DG407B	Room		-1	1	-1	1		
<b>Dynamic Characteristics</b>										
Switching Time of Multiplexer	$t_{TRANS}$	$V_{S1} = 8\text{ V}$ , $V_{S8} = 0\text{ V}$ , $V_{IN} = 2.4\text{ V}$	Room	130		163		163	ns	
Enable Turn-On Time	$t_{ON(EN)}$	$V_{INH} = 2.4\text{ V}$ , $V_{INL} = 0\text{ V}$ $V_{S1} = 5\text{ V}$	Room	93		125		125		
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	63		94		94		
Charge Injection	Q	$C_L = 1\text{ nF}$ , $V_S = 6\text{ V}$ , $R_S = 0$	Room	9					pC	
<b>Power Supplies</b>										
Positive Supply Current	I+	$V_{EN} = 0\text{ V}$ or $5\text{ V}$ , $V_A = 0\text{ V}$ or $5\text{ V}$	Room	13		30		30	$\mu\text{A}$	
Negative Supply Current	I-		Full			75		75		
			Room	-0.01	-20		-20			
			Full		-20		-20			

Notes:

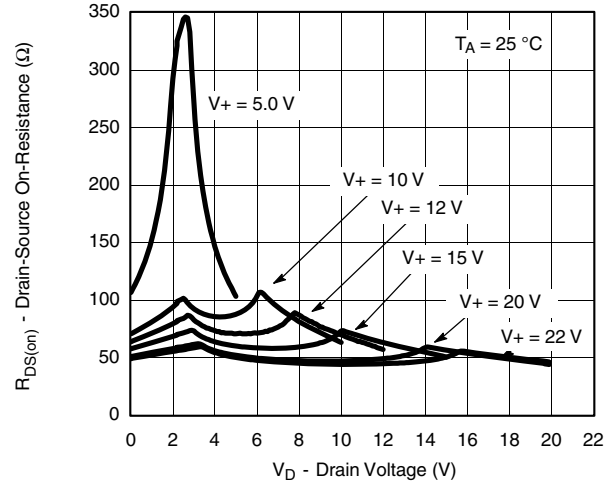
- a. Guaranteed by  $\pm 15\text{ V}$  leakage test, not production tested.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f.  $V_{IN}$  = input voltage to perform proper function.
- g.  $\Delta R_{DS(on)} = R_{DS(on)} \text{ MAX.} - R_{DS(on)} \text{ MIN.}$
- h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

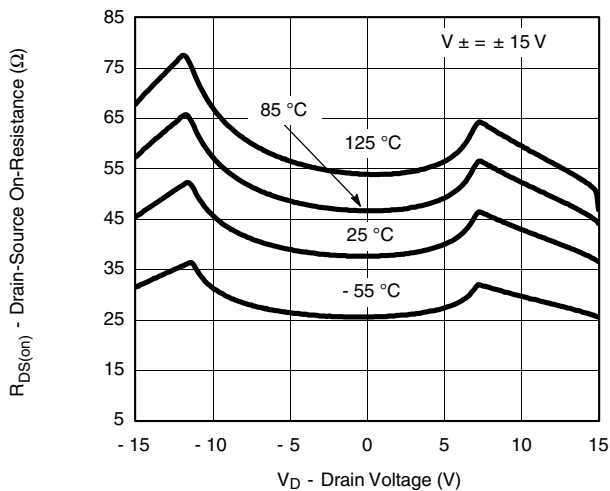
### TYPICAL CHARACTERISTICS ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



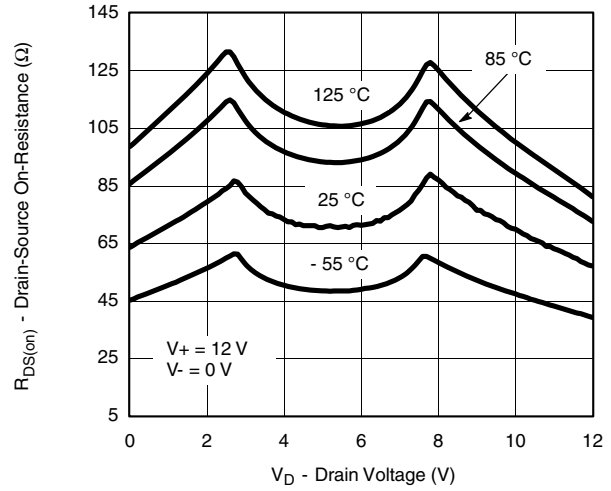
**On-Resistance vs.  $V_D$  and Dual Supply Voltage**



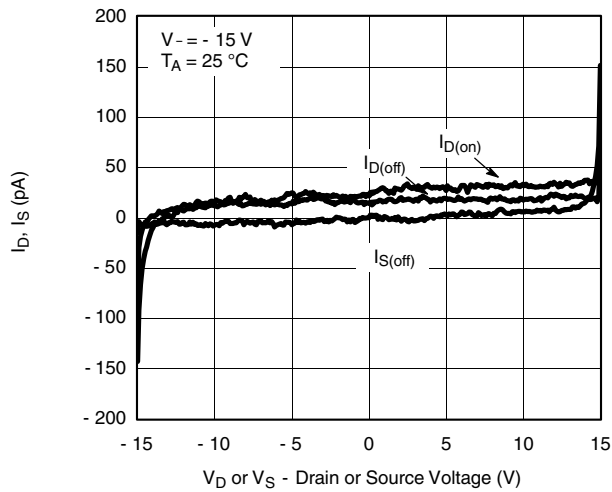
**On-Resistance vs.  $V_D$  and Unipolar Supply Voltage**



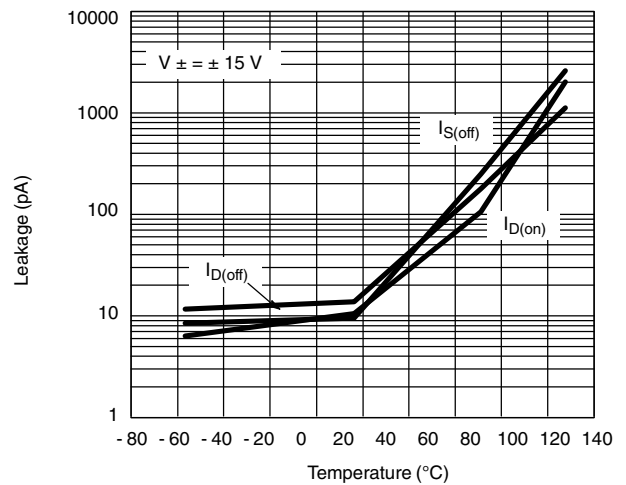
**On-Resistance vs.  $V_D$  and Temperature**



**On-Resistance vs.  $V_D$  and Temperature**

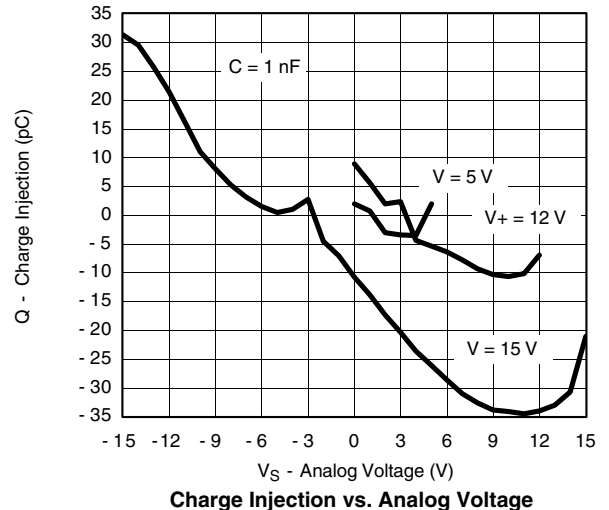
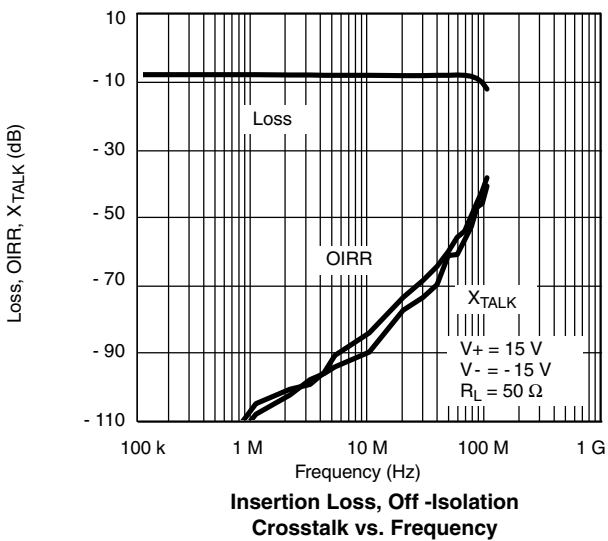
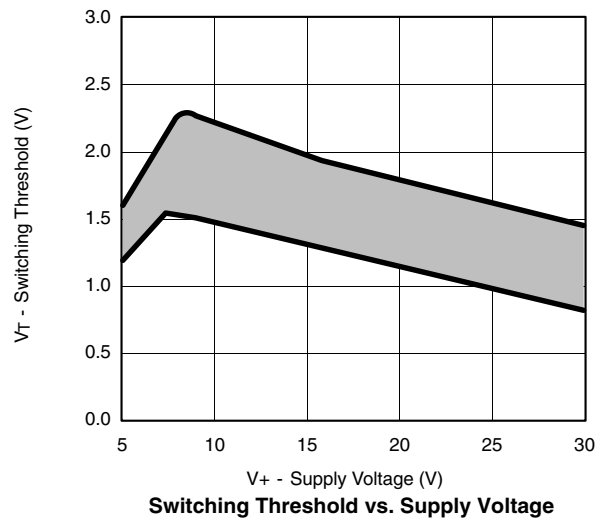
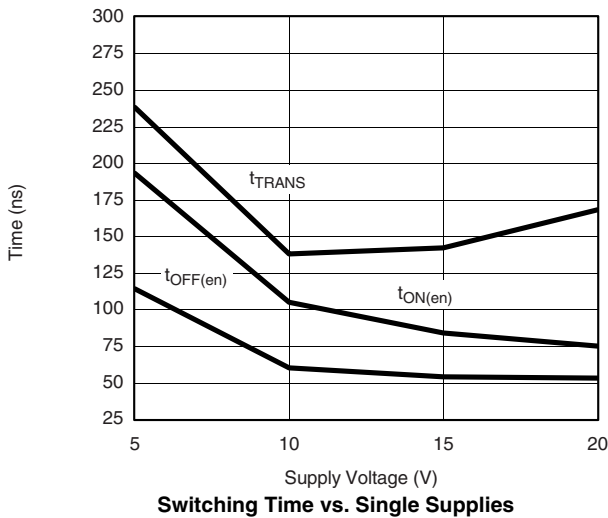
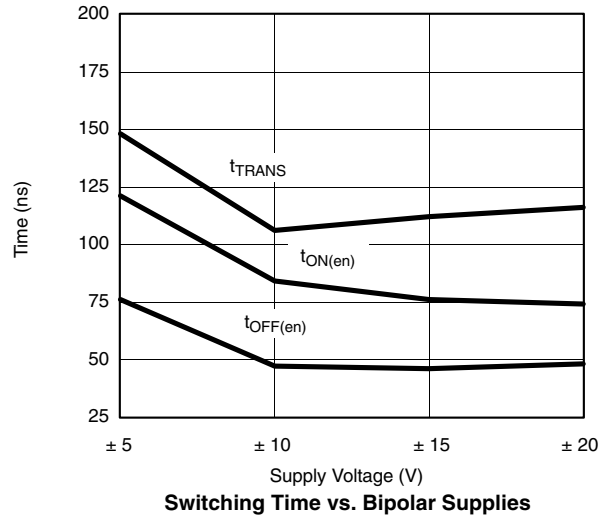
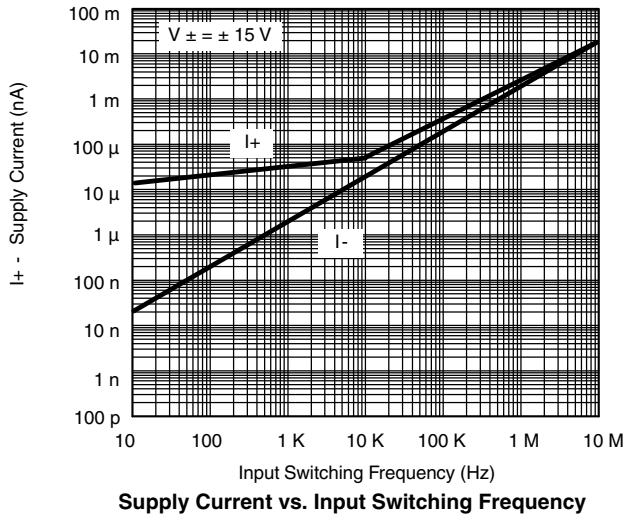


**Leakage vs. Analog Voltage**

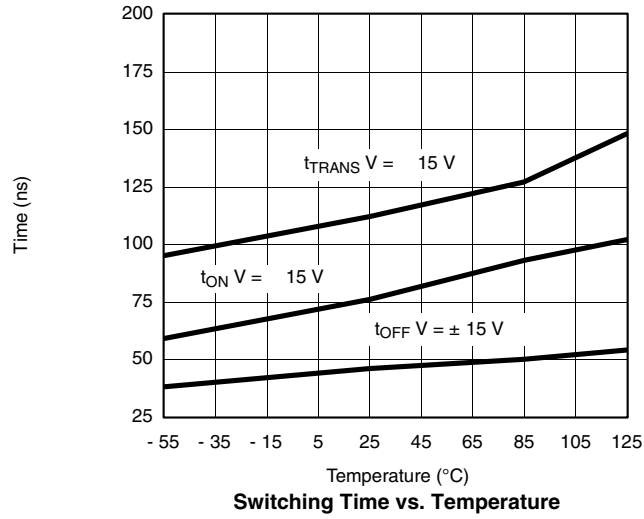


**Leakage vs. Current**

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)



**TYPICAL CHARACTERISTICS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**SCHEMATIC DIAGRAM** (Typical Channel)

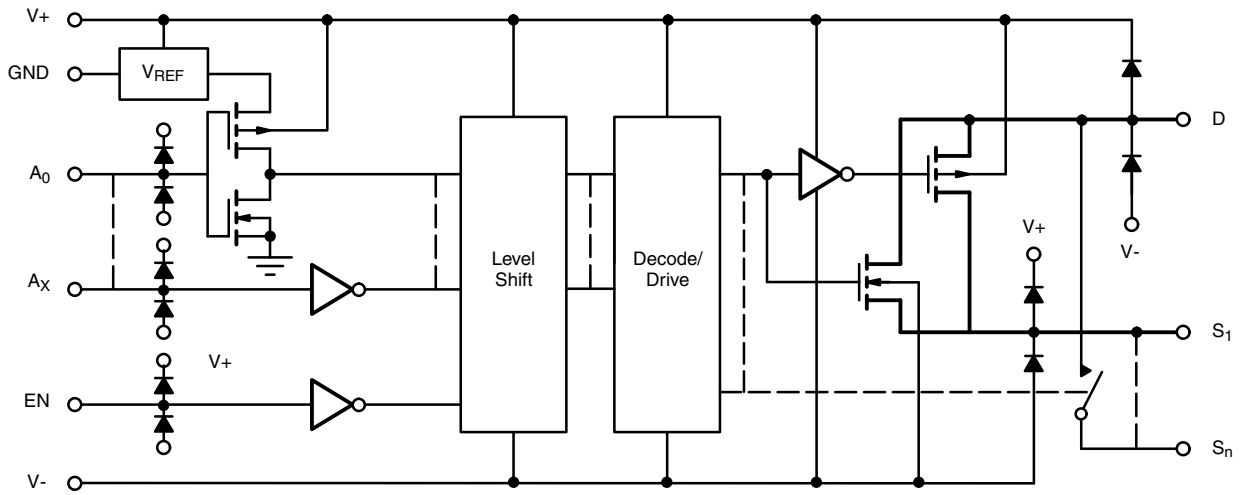
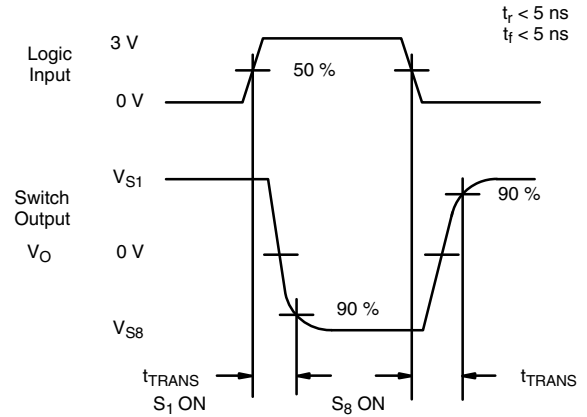
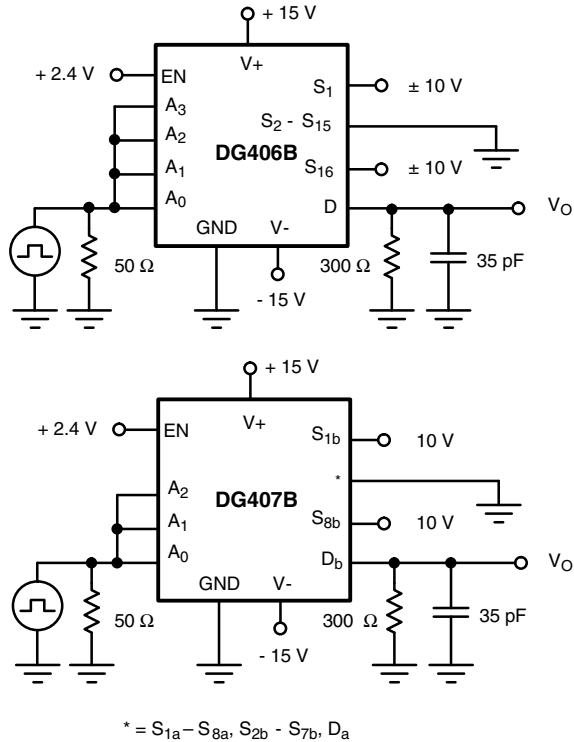


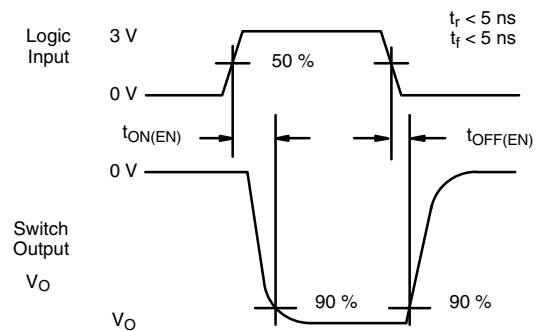
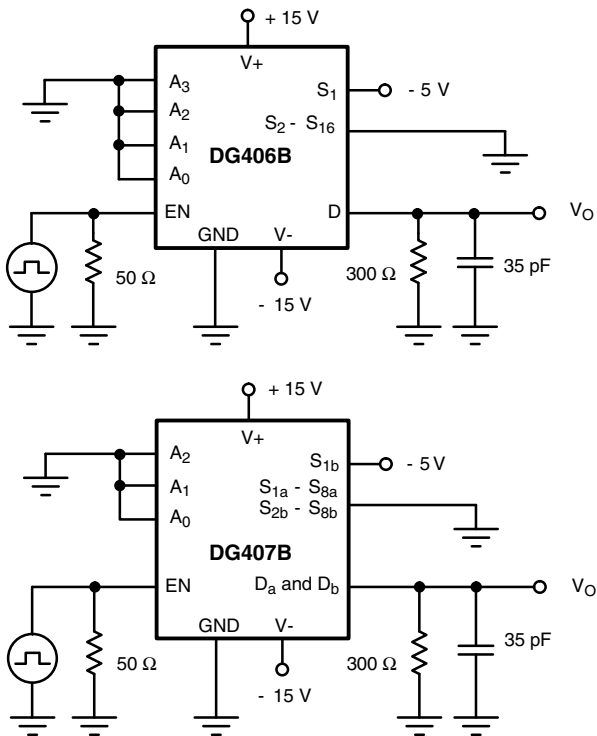
Figure 1.



**TEST CIRCUITS**



**Figure 2. Transition Time**



**Figure 3. Enable Switching Time**

## TEST CIRCUITS

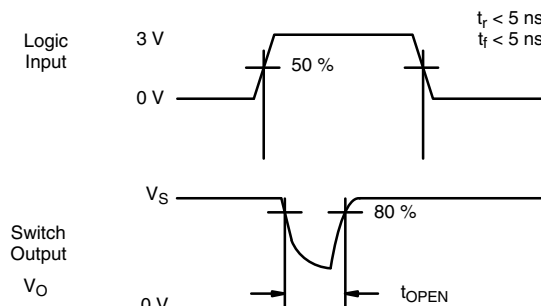
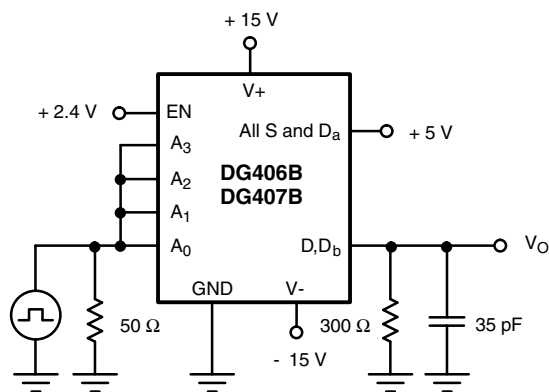


Figure 4. Break-Before-Make Interval

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?72552](http://www.vishay.com/ppg?72552).

### PDIP: 28-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	2.29	5.08	0.090	0.200
<b>A<sub>1</sub></b>	0.39	1.77	0.015	0.070
<b>B</b>	0.38	0.56	0.015	0.022
<b>B<sub>1</sub></b>	0.89	1.65	0.035	0.065
<b>C</b>	0.204	0.30	0.008	0.012
<b>D</b>	35.10	39.70	1.380	1.565
<b>E</b>	15.24	15.88	0.600	0.625
<b>E<sub>1</sub></b>	13.21	14.73	0.520	0.580
<b>e<sub>1</sub></b>	2.29	2.79	0.090	0.110
<b>e<sub>A</sub></b>	14.99	15.49	0.590	0.610
<b>L</b>	2.60	5.08	0.100	0.200
<b>Q<sub>1</sub></b>	0.95	2.345	0.0375	0.0925
<b>S</b>	0.995	2.665	0.0375	0.105

ECN: S-03946—Rev. F, 09-Jul-01  
DWG: 5488

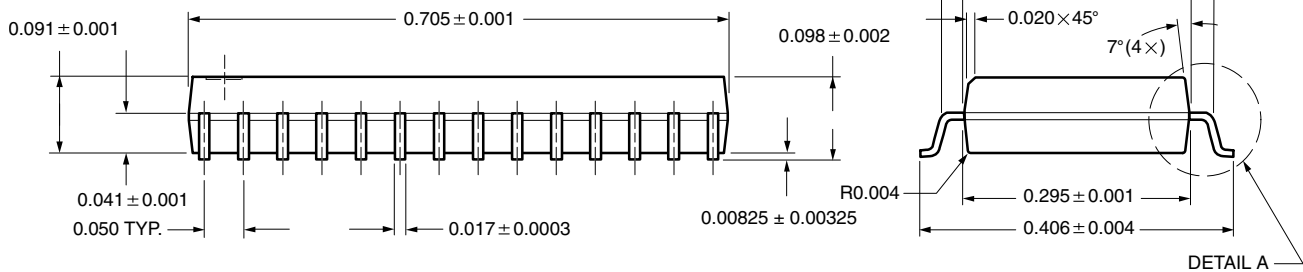
## PLCC: 28-LEAD



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.20	4.57	0.165	0.180
A <sub>1</sub>	2.29	3.04	0.090	0.120
A <sub>2</sub>	0.51	-	0.020	-
B	0.331	0.553	0.013	0.021
B <sub>1</sub>	0.661	0.812	0.026	0.032
D	12.32	12.57	0.485	0.495
D <sub>1</sub>	11.430	11.582	0.450	0.456
D <sub>2</sub>	9.91	10.92	0.390	0.430
e <sub>1</sub>	1.27 BSC		0.050 BSC	
ECN: T09-0766-Rev. D, 28-Sep-09 DWG: 5491				



### SOIC (WIDE-BODY): 28-LEADS



All Dimensions In Inches

ECN: E11-2209-Rev. D, 01-Aug-11  
DWG: 5850



28-LEAD LCC



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	1.37	2.24	0.054	0.088
<b>A<sub>1</sub></b>	1.63	2.54	0.064	0.100
<b>B</b>	0.56	0.71	0.022	0.028
<b>D</b>	11.23	11.63	0.442	0.458
<b>E</b>	11.23	11.63	0.442	0.458
<b>e</b>	1.27 BSC		0.050 BSC	
<b>L</b>	1.14	1.40	0.045	0.055
<b>L<sub>1</sub></b>	1.96	2.36	0.077	0.093

ECN: S-03946—Rev. B, 09-Jul-01  
DWG: 5319

### CERDIP: 28-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
<b>A</b>	4.06	5.92	0.160	0.232
<b>A<sub>1</sub></b>	0.38	1.52	0.015	0.060
<b>B</b>	0.38	0.51	0.015	0.020
<b>B<sub>1</sub></b>	1.14	1.65	0.045	0.065
<b>C</b>	0.20	0.30	0.008	0.012
<b>D</b>	36.58	37.08	1.440	1.460
<b>E</b>	15.24	15.88	0.600	0.625
<b>E<sub>1</sub></b>	12.95	13.46	0.510	0.530
<b>e<sub>1</sub></b>	2.54 BSC		0.100 BSC	
<b>e<sub>A</sub></b>	15.24 BSC		0.600 BSC	
<b>L</b>	3.18	3.81	0.125	0.150
<b>L<sub>1</sub></b>	3.81	5.08	0.150	0.200
<b>Q<sub>1</sub></b>	1.27	2.16	0.050	0.085
<b>S</b>	1.52	2.29	0.060	0.090
$\infty$	0°	15°	0°	15°
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5434				



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