

RoHS

HALOGEN

FREE

Precision Monolithic Quad SPST CMOS Analog Switches

DESCRIPTION

The DG411 series of monolithic guad analog switches was designed to provide high speed, low error switching of precision analog signals. Combining low power (0.35 µW) with high speed (t_{ON}: 110 ns), the DG411 family is ideally suited for portable and battery powered industrial and military applications.

To achieve high-voltage ratings and superior switching performance, the DG411 series was built on Vishay Siliconix's high voltage silicon gate process. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks input voltages up to the supply levels when off.

The DG411, DG412 respond to opposite control logic as shown in the Truth Table. The DG413 has two normally open and two normally closed switches.

FEATURES

- Halogen-free according to IEC 61249-2-21 **Definition**
- 44 V supply max. rating
- ± 15 V analog signal range
- On-resistance $R_{DS(on)}$: 25 Ω
- Fast switching t_{ON}: 110 ns
- Ultra low power P_D: 0.35 μW
- TTL, CMOS compatible
- Single supply capability
- Compliant to RoHS Directive 2002/95/EC

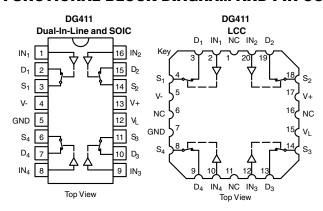
BENEFITS

- Widest dynamic range
- Low signal errors and distortion
- Break-bevor-make switching action
- Simple interfacing

APPLICATIONS

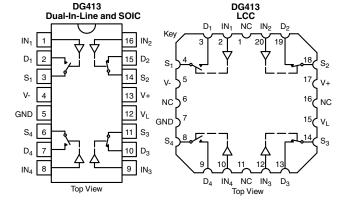
- Precision automatic test equipment
- Precision data acquisition
- Communication systems
- Battery powered systems
- Computer peripherals

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE					
Logic	DG411	DG412			
0	ON	OFF			
1	OFF	ON			

Logic "0" ≤ 0.8 V Logic "1" ≥ 2.4 V



TRUTH TABLE					
Logic	SW ₁ , SW ₄	SW ₂ , SW ₃			
0	OFF	ON			
1	ON	OFF			

Logic "0" ≤ 0.8 V Logic "1" ≥ 2.4 V

Document Number: 70050 S11-1185-Rev. G, 13-Jun-11



ORDERING INFORMATION				
Temp. Range	Package	Part Number		
		DG411DJ DG411DJ-E3		
	16-pin plastic DIP	DG412DJ DG412DJ-E3		
		DG413DJ DG413DJ-E3		
- 40 °C to 85 °C		DG411DY DG411DY-E3 DG411DY-T1 DG411DY-T1-E3		
	16-pin narrow SOIC	DG412DY DG412DY-E3 DG412DY-T1 DG412DY-T1-E3		
		DG413DY DG413DY-E3 DG413DY-T1 DG413DY-T1-E3		
		DG411DQ-E3 DG411DQ-T1-E3		
	16-pin TSSOP	DG412DQ-E3 DG412DQ-T1-E3		
		DG413DQ-E3 DG413DQ-T1-E3		

ABSOLUTE MAXIMUM RATINGS					
Parameter		Limit	Unit		
V + to V -		44			
GND to V -		25			
V _L		(GND - 0.3) to (V+) + 0.3	V		
Digital Inputs ^a , V _S , V _D		(V-) -2 to (V+) + 2 or 30 mA, whichever occurs first			
Continuous Current (Any terminal)		30	m A		
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle)		100	– mA		
Storage Temperature	(AK, AZ suffix)	- 65 to 150	°C		
Storage remperature	(DJ, DY suffix)	- 65 to 125]		
	16-pin plastic DIP ^c	470			
Device Discipation (Devices)h	16-pin narrow SOIC ^d	600	mW		
Power Dissipation (Package) ^b	16-pin CerDIP ^e	900	11100		
	LCC-20 ^e	900			

Notes:

- a. Signals on S_X , D_X , or IN_X exceeding V + or V will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC board.
- c. Derate 6 mW/°C above 25 °C.
- d. Derate 7.6 mW/°C above 75 °C.
- e. Derate 12 mW/°C above 75 °C.



SPECIFICATIONS)	T . A . IIII				***		***	1
		Test Conditions Unless Specified			A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		
		V + = 15 V, V - = - 15 V				120 0			
Parameter	Symbol	$V_L = 5 \text{ V}, V_{IN} = 2.4 \text{ V}, 0.8 \text{ V}^f$	Temp.b	Typ. ^c	Min. ^d	Max. ^d	Min. ^d	Max. ^d	Unit
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full		- 15	15	- 15	15	V
Drain-Source On-Resistance	R _{DS(on)}	V += 13.5 V, V -= -13.5 V $I_S = -10 \text{ mA}, V_D = \pm 8.5 \text{ V}$	Room Full	25		35 45		35 45	Ω
Switch Off Leakage	I _{S(off)}	V + = 16.5, V - = - 16.5 V	Room Full	± 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	
Current	I _{D(off)}	$V_D = \pm 15.5 \text{ V}, V_S = \pm 15.5 \text{ V}$	Room Full	± 0.1	- 0.25 - 20	0.25 20	- 0.25 - 5	0.25 5	nA
Channel On Leakage Current	I _{D(on)}	V + = 16.5 V, V - = -16.5 V $V_S = V_D = \pm 15.5 \text{ V}$	Room Full	± 0.1	- 0.4 - 40	0.4 40	- 0.4 - 10	0.4 10	
Digital Control									
Input Current, V _{IN} Low	Ι _{ΙL}	V _{IN} under test = 0.8 V	Full	0.005	- 0.5	0.5	- 0.5	0.5	μΑ
Input Current, V _{IN} High	I _{IH}	V_{IN} under test = 2.4 V	Full	0.005	- 0.5	0.5	- 0.5	0.5	μΛ
Dynamic Characteristics	5								
Turn-On Time	t _{ON}	$R_L = 300 \ \Omega, \ C_L = 35 \ pF$	Room Full	110		175 240		175 220	
Turn-Off Time	t _{OFF}	$V_S = \pm 10 \text{ V}$, see figure 2	Room Full	100		145 160		145 160	ns
Break-Before-Make Time Delay	t _D	DG413 only, $V_S = 10 \text{ V}$ R _L = 300 Ω, C _L = 35 pF	Room	25					
Charge Injection	q	$V_g = 0 \text{ V, } R_g = 0 \Omega$ $C_L = 10 \text{ nF}$	Room	5					рС
Off Isolation ^e	OIRR	$R_1 = 50 \Omega$, $C_1 = 5 pF$,	Room	68					
Channel-to-Channel Crosstalk ^e	X _{TALK}	f = 1 MHz	Room	85					dB
Source Off Capacitance ^e	C _{S(off)}		Room	9					
Drain Off Capacitance ^e	C _{D(off)}	f = 1 MHz	Room	9					pF
Channel On Capacitance ^e	C _{D(on)}	1 – 1 WH2	Room	35					Pi
Power Supplies	<u> </u>						I.	I.	
Positive Supply Current	l+		Room Full	0.0001		1 5		1 5	
Negative Supply Current	l-	V + = 16.5 V, V - = - 16.5 V	Room Full	- 0.0001	- 1 - 5		- 1 - 5		μΑ
Logic Supply Current	ΙL	$V_{IN} = 0 V \text{ or } 5 V$	Room Full	0.0001		1 5		1 5	μΑ
Ground Current	I _{GND}		Room Full	- 0.0001	- 1 - 5		- 1 - 5		



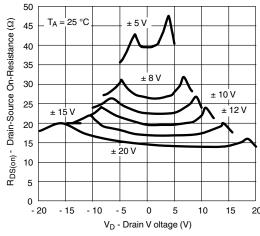
SPECIFICATIONS ^a (for Unipolar Supplies)									
Parameter	Symbol	Test Conditions Unless Specified	Temp. ^b Typ. ^c	A Suffix - 55 °C to 125 °C		D Suffix - 40 °C to 85 °C		Unit	
rarameter	Cymbol	V += 12 V, V -= 0 V $V_L = 5 V, V_{IN} = 2.4 V, 0.8 V^f$	Temp.	Typ.	Min. ^d	Max. ^d	Min. ^d	Max. ^d	
Analog Switch									
Analog Signal Range ^e	V_{ANALOG}		Full			12		12	٧
Drain-Source On-Resistance	R _{DS(on)}	V += 10.8 V, $I_S = -10 \text{ mA}, V_D = 3 \text{ V}, 8 \text{ V}$	Room Full	40		80 100		80 100	Ω
Dynamic Characteristics									
Turn-On Time	t _{ON}	$R_L = 300 \ \Omega, \ C_L = 35 \ pF$	Room Hot	175		250 400		250 315	
Turn-Off Time	t _{OFF}	$V_S = 8 V$, see figure 2	Room Hot	95		125 140		125 140	ns
Break-Before-Make Time Delay	t _D	DG413 only, $V_S = 8 V$ $R_L = 300 Ω$, $C_L = 35 pF$	Room	25					
Charge Injection	Q	$V_g = 6 \text{ V}, R_g = 0 \Omega, C_L = 10 \text{ nF}$	Room	25					рС
Power Supplies									
Positive Supply Current	l+		Room Hot	0.0001		1 5		1 5	
Negative Supply Current	l-	V . 12 E V V . 0 V oz E V	Room Hot	- 0.0001	- 1 - 5		- 1 - 5		
Logic Supply Current	ΙL	$V + = 13.5 \text{ V}, V_{IN} = 0 \text{ V or } 5 \text{ V}$	Room Hot	0.0001		1 5		1 5	μΑ
Ground Current	I _{GND}		Room Hot	- 0.0001	- 1 - 5		- 5		

Notes:

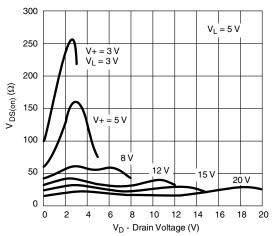
- a. Refer to process option flowchart.
- b.Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e.Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



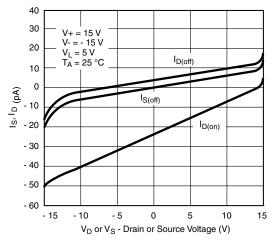
On-Resistance vs. V_D and Power Supply Voltage



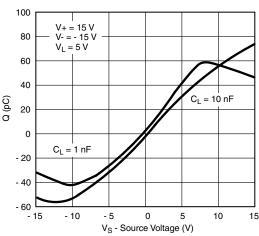
On-Resistance vs. V_D and Unipolar Supply Voltage



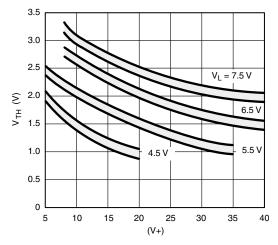
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



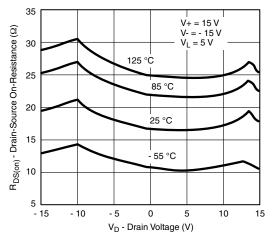
Leakage Current vs. Analog Voltage



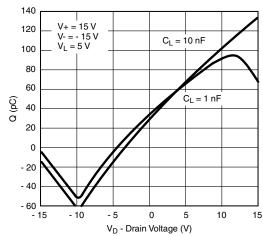
Charge Injection vs. Analog Voltage



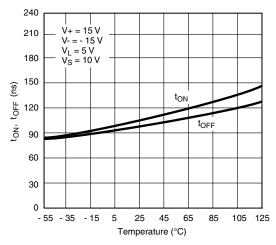
Input Switching Threshold vs. Supply Voltage



I_D, I_S Leakages vs. Temperature

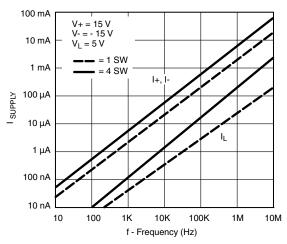


Charge Injection vs. Analog Voltage



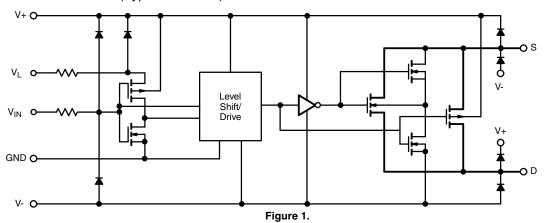
Switching Time vs. Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Supply Current vs. Input Switching Frequency

SCHEMATIC DIAGRAM (Typical Channel)



TEST CIRCUITS

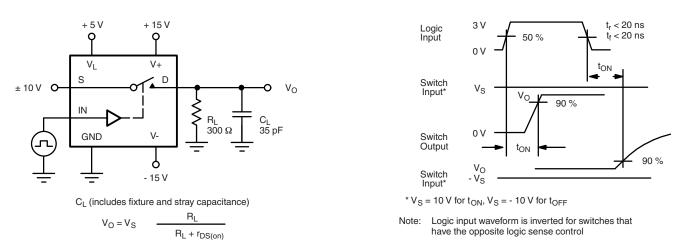
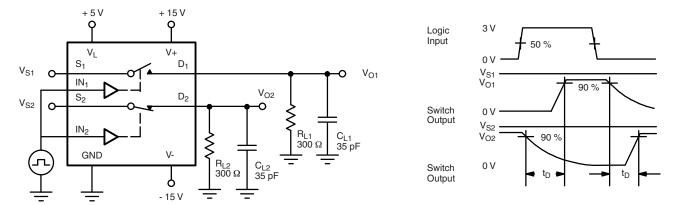


Figure 2. Switching Time



TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Figure 3. Break-Before-Make (DG413)

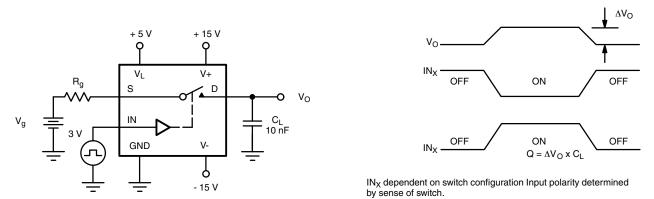


Figure 4. Charge Injection

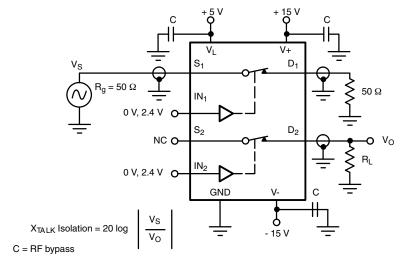


Figure 5. Crosstalk



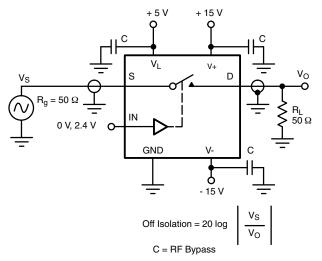


Figure 6. Off Isolation

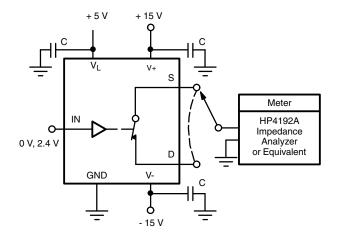


Figure 7. Source/Drain Capacitances

APPLICATIONS

Single Supply Operation:

The DG411, DG412, DG413 can be operated with unipolar supplies from 5 V to 44 V. These devices are characterized and tested for unipolar supply operation at 12 V to facilitate the majority of applications. In single supply operation, V+ is tied to V_L and V_T is tied to 0 V_T . See Input Switching Threshold vs. Supply Voltage curve for V_I versus input threshold requirments.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in figure 8, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

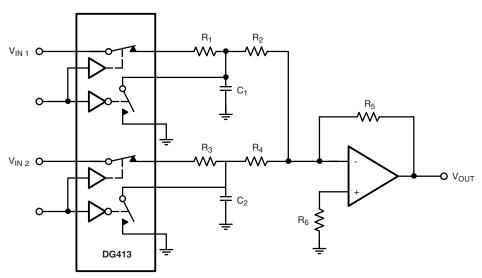


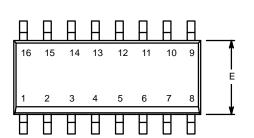
Figure 8. Summing Amplifier

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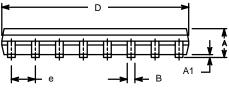
SOIC (NARROW): 16-LEAD JEDEC Part Number: MS-012

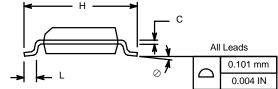


	MILLIMETERS		INC	HES	
Dim	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.38	0.51	0.015	0.020	
С	0.18	0.23	0.007	0.009	
D	9.80	10.00	0.385	0.393	
E	3.80	4.00	0.149	0.157	
е	e 1.27 BSC			BSC	
Н	5.80	6.20	0.228	0.244	
L	0.50	0.93	0.020	0.037	
0	0°	8°	0°	8°	
FCN: S-03946—Rev. F. 09-Jul-01					

ECN: S-03946—Rev. F, 09-Jul-01

DWG: 5300

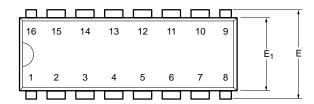


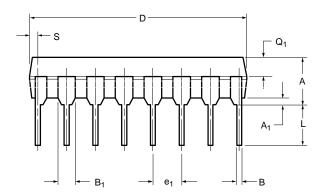


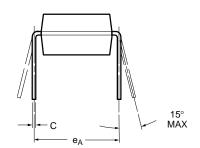
www.vishay.com 02-Jul-01



PDIP: 16-LEAD





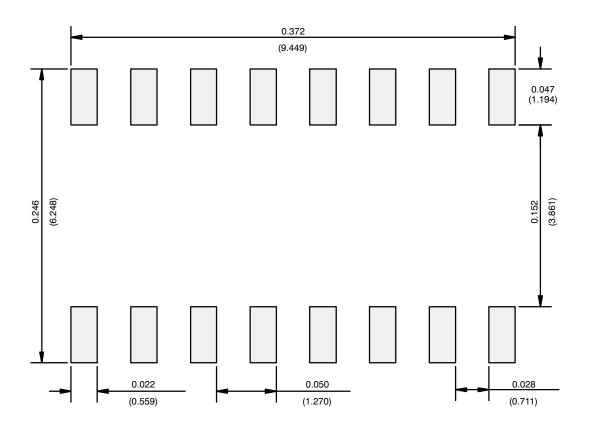


	MILLIN	IETERS	INC	HES		
Dim	Min	Max	Min	Max		
Α	3.81	5.08	0.150	0.200		
A ₁	0.38	1.27	0.015	0.050		
В	0.38	0.51	0.015	0.020		
B ₁	0.89	1.65	0.035	0.065		
С	0.20	0.30	0.008	0.012		
D	18.93	21.33	0.745	0.840		
E	7.62	8.26	0.300	0.325		
E ₁	5.59	7.11	0.220	0.280		
e ₁	2.29	2.79	0.090	0.110		
e _A	7.37	7.87	0.290	0.310		
L	2.79	3.81	0.110	0.150		
Q ₁	1.27	2.03	0.050	0.080		
S	0.38	1.52	.015	0.060		
	ECN: S-03946—Rev. D, 09-Jul-01 DWG: 5482					

Document Number: 71261 www.vishay.com 06-Jul-01 www.vishay.com



RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads Dimensions in Inches/(mm)

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PI5A4157ZUEX PI5A3166TAEX FSA634UCX TC4066BP(N,F) DG302BDJ-E3 PI5A100QEX HV2605FG-G HV2301FG-G
RS2117YUTQK10 RS2118YUTQK10 RS2227XUTQK10 ADG452BRZ-REEL7 MAX4066ESD+ MAX391CPE+ MAX4730EXT+T
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NLAST4599DTT1G DG300BDJ-E3 DG2503DB-T2-GE1 TC4W53FU(TE12L,F) 74HC2G66DC.125 ADG619BRMZ-REEL DG2535EDQT1-GE3 LTC201ACN#PBF 74LV4066DB,118 FSA2275AUMX DIO1500WL12 ADG742BKSZ-REEL7 DIO1269LP10