

COMPLIANT

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Low Power, High Voltage SPST Analog Switches

DESCRIPTION

The DG467 and DG468 are dual supply single-pole/single-throw (SPST) switches. On resistance is 10 Ω max. and flatness is 2 Ω max. over the specified analog signal range. These analog switches were designed to provide high speed, low error switching of precision analog signals. The primary application areas are in the routing and switching in telecommunications and test equipment. Combining low power, low leakages, low on-resistance and small physical size, the DG467/468 are also ideally suited for portable and battery powered industrial and military equipment.

The DG467 has one normally closed switch, while the DG468 switch is normally open. They operate either from a single + 7 V to 36 V supply or from dual \pm 4.5 V to \pm 20 V supplies. They are offered in the very popular, small TSOP6 package.

FEATURES

- ± 15 V Analog Signal Range
- On-Resistance $R_{DS(on)}$: 10 Ω max.
- Fast Switching Action Ton: 100 ns
- V_L Logic Supply Not Required
- TTL CMOS Input Compatible
- Rail To Rail Signal Handling
- Dual Or Single Supply Operation
- Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

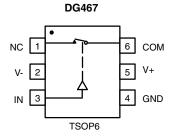


- Wide Dynamic Range
- · Low Signal Errors and Distortion
- Break-Befor-Make Switching Action
- Simple Interfacing
- Reduced Board Space
- Improved Reliability

APPLICATIONS

- · Precision Test Equipment
- Precision Instrumentaion
- Communications Systems
- PBX, PABX Systems
- · Audio Equipment
- Redundant Systems
- PC Multimedia Boards
- Hard Disc Drivers

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



NO 1		6 COM
V- 2 IN 3		5 V+ 4 GND
	TSOP6	

DG468

TRUTH TABLE							
Logic	DG467	DG468					
0	ON	OFF					
1	OFF	ON					

Logic "0" \leq 0.8 V Logic "1" \geq 2.4 V

Device Marking: DG467DV = G7xxx DG468DV = G8xxx

Document Number: 74413 S12-2269–Rev. D, 24-Sep-12



ORDERING INFORMATION							
Temp Range Package Part Number							
DG467/DG468							
- 40 °C to 85 °C	6-Pin TSOP	DG467DV-T1-E3					
- 40 C 10 65 C	0-FIII 190F	DG468DV-T1-E3					

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter Referenced To V-		Symbol	Limit	Unit		
V+			44			
GND			25			
Digital Inputs ^a , V _{NO/NC} , V _{COM}			(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first	V		
Current, (Any Terminal) Continuous			30	mA		
Current (NO or NC or COM) Pulsed at 1 ms, 10 % dut		100	ША			
Storage Temperature			- 65 to 150	°C		
Power Dissipation (Package) ^b	6-Pin TSOP ^c		570	mW		

Notes:

- a. Signals on NO, NC, COM, or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads welded or soldered to PC Board.
- c. Derate 7 mW/°C above 70 °C.



		Test Conditions Unless Otherwise Specified		D Suffix - 40 °C to 85 °C			
Davamatav	Symbol	V+ = 15 V, V- = -15 V $V_{IN} = 2.4 V, 0.8 V^f$	Temp.b	Min. ^d	Typ. ^c	Max. ^d	l lmit
Parameter Analog Switch	Symbol	V N - 2.4 V, 0.0 V	remp."	win.	Typ.	wax.	Unit
Analog Signal Range ^{eron}	V _{ANALOG}		Full	- 15		15	V
Drain-Source On-Resistance	R _{ON}	I _{NO/NC} = 10 mA, V _{COM} = 10 V V+ = 13.5 V, V- = - 13.5 V	Room	- 10	7	9	
On-Resistance Flatness	R _{ON} Flatness	$I_{NO/NC} = 10 \text{ mA}, V_{COM} = \pm 5 \text{ V}, 0 \text{ V}$ V+ = 13.5 V, V- = -13.5 V	Room Full		0.7	1 2	Ω
Switch Off Leakage Current	I _{NO/NC(off)}	V+ = 16.5, V- = - 16.5 V V _{COM} = ± 15.5 V	Room Full	- 1 - 10	- 0.1	1 10	
	I _{COM(off)}	$V_{NO/NC} = -/+ 15.5 V$	Room Full	- 1 - 10	- 0.1	1 10	nA
Channel On Leakage Current	I _{COM(on)}	V+ = 16.5 V, V- = -16.5 $V_{COM} = V_{NO/NC} = \pm 15.5 \text{ V}$	Room Full	- 1 - 10	- 0.1	1 10	
Digital Control							
Input, High Voltage	V _{INH}		Full	2.4			.,
Input, Low Voltage	V _{INL}		Full			0.8	V
Input Capacitance ^e	C _{IN}		Room		5		pF
Input Current	I _{IN}	V _{IN} = 0 or 5 V		- 1		1	μΑ
Dynamic Characteristics							
Turn-On Time	t _{ON}	R _I = 300 Ω, C _I = 35 pF	Room Full		100	140 160	ns
Turn-Off Time	t _{OFF}	$V_{NO/NC} = \pm 10 \text{ V}$	Room Full		50	80 100	113
Charge Injection ^e	Q	$C_L = 1 \text{ nF, } V_{gen} = 0 \text{ V, } R_{gen} = 0 \Omega$	Room		21		рC
Off-Isolation ^e	OIRR	C_L = 5 pF, R_L = 50 Ω , f = 1 MHz	Room		- 61		dB
Source Off Capacitance ^e	C _{S(off)}	f = 1 MHz	Room		30		
Drain Off Capacitance ^e	C _{D(off)}	I = I IVIDZ	Room		15		pF
Channel On Capacitance ^e	C _{D(on)}	f = 1 MHz	Room		76		
Power Supplies							
Positive Supply Current	l+	V+ = 16.5 V, V- = - 16.5 V	Room Full		5	15 20	μΑ
Negative Supply Current	I-	$V_{IN} = 0 \text{ or } 5 \text{ V}$	Room Full	- 1 - 10	- 0.02		μ,



SPECIFICATIONS ^a (V+ = 12 V)								
		Test Conditions Unless Otherwise Specified		- 4	D Suffix - 40 °C to 85 °C			
Parameter	Symbol	V+ = 12 V, V- = 0 V $V_{IN} = 2.4 \text{ V}, 0.8 \text{ V}^{f}$	V+ = 12 V, V- = 0 V $V_{\text{IN}} = 2.4 \text{ V}, 0.8 \text{ V}^{\text{f}}$ Temp. ^b		Typ. ^c	Max. ^d	Unit	
Analog Switch								
Analog Signal Range ^e	V _{ANALOG}		Full	0		12	V	
Drain-Source On-Resistance	R _{ON}	$I_{NO/NC} = -10 \text{ mA}, V_{COM} = 8 \text{ V}$ V+ = 10.8 V	Room Full		12	16 20	Ω	
On-Resistance Flatness	R _{ON} Flatness	$I_{NO/NC}$ = 10 mA, V_{COM} = 2, 6, 8 V V+ = 10.8 V	Room Full		1.5	3 4	Ω	
Dynamic Characteristics	Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO. NC} = ± 10 V, R _L = 300 Ω, C _L = 35 pF	Room Full		130	160 200	nS	
Turn-Off Time	t _{OFF}	NO, NC - 10 V, 11 - 300 S2, OL - 33 PI	Room Full		50	80 100	110	
Charge Injection ^e	Q	$C_L = 1 \text{ nF, } V_{gen} = 0 \text{ V, } R_{gen} = 0 \Omega$	Room		8		рC	
Power Supplies								
Positive Supply Current	l+	V+ = 13.2 V, V _{IN} = 0 V, 5 V	Room Full		3	7 10	μΑ	

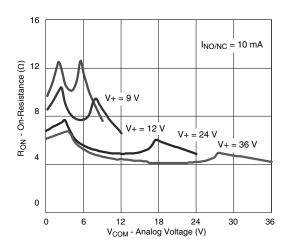
Notes:

- a. Refer to PROCESS OPTION FLOWCHART.
- b. Room = 25 $^{\circ}$ C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.

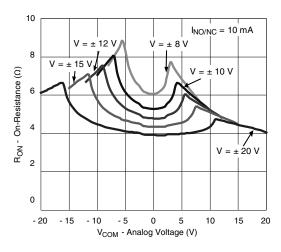
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



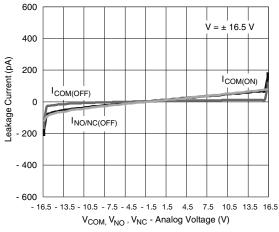
TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



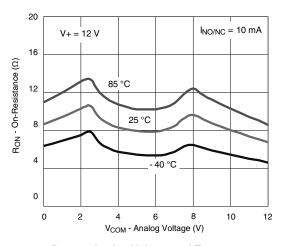
 $\rm R_{ON}$ vs. $\rm V_{COM}$ and Single Supply Voltage



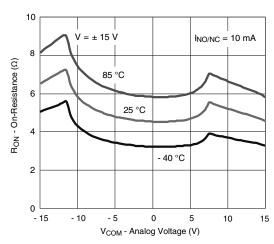
 R_{ON} vs. V_{COM} and Dual Supply Voltage



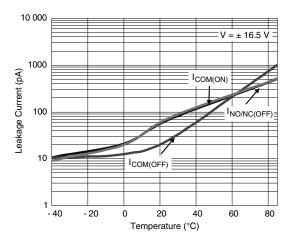
Leakage vs. Analog Voltage



R_{ON} vs. Analog Voltage and Temperature



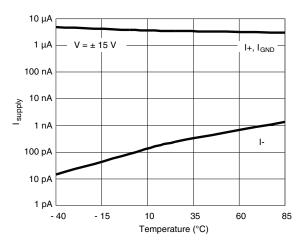
 $\ensuremath{\text{R}_{\text{ON}}}$ vs. Analog Voltage and Temperature



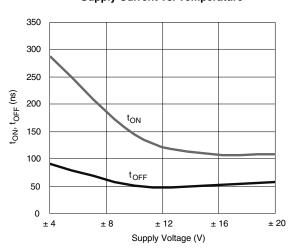
Leakage Current vs. Temperature

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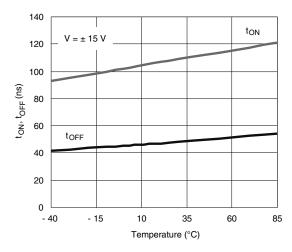
TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



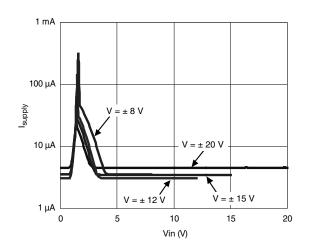
Supply Current vs. Temperature



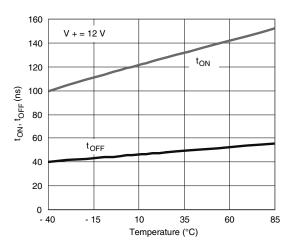
Switching Time vs. Supply Voltages



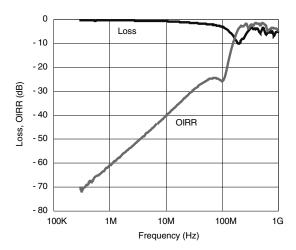
Switching Time vs. Temperature



Supply Current vs. $V_{\rm IN}$



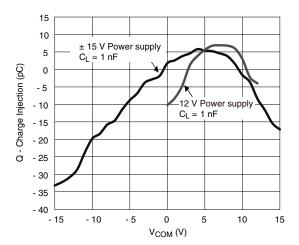
Switching Time vs. Temperature



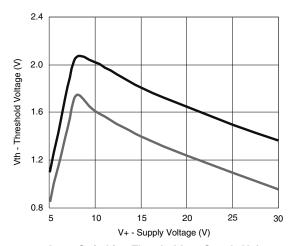
Off Isolation and Insertion Loss vs. Frequency



TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



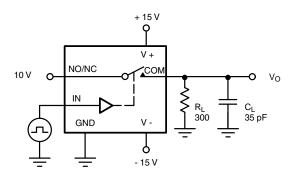
Charge Injection vs. Analog Voltage



Input Switching Threshold vs. Supply Voltage

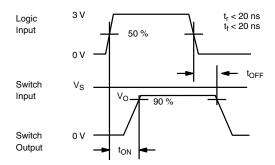
TEST CIRCUITS

V_O is the steady state output with the switch on.



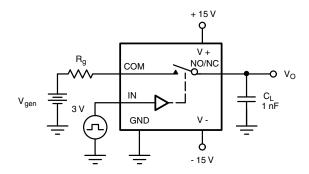
C_L (includes fixture and stray capacitance)

$$V_O = V_S$$
 $\frac{R_L}{R_L + r_{ON}}$



Note: Logic input waveform is inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



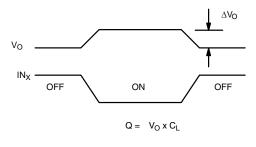


Figure 2. Charge Injection

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TEST CIRCUITS

V_O is the steady state output with the switch on.

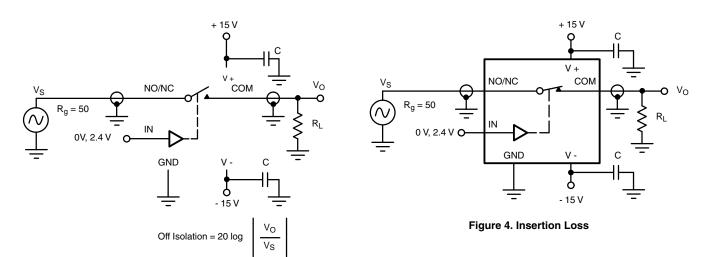


Figure 3. Off Isolation

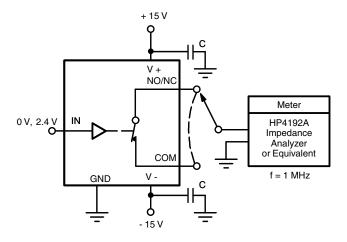


Figure 5. Source/Drain Capacitances

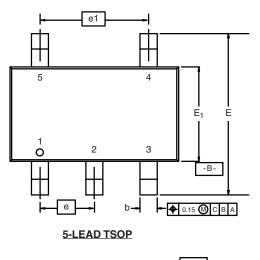
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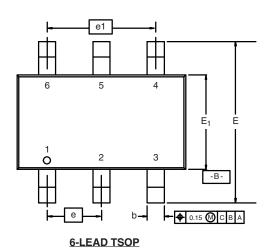




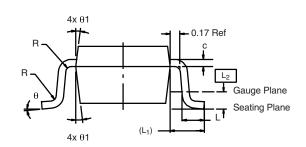
TSOP: 5/6-LEAD

JEDEC Part Number: MO-193C





-A-D · A_2 Seating Plane **a** 0.08 C -C- A₁

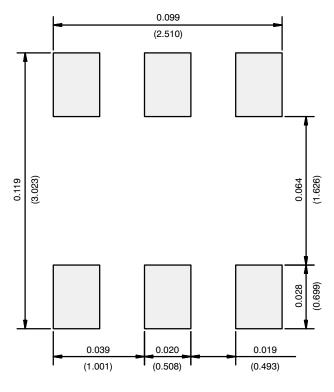


	MIL	LIMETER	RS	INCHES			
Dim	Min	Nom	Max	Min	Nom	Max	
Α	0.91	-	1.10	0.036	-	0.043	
A ₁	0.01	-	0.10	0.0004	-	0.004	
A ₂	0.90	-	1.00	0.035	0.038	0.039	
b	0.30	0.32	0.45	0.012	0.013	0.018	
С	0.10	0.15	0.20	0.004	0.006	0.008	
D	2.95	3.05	3.10	0.116	0.120	0.122	
Е	2.70	2.85	2.98	0.106	0.112	0.117	
E ₁	1.55	1.65	1.70	0.061	0.065	0.067	
е		0.95 BSC			0.0374 BSC	;	
e ₁	1.80	1.90	2.00	0.071	0.075	0.079	
L	0.32	-	0.50	0.012	-	0.020	
L ₁		0.60 Ref			0.024 Ref		
L ₂	0.25 BSC			0.010 BSC			
R	0.10	-	-	0.004	-	-	
θ	0°	4°	8°	0°	4°	8°	
θ_1	7° Nom 7° Nom						
ECN: C DWG: 5		ev. I, 18-Dec	c-06				

Document Number: 71200 www.vishay.com 18-Dec-06

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RECOMMENDED MINIMUM PADS FOR TSOP-6



Recommended Minimum Pads Dimensions in Inches/(mm)

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PI5A4157ZUEX PI5A3166TAEX FSA634UCX TC4066BP(N,F) DG302BDJ-E3 PI5A100QEX HV2605FG-G HV2301FG-G
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