

Precision 16-Channel/Dual 8-Channel CMOS Analog Multiplexers

DESCRIPTION

The DG506B and DG507B are high performance analog multiplexers. Their ultra-low switch charge injection, low channel capacitance, and low leakage level allows them to achieve superior switching performance. The DG506B is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address (A0, A1, A2, A3). The DG507B is a dual 8-channel differential analog multiplexer designed to connect one of eight differential inputs to a common dual output as determined by its 3-bit binary address (A0, A1, A2). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, addresses (Ax) and enable (EN) are TTL compatible over the full specified operating temperature range.

The DG506B and DG507B are fabricated on an enhanced SG-II CMOS process that achieves improved performance on: reduced charge injection, lower device leakage, and minimized parasitic capacitance.

As the DG506, DG507 has a long history in the industry with many suppliers offering copies, and in some cases improved variations, with the best in class improvements, the Vishay Siliconix new version of the DG506B, DG507B are the superior alternatives to what is currently available.

Applications for the DG506B, DG507B include high speed and high precision data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

The DG506B and DG507B have the absolute maximum voltage rating extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latch-up.

The DG506B and DG507B are both available in 28-lead SOIC and TSSOP package options with extended temperature range of -40 °C to +125 °C.

For more information, refer to Vishay Siliconix DG506B, DG507B evaluation board note.

FEATURES

- Operate with single or dual power supply
- V+ to V- analog signal swing range
- 44 V power supply maximum rating
- Extended operate temperature range: -40 °C to +125 °C
- Low leakage typically < 3 pA
- Low charge injection - $Q_{INJ} = 1$ pC
- Low power - $I_{SUPPLY}: 5$ μ A
- TTL compatible logic
- > 250 mA latch up current per JESD78
- Available in SOIC28 and TSSOP28 packages
- Superior alternative to:
 - ADG506A, DG506A, HI-506
 - ADG507A, DG507A, HI-507
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

BENEFITS

- Reduced switching errors
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges (± 5 V to ± 20 V)

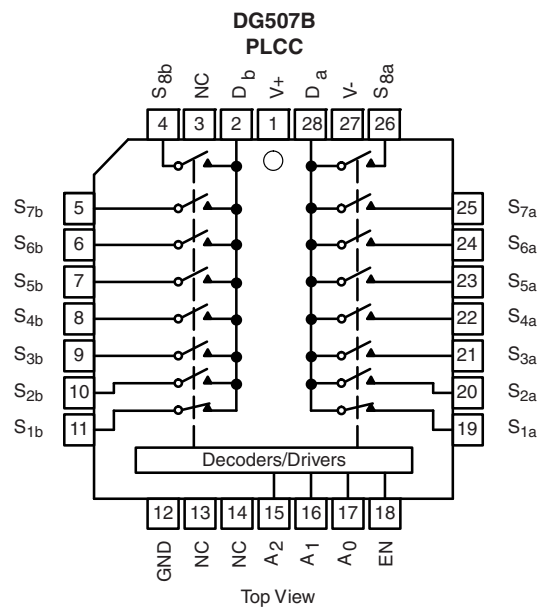
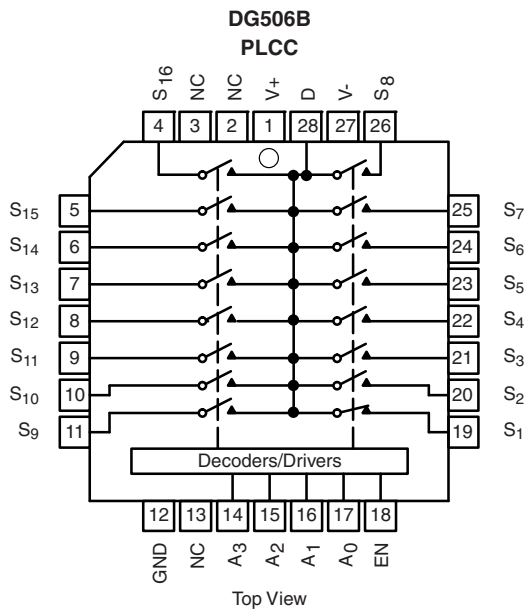
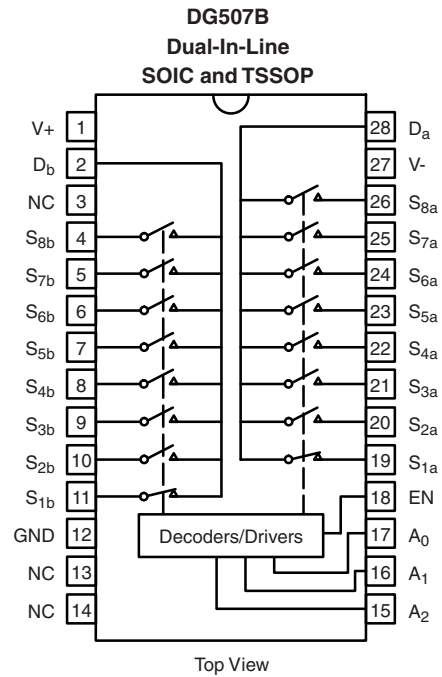
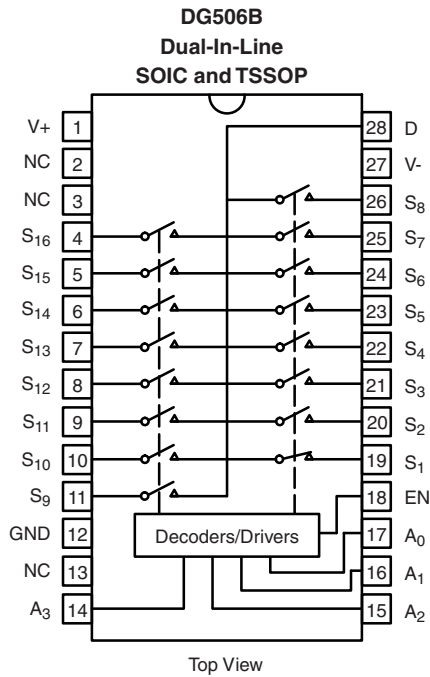
APPLICATIONS

- Data acquisition systems
- Audio and video signal routing
- ATE systems
- Medical instrumentation



RoHS
COMPLIANT
HALOGEN
FREE

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





TRUTH TABLE DG506B					
A ₃	A ₂	A ₁	A ₀	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
1	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

TRUTH TABLE DG507B				
A ₂	A ₁	A ₀	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V_{IL} ≤ 0.8 V
 Logic "1" = V_{IH} ≥ 2.4 V
 X = Do not care

ORDERING INFORMATION DG506B		
Temp. Range	Package	Part Number
-40 °C to 125 °C	28-Pin SOIC	DG506BEW-T1-GE3
	28-Pin TSSOP	DG506BEQ-T1-GE3
	28-Pin PLCC	DG506BEN-T1-GE3

ORDERING INFORMATION DG507B		
Temp. Range	Package	Part Number
-40 °C to 125 °C	28-Pin SOIC	DG507BEW-T1-GE3
	28-Pin TSSOP	DG507BEQ-T1-GE3
	28-Pin PLCC	DG507BEN-T1-GE3

ABSOLUTE MAXIMUM RATINGS			
Parameter		Limit	Unit
Voltages Referenced to V-	V+	44	V
	GND	25	
Digital Inputs ^a , V _S , V _D		(V-) - 2 to (V+) + 2 or 20 mA, whichever occurs first	
Current (Any terminal)		30	mA
Peak Current, S or D (Pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage Temperature	(EW, EQ, EN suffix)	-65 to 150	°C
Power Dissipation (Packages) ^b	28-Pin Wide Body SOIC ^c	840	mW
	28-Pin TSSOP ^d	817	
	28-Pin PLCC ^e	1693	
Thermal Resistance (θ _{J-A}) ^b	28-Pin Wide Body SOIC ^c	95.3	°C/W
	28-Pin TSSOP ^d	97.9	
	28-Pin PLCC ^e	47.3	

Notes:

- a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- b. All leads soldered or welded to PC board.
- c. Derate 10.5 mW/°C above 70 °C.
- d. Derate 10.2 mW/°C above 70 °C.
- e. Derate 21.2 mW/°C above 70 °C.

SPECIFICATIONS										
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ ($\pm 10\%$) V_{AX} , $V_{EN} = 2.4\text{ V}$, 0.8 V^a	Temp. ^b	Typ. ^c	A Suffix -40 °C to 125 °C		D Suffix -40 °C to 85 °C		Unit	
					Min. ^d	Max. ^d	Min. ^d	Max. ^d		
Analog Switch										
Analog Signal Range ^e	V_{ANALOG}		Full		-15	15	-15	15	V	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_D = \pm 10\text{ V}$, $I_S = -1\text{ mA}$	Room	170		300		300	Ω	
			Full			400		400		
$R_{DS(on)}$ Matching	$\Delta R_{DS(on)}$	$V_D = \pm 10\text{ V}$	Room	10						
Source Off Leakage Current	$I_{S(off)}$	$V_D = \pm 10\text{ V}$ $V_S = \mp 10\text{ V}$ $V_{EN} = 0\text{ V}$	Room	0.005	-1	1	-1	1	nA	
Drain Off Leakage Current	$I_{D(off)}$		DG506B	Room	0.005	-1	1	-1		1
			DG506B	Full		-100	100	-100		100
			DG507B	Room	0.005	-1	1	-1		1
		DG507B	Full		-50	50	-50	50		
Drain On Leakage Current	$I_{D(on)}$	$V_S = V_D = \mp 10\text{ V}$ sequence each switch on	DG506B	Room	0.005	-1	1	-1		1
			DG506B	Full		-100	100	-100		100
			DG507B	Room	0.005	-1	1	-1		1
			DG507B	Full		-50	50	-50	50	
Digital Control										
Logic High Input Voltage	V_{INH}		Full		2.4		2.4		V	
Logic Low Input Voltage	V_{INL}		Full			0.8		0.8		
Logic High Input Current	I_{IH}	V_{AX} , $V_{EN} = 2.4\text{ V}$	Full		-1	1	-1	1	μA	
Logic Low Input Current	I_{IL}	V_{AX} , $V_{EN} = 0.8\text{ V}$	Full		-1	1	-1	1		
Logic Input Capacitance ^e	C_{in}	$f = 1\text{ MHz}$	Room	5					pF	
Dynamic Characteristics										
Transition Time	t_{TRANS}	$V_{S1} = +10\text{ V}/-10\text{ V}$, $V_{S16} = -10\text{ V}/+10\text{ V}$, $R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$ see figure 2	Room	190		300		300	ns	
			Full			360		360		
Break-Before-Make Interval	t_{OPEN}	$V_{S1} = V_{S16} = 5.0\text{ V}$, $C_L = 35\text{ pF}$, $R_L = 1\text{ k}\Omega$, see figure 4	Room	84	30		30		ns	
			Full		10		10			
Enable Turn-On Time	$t_{ON(EN)}$	$V_{S1} = 5\text{ V}$, V_{S2} to $V_{S16} = 0\text{ V}$, $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ see figure 3	Room	151		250		250	ns	
			Full			310		310		
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	53		200		200		
			Full			220		220		
Charge Injection ^e	Q_{INJ}	$C_L = 1\text{ nF}$, $R_{GEN} = 0\ \Omega$, $V_{GEN} = 0\text{ V}$	Full	1					pC	
Off Isolation ^e	OIRR	$C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f = 1\text{ MHz}$	DG506B	Room	-85				dB	
			DG507B		-84					
Crosstalk ^e	XTALK	$C_L = 5\text{ pF}$, $R_L = 50\ \Omega$, $f = 1\text{ MHz}$	DG506B	Room	-85				dB	
			DG507B		-84					
-3 dB Bandwidth ^e	BW	$R_L = 50\ \Omega$	DG506B	Room	114				MHz	
			DG507B		217					
Total Harmonic Distortion ^e	THD	$R_L = 10\text{ k}\Omega$, 5 V_{rms}	Room	0.04					%	
Source Off Capacitance ^e	$C_{S(off)}$	$f = 1\text{ MHz}$	Room	3					pF	
Drain Off Capacitance ^e	$C_{D(off)}$		DG506B	Room	31					
			DG507B	Room	17					
Drain On Capacitance ^e	$C_{D(on)}$		DG506B	Room	38					
			DG507B	Room	24					
Power Supply										
Positive Supply Current	I_+	V_{AX} , $V_{EN} = 0\text{ V}$ or 5 V	Room	0.005		0.1		0.1	mA	
			Full			0.1		0.1		
Negative Supply Current	I_-		Full			-1		-1	μA	



SPECIFICATIONS Single Supply 12 V										
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ ($\pm 10\%$) V_{AX} , $V_{EN} = 2.4\text{ V}$, 0.8 V^a	Temp. ^b	Typ. ^c	A Suffix -40 °C to 125 °C		D Suffix -40 °C to 85 °C		Unit	
					Min. ^d	Max. ^d	Min. ^d	Max. ^d		
Analog Switch										
Analog Signal Range ^e	V_{ANALOG}		Full		0	12	0	12	V	
On-Resistance	$R_{DS(on)}$	$V_D = 10\text{ V}/0\text{ V}$, $I_S = 1\text{ mA}$	Room	270		450		450	Ω	
$R_{DS(on)}$ Matching	$\Delta R_{DS(on)}$		Full			650		650		
Switch Off Leakage Current	$I_{S(off)}$	$V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ $V_D = 0\text{ V}/10\text{ V}$, $V_S = 10\text{ V}/0\text{ V}$	Room	0.005	-1	1	-1	1	nA	
			Full		-50	-50	-50	50		
	$I_{D(off)}$		DG506B	Room	0.005	-1	1	-1		1
			Full			-100	100	-100		100
	$I_{D(off)}$		DG507B	Room	0.005	-1	1	-1		1
			Full			-50	50	-50		50
Channel On Leakage Current	$I_{D(on)}$	$V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ $V_S = V_D = 0\text{ V}/10\text{ V}$	DG506B	Room	0.005	-1	1	-1	1	
			Full			-100	100	-100	100	
			DG507B	Room	0.005	-1	1	-1	1	
			Full			-50	50	-50	50	
Digital Control										
Logic High Input Voltage	V_{INH}		Full		2.4		2.4		V	
Logic Low Input Voltage	V_{INL}		Full			0.8		0.8		
Logic High Input Current	I_{IH}	V_{AX} , $V_{EN} = 2.4\text{ V}$	Full		-1	1	-1	1	μA	
Logic Low Input Current	I_{IL}	V_{AX} , $V_{EN} = 0.8\text{ V}$	Full		-1	1	-1	1		
Logic Input Capacitance ^e	C_{in}	$f = 1\text{ MHz}$	Room	5					pF	
Dynamic Characteristics										
Transition Time	t_{TRANS}	$V_{S1} = 10\text{ V}/0\text{ V}$, $V_{S16} = 0\text{ V}/10\text{ V}$, $R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$, see figure 2	Room	228		380		380	ns	
			Full			450		450		
Break-Before-Make Interval	t_{OPEN}	$V_{S1} = V_{S16} = 5\text{ V}$, $C_L = 35\text{ pF}$, $R_L = 1\text{ k}\Omega$, see figure 4	Room	115	40		40			
			Full		10		10			
Enable Turn-On Time	$t_{ON(EN)}$	$V_{S1} = 5\text{ V}$, V_{S2} to $V_{S16} = 0\text{ V}$, $R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$ see figure 3	Room	197		300		300		
			Full			420		420		
Enable Turn-Off Time	$t_{OFF(EN)}$		Room	46		200		200		
			Full			220		220		
Charge Injection ^e	Q_{INJ}		$C_L = 1\text{ nF}$, $R_{GEN} = 0\ \Omega$, $V_{GEN} = 0\text{ V}$	Full	4				pC	
Off Isolation ^e	OIRR		$C_L = 5\text{ pF}$, $R_L = 50\ \Omega$ $f = 1\text{ MHz}$	DG506B	Room	-86				dB
		DG507B			-84					
Crosstalk ^e	X_{TALK}	$C_L = 5\text{ pF}$, $R_L = 50\ \Omega$ $f = 1\text{ MHz}$	DG506B	Room	-85					
			DG507B		-84					
- 3 dB Bandwidth ^e	BW	$R_L = 50\ \Omega$	DG506B	Room	104				MHz	
			DG507B		191					
Total Harmonic Distortion ^e	THD	$R_L = 10\text{ k}\Omega$, 5 V_{RMS} , $f = 20\text{ Hz}$ to 20 kHz	Room	0.23					%	

SPECIFICATIONS Single Supply 12 V											
Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ ($\pm 10\%$) V_{AX} , $V_{EN} = 2.4\text{ V}$, 0.8 V^a			Temp. ^b	Typ. ^c	A Suffix -40 °C to 125 °C		D Suffix -40 °C to 85 °C		Unit
		Min. ^d	Max. ^d	Min. ^d			Max. ^d				
Dynamic Characteristics											
Source Off Capacitance ^e	$C_{S(off)}$	f = 1 MHz	DG506B	Room	4					pF	
Drain Off Capacitance ^e	$C_{D(off)}$				DG507B	37					
Channel On Capacitance ^e	$C_{D(on)}$				DG506B	43					
					DG507B	26					
Power Supply											
Power Supply Current	I+	V_{AX} , $V_{EN} = 0\text{ V}$, or 5 V		Room	0.005		0.1		0.1	mA	
				Full			0.1		0.1		

Notes:

- a. V_{AX} , V_{EN} = input voltage perform proper function.
- b. Room = 25 °C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
- e. Guaranteed by design, not subject to production test.
- f. $\Delta R_{DS(on)} = R_{DS(on)} \text{ max.} - R_{DS(on)} \text{ min.}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SCHEMATIC DIAGRAM Typical Channel

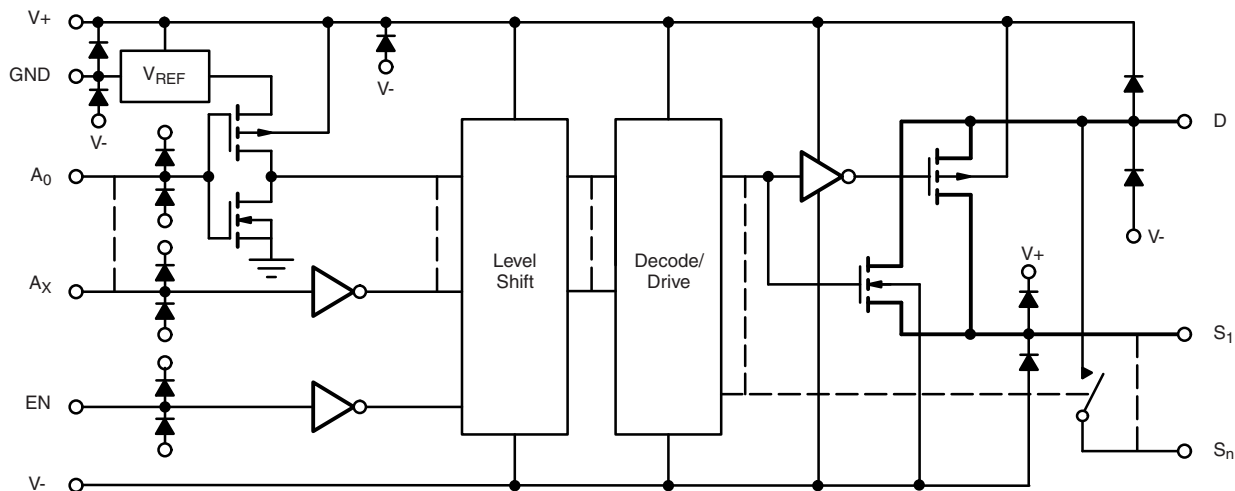
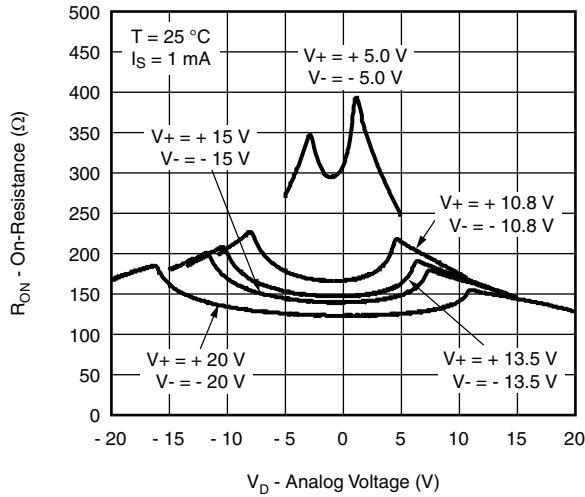
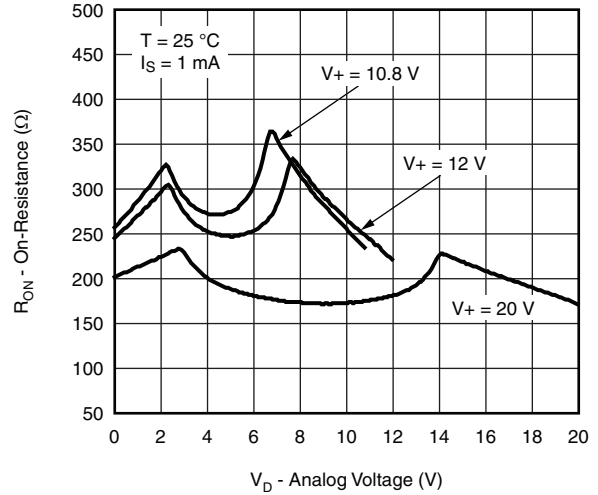


Figure 1.

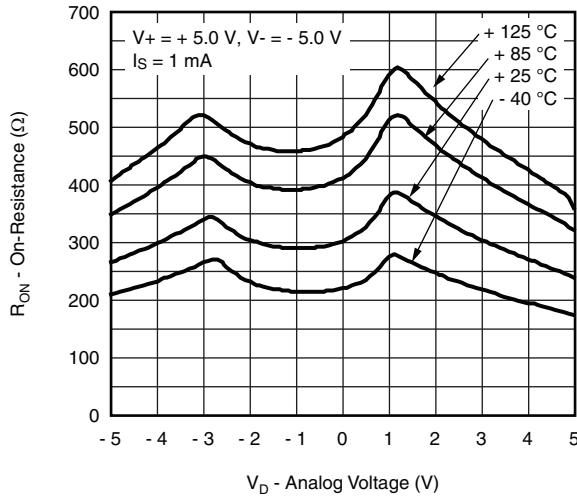
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



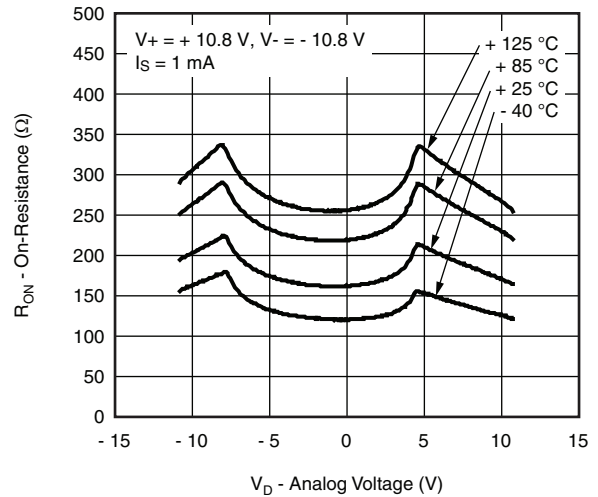
On-Resistance vs. V_D and Dual Supply Voltage



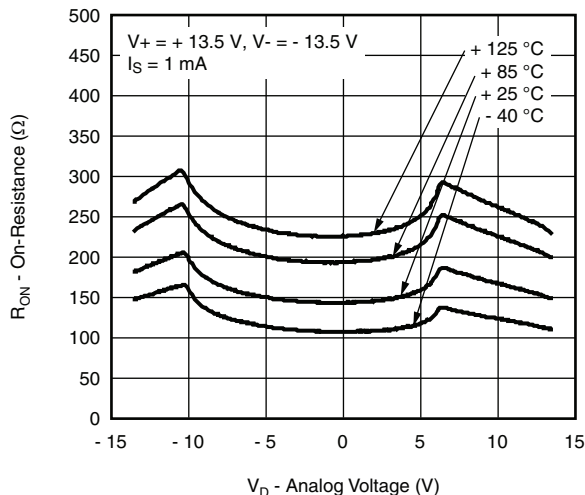
On-Resistance vs. V_D and Single Supply Voltage



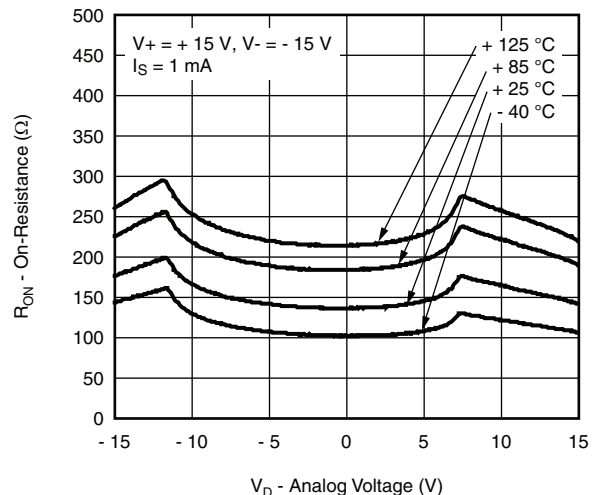
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

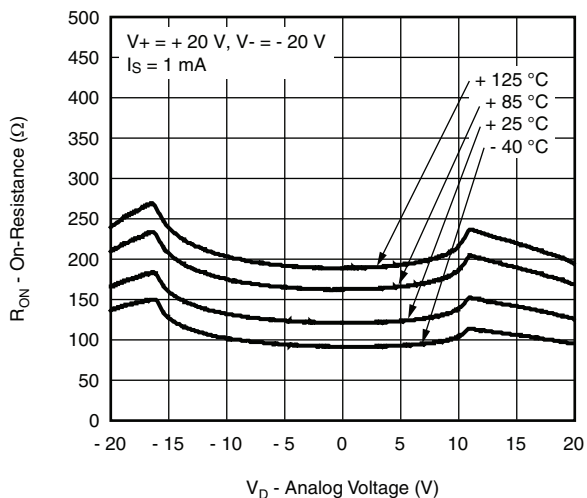


On-Resistance vs. Analog Voltage and Temperature

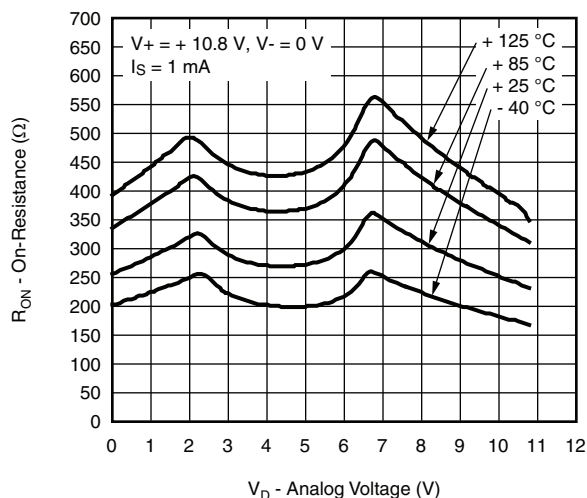


On-Resistance vs. Analog Voltage and Temperature

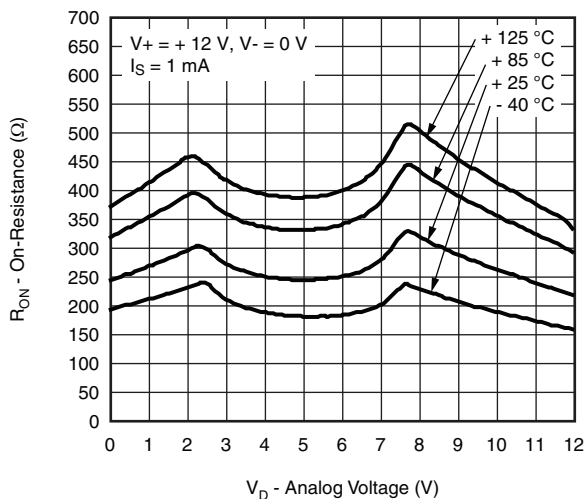
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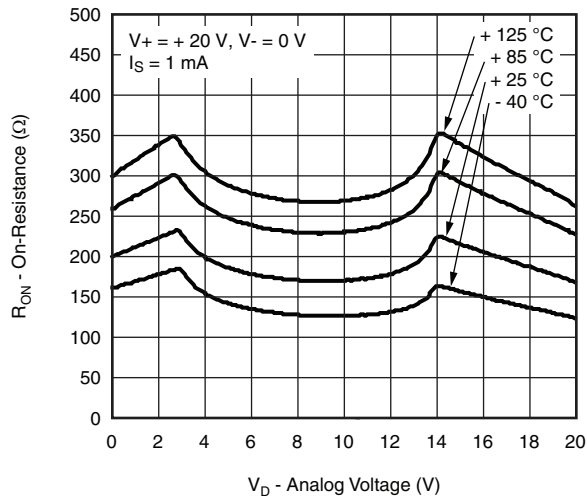
On-Resistance vs. Analog Voltage and Temperature



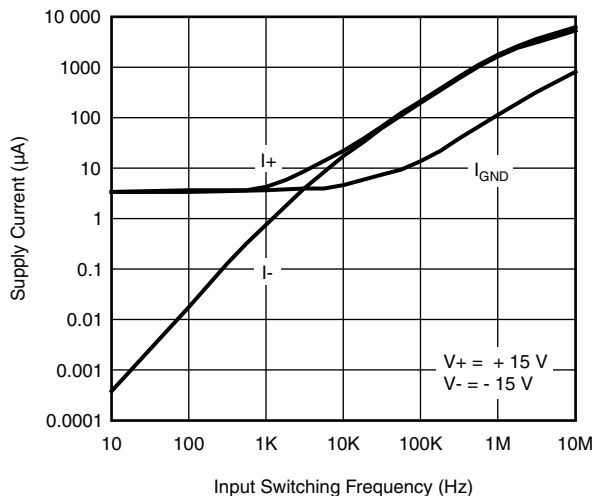
On-Resistance vs. Analog Voltage and Temperature



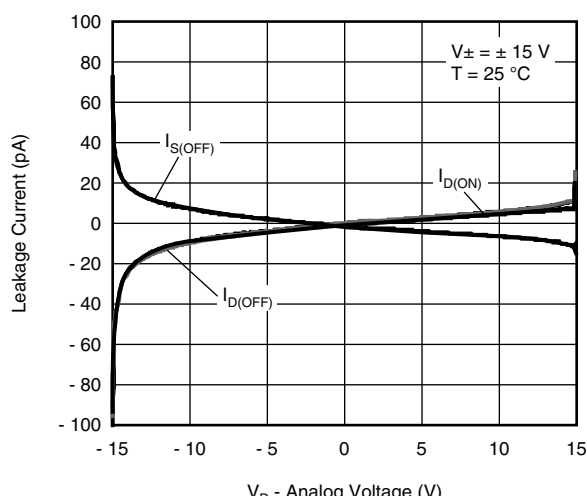
On-Resistance vs. Analog Voltage and Temperature



On-Resistance vs. Analog Voltage and Temperature

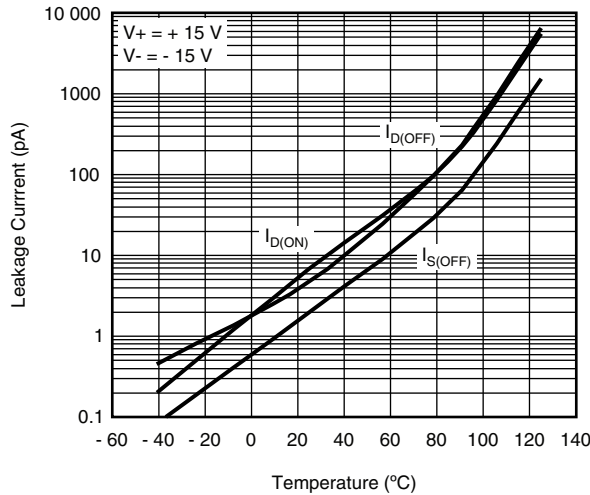


Supply Current vs. Input Switching Frequency

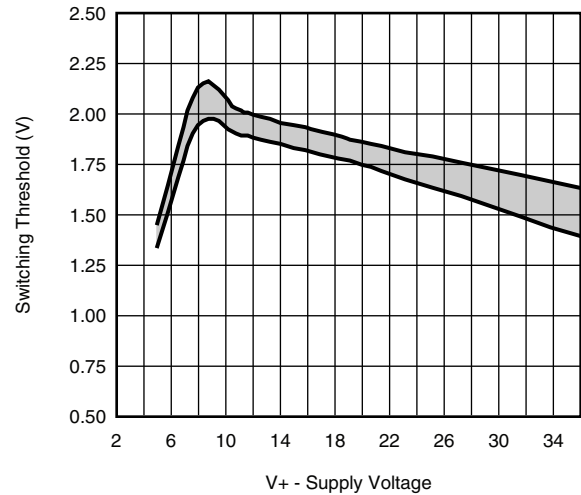


Leakage Current vs. Analog Voltage

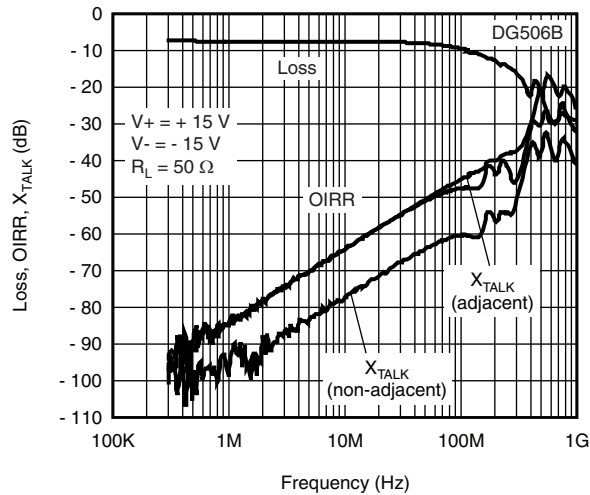
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



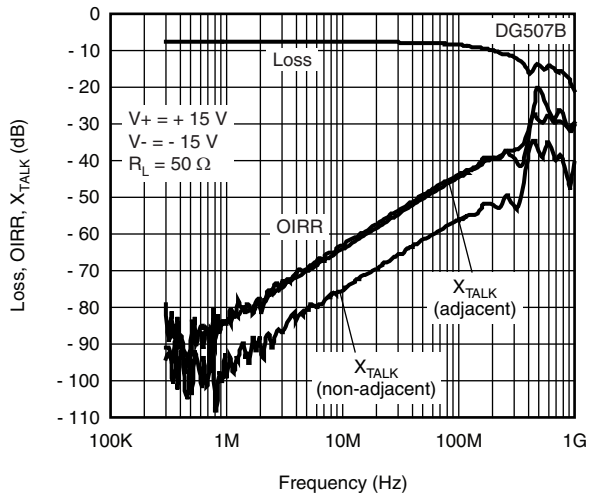
Leakage Current vs. Temperature



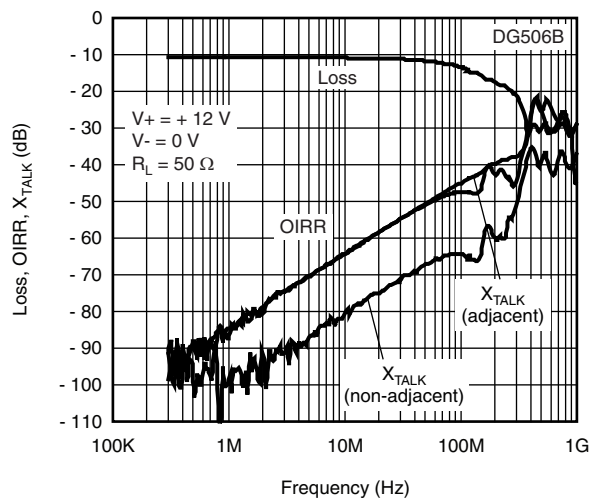
Switching Threshold vs. Single Supply V



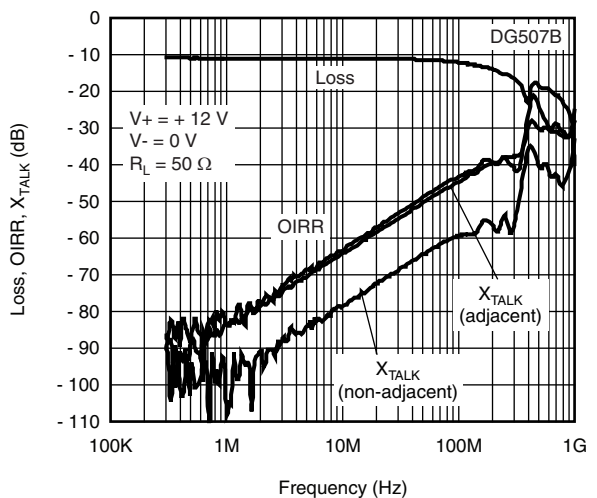
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

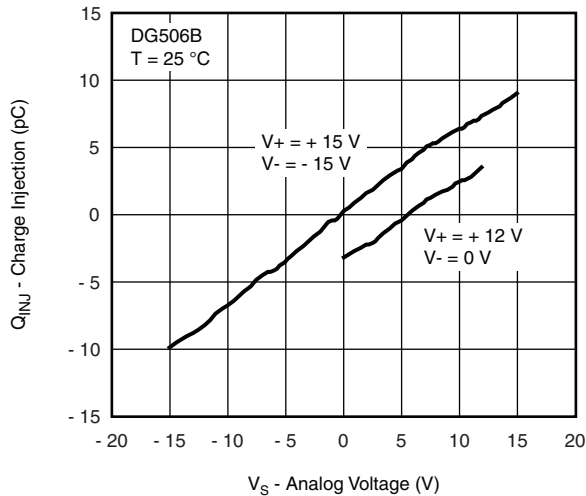


Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

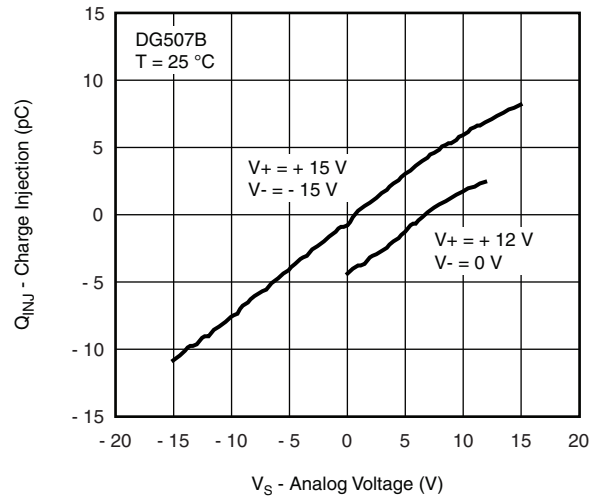


Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

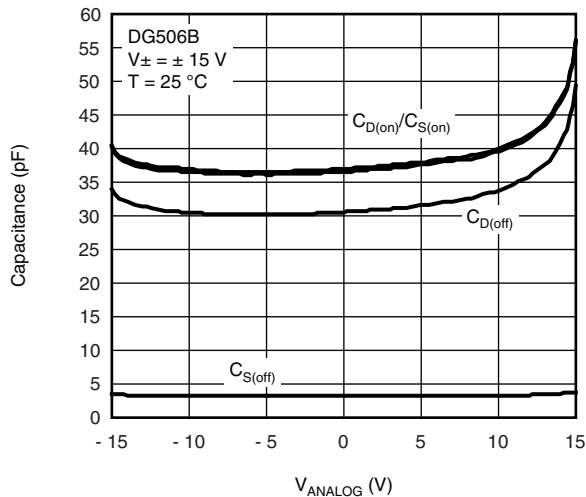
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



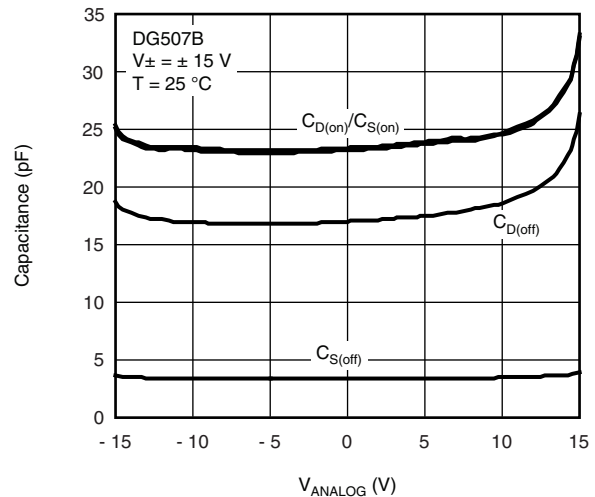
Charge Injection vs. Analog Voltage



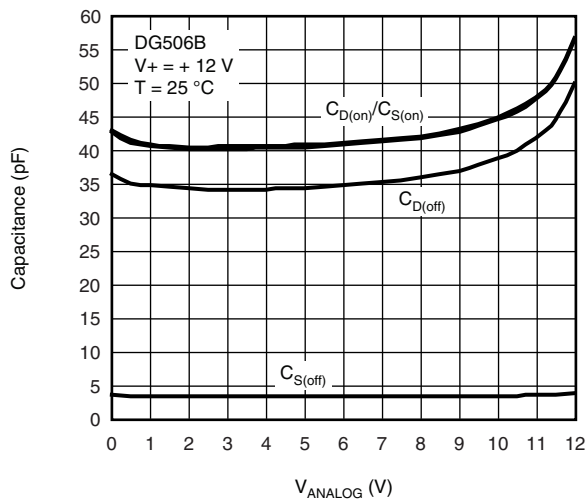
Charge Injection vs. Analog Voltage



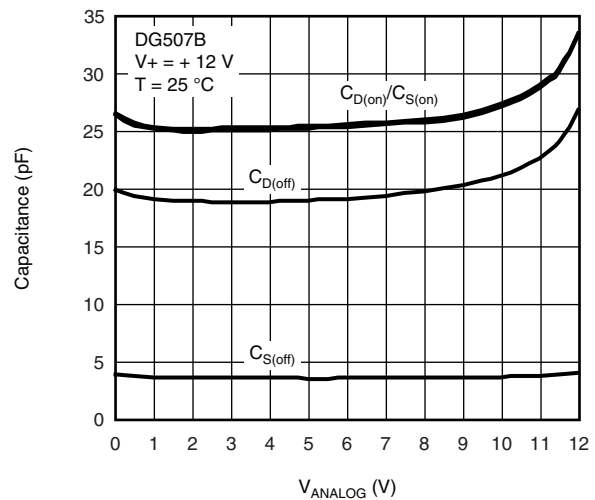
Capacitance vs. VANALOG



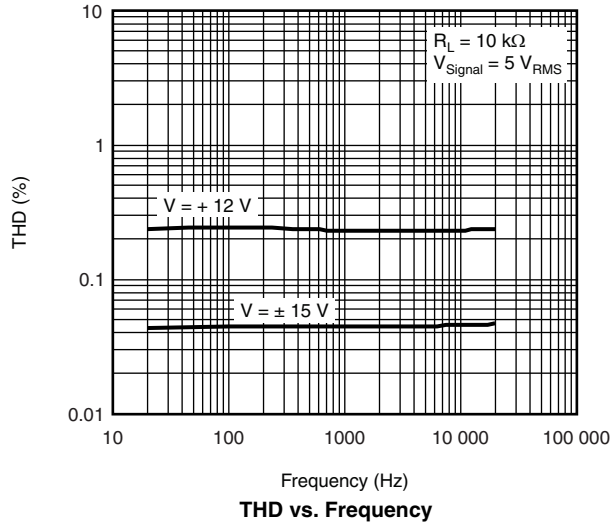
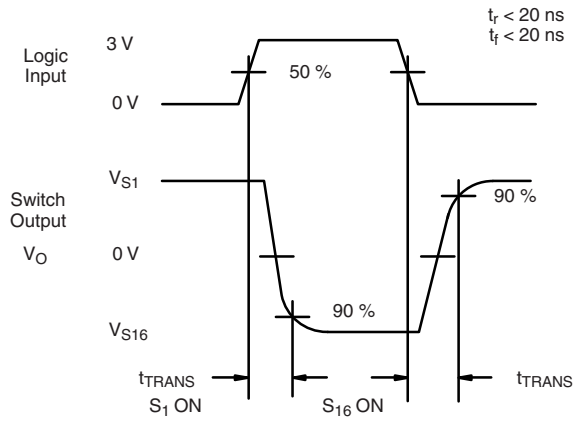
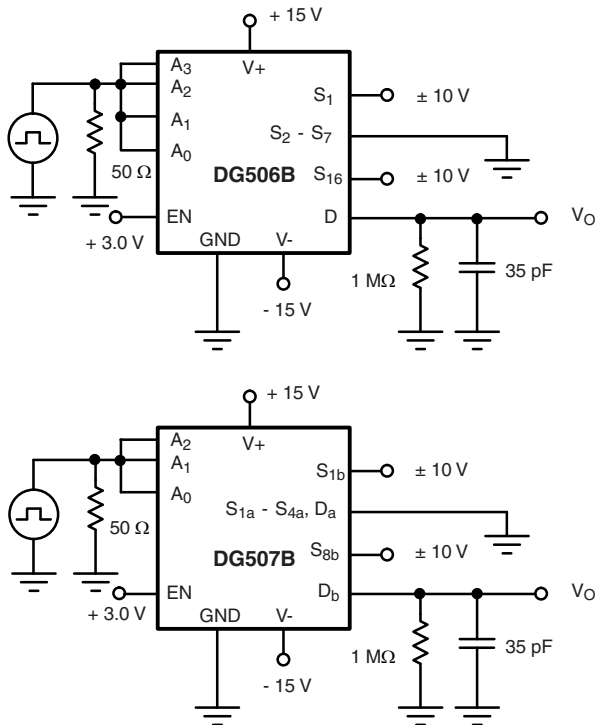
Capacitance vs. VANALOG



Capacitance vs. VANALOG



Capacitance vs. VANALOG

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

TEST CIRCUITS

Figure 2. Transition Time

TEST CIRCUITS

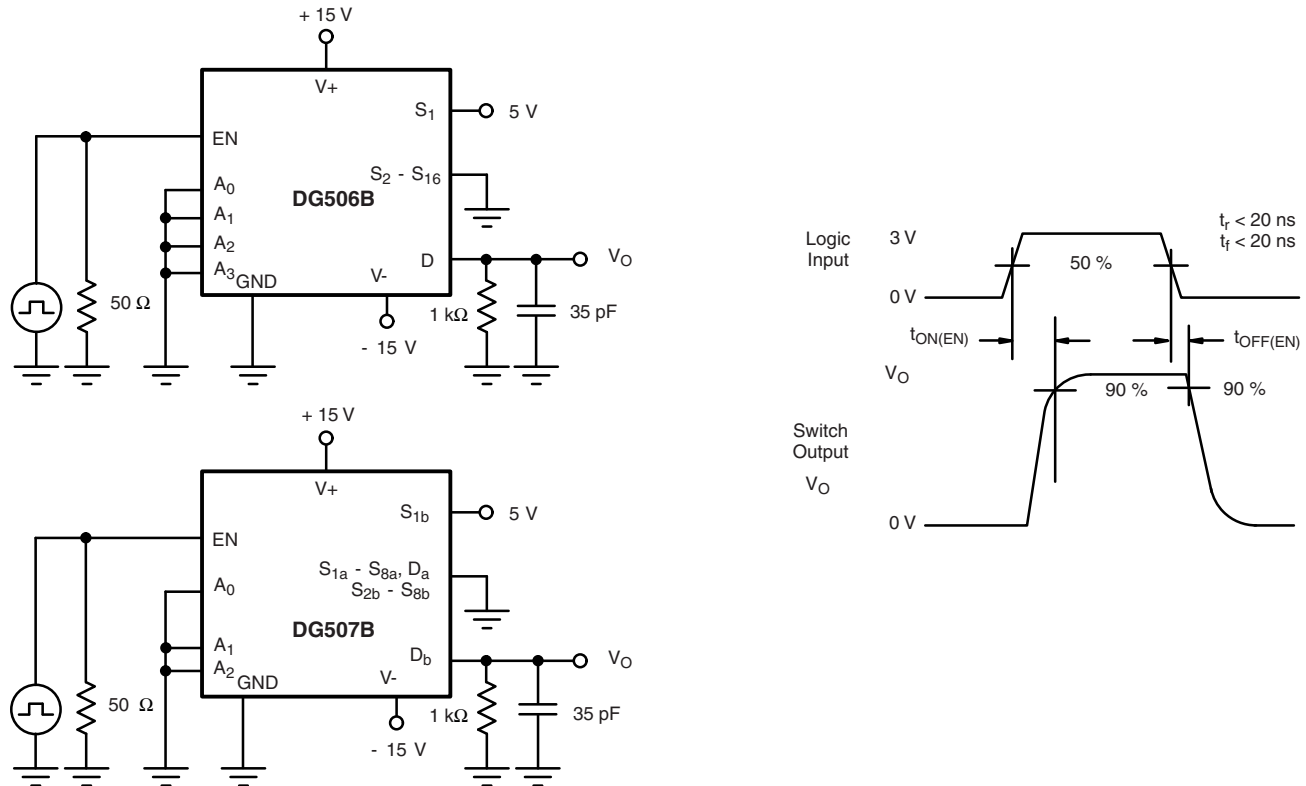


Figure 3. Enable Switching Time

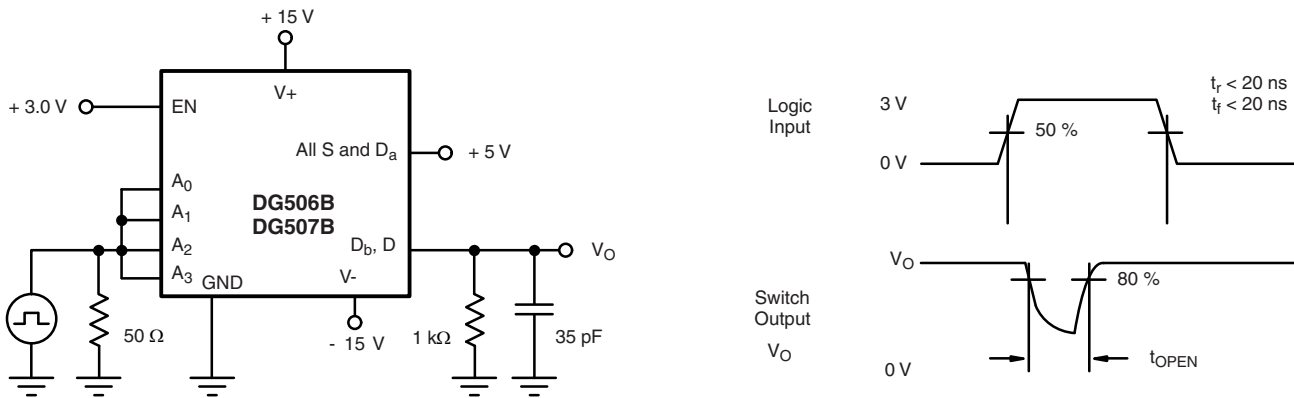
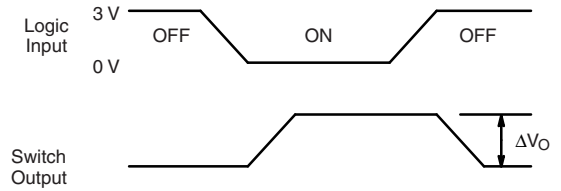
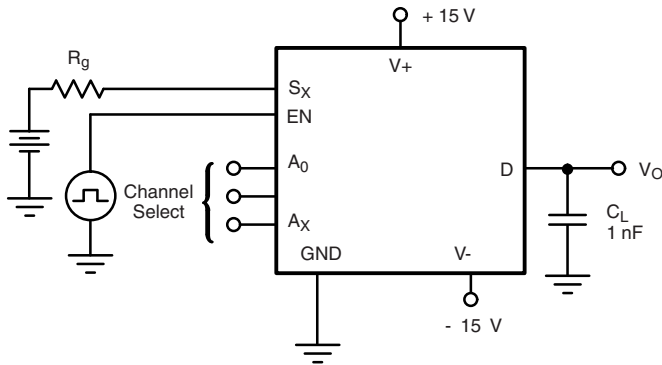
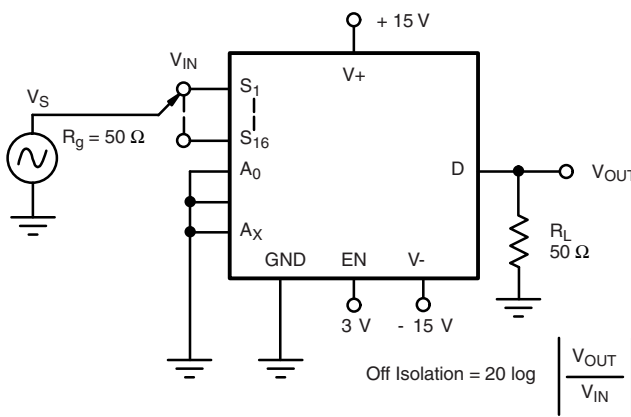
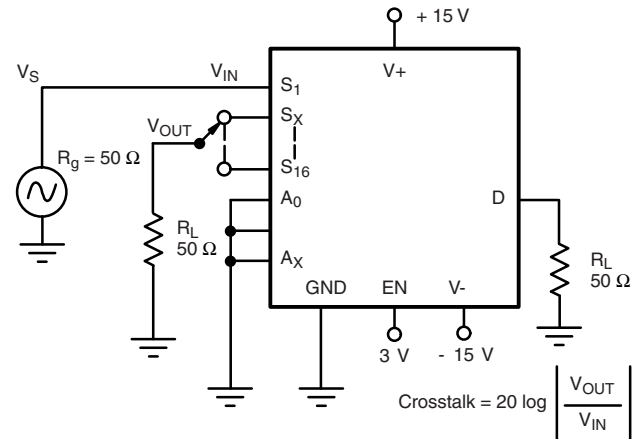
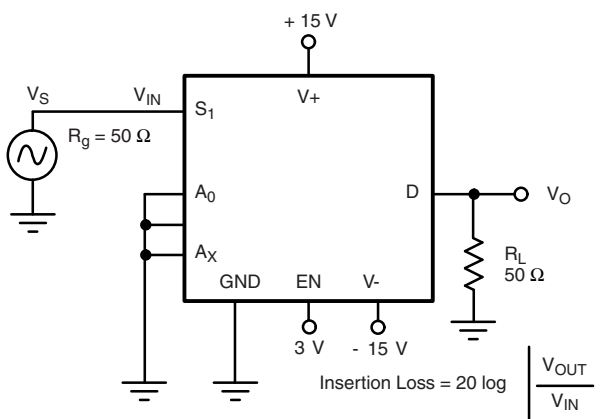
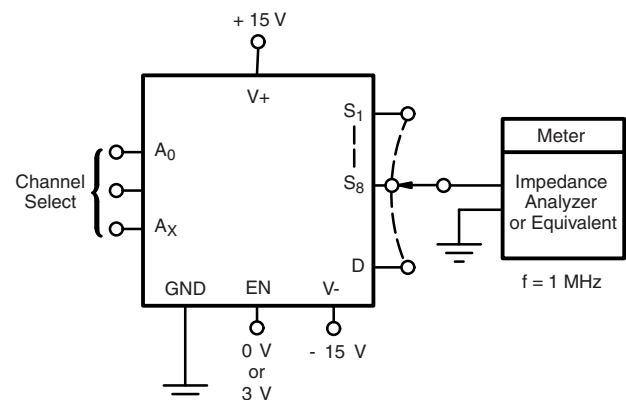


Figure 4. Break-Before-Make Interval

TEST CIRCUITS


ΔV_O is the measured voltage due to charge transfer error Q , when the channel turns off.

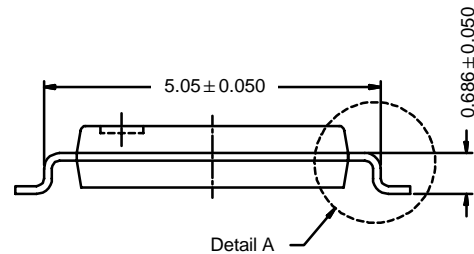
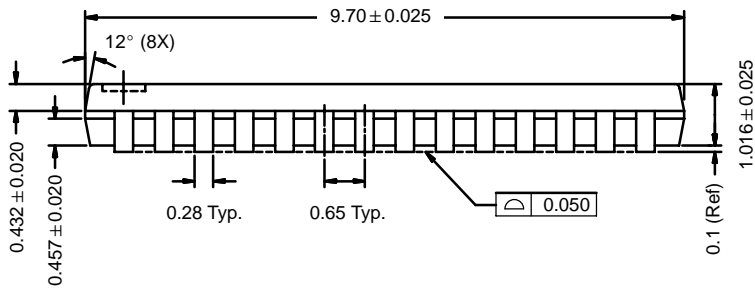
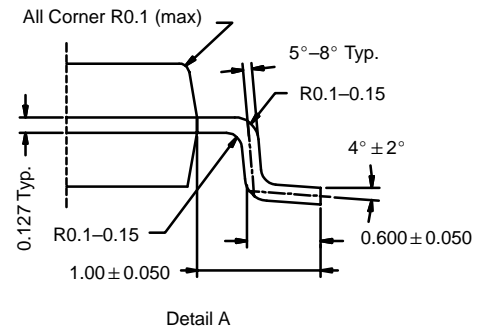
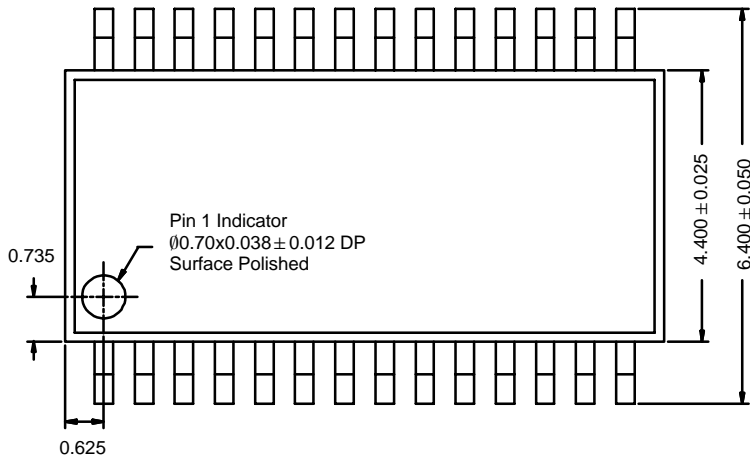
$$Q_{INJ} = C_L \times \Delta V_O$$

Figure 5. Charge Injection

Figure 6. Off Isolation

Figure 7. Crosstalk

Figure 8. Insertion Loss

Figure 9. Source Drain Capacitance

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TSSOP: 28-LEAD



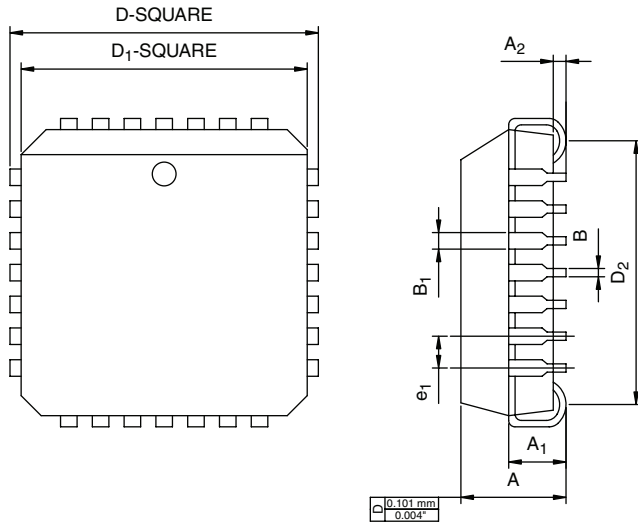
ECN: S-03946—Rev. C, 09-Jul-01
DWG: 5851

NOTES:

1. Package Surface: Shiny Finish (Ro 0.15 – 0.20).
2. Package Warpage: 0.012 (max).
3. Package Corner Radius: R0.1 mm (max).
4. Top to BTM Cavity Mismatch: 0.037 (max).
5. Tolerance: ± 0.050 unless otherwise specified.
6. End Flash Max: 0.1016 mm.



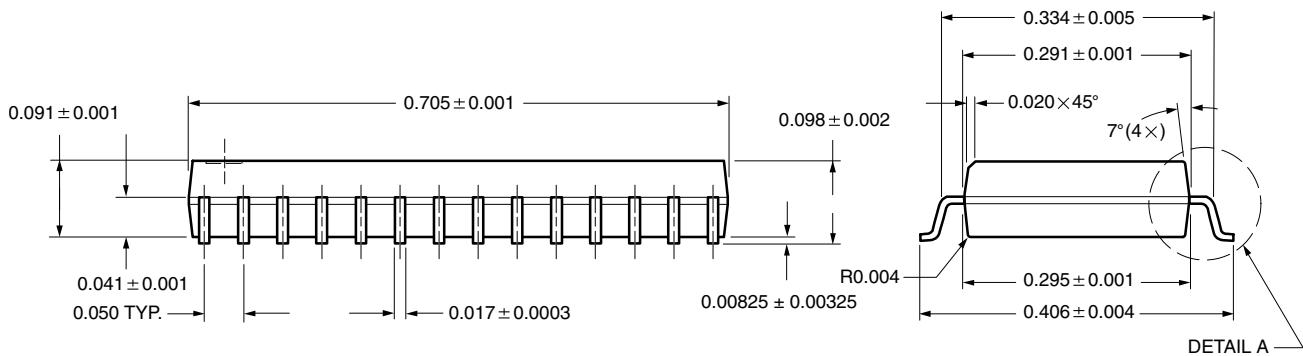
PLCC: 28-LEAD



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.20	4.57	0.165	0.180
A ₁	2.29	3.04	0.090	0.120
A ₂	0.51	-	0.020	-
B	0.331	0.553	0.013	0.021
B ₁	0.661	0.812	0.026	0.032
D	12.32	12.57	0.485	0.495
D ₁	11.430	11.582	0.450	0.456
D ₂	9.91	10.92	0.390	0.430
e ₁	1.27 BSC		0.050 BSC	
ECN: T09-0766-Rev. D, 28-Sep-09 DWG: 5491				



SOIC (WIDE-BODY): 28-LEADS



All Dimensions In Inches

ECN: E11-2209-Rev. D, 01-Aug-11
DWG: 5850



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