Precision 8-Ch/Dual 4-Ch/Triple 2-Ch Low Voltage Analog Switches/Multiplexers

DESCRIPTION

The DG9051, DG9052, DG9053 are low-voltage monolithic CMOS analog switches and multiplexers. DG9051 is an 8-channel multiplexer; DG9052 is a dual 4 channel multiplexer; and DG9053 is a triple single-pole/double throw (SPDT) switch.

They are designed to operate from a + 2.7 V to + 12 V single supply or ± 2.7 V to ± 6 V dual power supplies. All control logic inputs have guaranteed 2 V logic high/0.8 V logic low when operating from a single 5 V or dual ± 5 V supplies, and 2.4 V logic high/0.8 V logic low when V + = 12 V.

Built on Vishay Siliconix's proprietary high-density process, the DG9051, DG9052, DG9053 offer the advantage of bi-directional signal, rail to rail analog signal handling.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the Lead (Pb)-Free device terminations. For analog switching products manufactured with 100 % matte tin device termination, the Lead (Pb)-free "-E3"suffix is being used as a de-signator.

FEATURES

- **Halogen-free according to IEC 61249-2-21 Definition**
- 2.7 V to 12 V single supply or ± 2.7 V to ± 6 V dual aupply operation
- Guaranteed R_{ON} matching
- Low Voltage CMOS Logic Compatible
- Compliant to RoHS Directive 2002/95/EC

Pb-free
RoHS COMPLIANT
HALOGEN FREE

BENEFITS

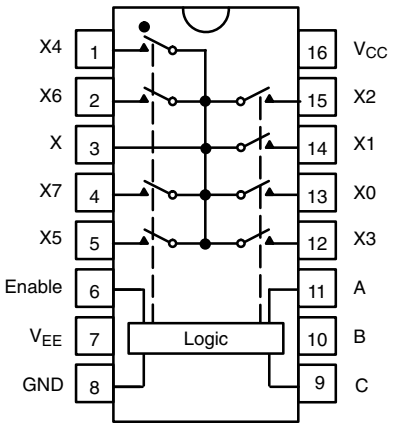
- Wide operation voltage range
- Pin compatible with 74HC4051/2/5
- Guaranteed low leakage

APPLICATIONS

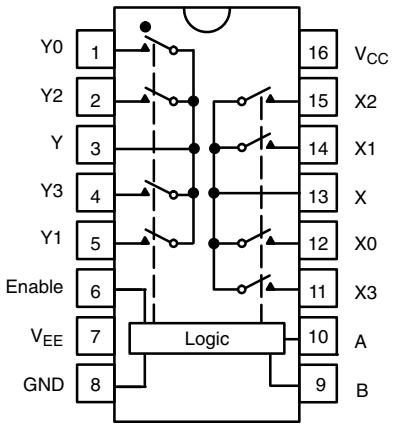
- Battery powered equipment
- Test process equipment
- Communication systems
- A/V and mixed signal routing
- Automotive

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

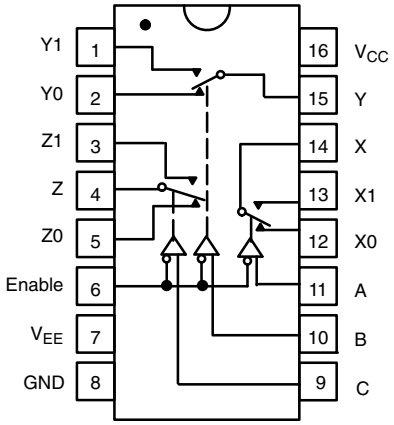
DG9051



DG9052



DG9053



ORDERING INFORMATION		
Temp. Range	**Package**	**Part Number**
- 40 °C to 85°C	TSSOP-16	DG9051DQ-T1-E3
		DG9052DQ-T1-E3
		DG9053DQ-T1-E3

The information shown here is a preliminary product proposal, not a commercial product data sheet. Siliconix is not committed to produce this or any similiar product. This information should not be used for design purposes, nor construed as an offer to furnish or sell such products.

TRUTH TABLE

Enable Input	Select Inputs			On Switches		
	C*	B	A	DG9051	DG9052	DG9053
H	X	X	X	All switches open	All switches open	All switches open
L	L	L	L	X - X0	X - X0, Y - Y0	X - X0, Y - Y0, Z - Z0
L	L	L	H	X - X1	X - X1, Y - Y1	X - X1, Y - Y0, Z - Z0
L	L	H	L	X - X2	X - X2, Y - Y2	X - X0, Y - Y1, Z - Z0
L	L	H	H	X - X3	X - X3, Y - Y3	X - X1, Y - Y1, Z - Z0
L	H	L	L	X - X4	X - X0, Y - Y0	X - X0, Y - Y0, Z - Z1
L	H	L	H	X - X5	X - X1, Y - Y1	X - X1, Y - Y0, Z - Z1
L	H	H	L	X - X6	X - X2, Y - Y2	X - X0, Y - Y1, Z - Z1
L	H	H	H	X - X7	X - X3, Y - Y3	X - X1, Y - Y1, Z - Z1

X = Don't care

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Limit	Unit
Voltage Referenced to V-	V +	13.5	V
	GND	7	
Digital Inputs[a]	V_S, V_D	(V -) - 0.3 to (V +) + 0.3	
Current (Any Terminal Except S or D)		30	mA
Continuous Current, S or D		100	
Peak Current, S or D (Pulsed at 1 ms, 10 % Duty Cycle Max.)		200	
Package Solder Reflow Conditions[b]	IR/Convection	260	°C
Storage Temperature		- 65 to 150	
Power Dissipation (Packages)[c]	T_A = 70 °C, TSSOP-16[d]	925	mW

SPECIFICATIONS (Single Supply 12 V)							
Parameter	**Symbol**	**Test Condition Unless Otherwise Specified** V + = 12 V, ± 10 %, V - = 0 V V_A, $V_{\overline{EN}}$ = 0.8 V or 2.4 V[f]	**Temp.[b]**	**Limits** - 40 °C to 85°C **Min.[c]**	**Typ.[d]**	**Max.[c]**	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	0		12	V
On-Resistance	R_{ON}	V_D = 3.5 V, I_S = 1 mA Sequence Each Switch On	Room Full		30	40 50	Ω
R_{ON} Match Between Channels[g]	ΔR_{ON}	V_D = 3.5 V, I_S = 1 mA	Room			5	
Switch Off Leakage Current	$I_{S(off)}$	$V_{\overline{EN}}$ = 2.4 V, V_D = 11 V or 1 V, V_S = 1 V or 11 V	Room Full	- 1 - 20		1 20	nA
	$I_{D(off)}$		Room Full	- 1 - 20		1 20	
Channel On Leakage Current	$I_{D(on)}$	$V_{\overline{EN}}$ = 0 V, V_S = V_D = 1 V or 11 V	Room Full	- 2 - 10		2 10	
Digital Control							
Logic High Input Voltage	V_{INH}		Full	2.4			V
Logic Low Input Voltage	V_{INL}		Full			0.8	
Input Current	I_{IN}	V_{AX} = $V_{\overline{EN}}$ = 2.4 V or 0.8 V	Full	- 1		1	µA
Dynamic Characteristics							
Transition Time	t_{TRANS}	V_{NO}/V_{NC} = 8 V/0 V, 0 V/8 V R_L = 300 Ω, C_L = 35 pF	Room Full		26	35 55	ns
Break-Before-Make Time	t_{BBM}	$V_{X,Y,Z}$ = 5 V, V_S = 0 V, R_L = 306 Ω, C_L = 35 pF	Room Full	3	10		
Enable Turn-On Time	$t_{ON(\overline{EN})}$		Room Full		20	35 45	
Enable Turn-Off Time	$t_{OFF(\overline{EN})}$		Room Full		16	30 40	
Charge Injection[e]	Q	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		38		pC
Off-Isolation[e,h]	OIRR	f = 1 MHz, R_L = 50 Ω	Room		- 78		dB
Crosstalk[e]	X_{TALK}		Room		- 83		
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, $V_{\overline{EN}}$ = 2.4 V	Room		4		pF
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 2.4 V	Room		8		
Drain On Capacitance[e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 0 V	Room		15		
Power Supply							
Power Supply Current	I+	$V_{\overline{EN}}$ = V_A = 0 V or V+	Room			1	µA

SPECIFICATIONS (Dual Supply V + = 5 V, V - = - 5 V)							
Parameter	**Symbol**	**Test Condition Unless Otherwise Specified** V + = 5 V, V - = - 5 V ± 10 % V_A, $V_{\overline{EN}}$ = 0.8 V or 2 V[f]	**Temp.[b]**	**Limits** - 40 °C to 85°C **Min.[c]**	**Typ.[d]**	**Max.[c]**	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	- 5		5	V
On-Resistance	R_{ON}	V + = 4.5 V, V - = - 4.5 V, V_D = ± 3 V, I_S = 1 mA Sequence Each Switch On	Room Full		35	55 60	Ω
R_{ON} Match Between Channels[g]	ΔR_{ON}	V + = 4.5 V, V - = - 4.5 V, V_D = ± 3 V, I_S = 1 mA	Room			5	Ω
On-Resistance Flatness[i]	R_{ON} Flatness		Room		7	10	Ω
Switch Off Leakage Current[a]	$I_{S(off)}$	V + = 5.5 V, V - = - 5.5 V $V_{\overline{EN}}$ = 2 V, V_D = ± 4 .5 V, V_S = ± 4.5 V	Room Full	- 1 - 20		1 20	nA
	$I_{D(off)}$		Room Full	- 1 - 20		1 20	nA
Channel On Leakage Current[a]	$I_{D(on)}$	V + = 5.5 V, V - = - 5.5 V $V_{\overline{EN}}$ = 0 V, V_D = ± 4.5 V, V_S = ± 4.5 V	Room Full	- 2 - 10		2 10	nA
Digital Control							
Logic High Input Voltage	V_{INH}		Full	2			V
Logic Low Input Voltage	V_{INL}		Full			0.8	V
Input Current[a]	I_{IN}	V_{AX} = $V_{\overline{EN}}$ = 2 V or 0.8 V	Full	- 1		1	µA
Dynamic Characteristics							
Transition Time[e]	t_{TRANS}	V + = 4.5 V, V - = - 4.5 V $V_{NO/NC}$ = ± 3 V, R_L = 300 Ω, C_L = 35 pF	Room Full		35	50 65	ns
Break-Before-Make Time[e]	t_{BBM}	$V_{X,Y,Z}$ = +/- 3 V, V_S = 0 V, R_L = 300 Ω, C_L = 35 pF	Room Full	5	12		ns
Enable Turn-On Time[e]	$t_{ON(\overline{EN})}$		Room Full		38	55 70	ns
Enable Turn-Off Time[e]	$t_{OFF(\overline{EN})}$		Room Full		22	35 50	ns
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, $V_{\overline{EN}}$ = 2 V	Room		5		pF
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 2 V	Room		9		pF
Drain On Capacitance[e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 0 V	Room		13		pF
Power Supply							
Power Supply Current	I+	$V_{\overline{EN}}$ = V_A = 0 V or V +	Room			1	µA
	I-		Room	- 1			µA

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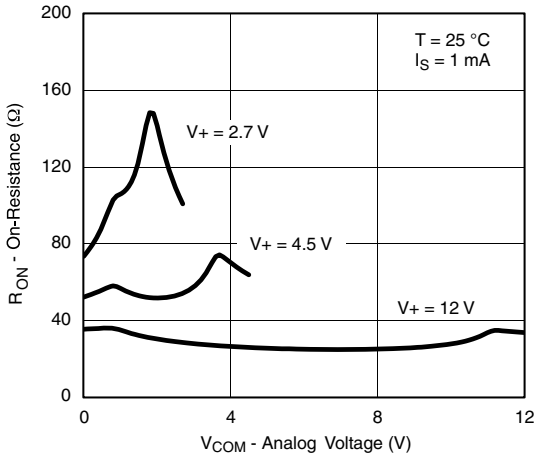
SPECIFICATIONS (Single Supply 5 V)							
Parameter	**Symbol**	**Test Condition Unless Otherwise Specified** V + = 5 V, ± 10 %, V - = 0 V V_A, $V_{\overline{EN}}$ = 0.8 V or 2 V[f]	**Temp.[b]**	**Limits** - 40 °C to 85°C **Min.[c]**	**Typ.[d]**	**Max.[c]**	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	0		5	V
On-Resistance	R_{ON}	V + = 4.5 V, V_D or V_S = 3 V or 3.5 V, I_S = 1 mA	Room Full		80	100 120	Ω
R_{ON} Match Between Channels[g]	ΔR_{ON}	V + = 4.5 V, V_D = 3 V, I_S = 1 mA	Room			8	
Switch Off Leakage Current[a]	$I_{S(off)}$	V + = 5.5 V, $V_{\overline{EN}}$ = 2 V V_S = 1 V or 4.5 V, V_D = 4.5 V or 1 V	Room Full	- 1 - 20		1 20	nA
	$I_{D(off)}$		Room Full	- 1 - 20		1 20	
Channel On Leakage Current[a]	$I_{D(on)}$	V + = 5.5 V, $V_{\overline{EN}}$ = 0 V V_D = V_S = 1 V or 4.5 V	Room Full	- 2 - 10		2 10	
Digital Control							
Logic High Input Voltage	V_{INH}		Full	2			V
Logic Low Input Voltage	V_{INL}		Full			0.8	
Input Current[a]	I_{IN}	V_{AX} = $V_{\overline{EN}}$ = 2 V or 0.8 V	Full	- 1		1	µA
Dynamic Characteristics							
Transition Time	t_{TRANS}	V + = 4.5 V, V - = 0 V, $V_{NO\ /\ NC}$ = 3 V / 0 V, 0 V / 3 V, R_L = 300 Ω, C_L = 35 pF	Room		40		ns
Break-Before-Make Time	t_{BBM}	V + = 4.5 V, $V_{X,Y,Z}$ = 3 V, V_S = 0 V, R_L = 300 Ω, C_L = 35 pF	Room		15		
Enable Turn-On Time	$t_{ON(\overline{EN})}$		Room		40		
Enable Turn-Off Time	$t_{OFF(\overline{EN})}$		Room		20		
Charge Injection[e]	Q	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		20		pC
Off-Isolation[e,h]	OIRR	f = 1 MHz, R_L = 50 Ω	Room		- 79		dB
Crosstalk[e]	X_{TALK}		Room		- 83		
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, $V_{\overline{EN}}$ = 0 V	Room		4		pF
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 2 V	Room		8		
Drain On Capacitance[e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 0 V	Room		15		
Power Supply							
Power Supply Current	I+	$V_{\overline{EN}}$ = V_A = 0 V or V +	Room			1	µA

SPECIFICATIONS (Single Supply 3 V)							
Parameter	**Symbol**	**Test Condition Unless Otherwise Specified** V + = 3 V, ± 10 %, V - = 0 V $V_{\overline{EN}}$ = 0.4 V or 2 V	**Temp.[b]**	**Limits** - 40 °C to 85°C **Min.[c]**	**Typ.[d]**	**Max.[c]**	**Unit**
Analog Switch							
Analog Signal Range[e]	V_{ANALOG}		Full	0		3	V
On-Resistance	R_{ON}	V + = 2.7 V, V_D = 1.5 V, I_S = 0.1 mA	Room		130		Ω
R_{ON} Match Between Channels[g]	ΔR_{ON}	V + = 2.7 V, V_D = 1.5 V, I_S = 0.1 mA	Room			12	Ω
Switch Off Leakage Current[a]	$I_{S(off)}$	V + = 3.3 V, $V_{\overline{EN}}$ = 2 V V_S = 3 or 0.3 V, V_D = 0.3 or 3 V	Room Full	- 1 - 20		1 20	nA
	$I_{D(off)}$		Room Full	- 1 - 20		1 20	nA
Channel On Leakage Current[a]	$I_{D(on)}$	V + = 3.3 V, $V_{\overline{EN}}$ = 0 V V_S = 3 or 0.3 V, V_D = 0.3 or 3 V	Room Full	- 2 - 10		2 10	nA
Digital Control							
Logic High Input Voltage	V_{INH}		Full	2			V
Logic Low Input Voltage	V_{INL}		Full			0.4	V
Input Current[a]	I_{IN}	V_{AX} = $V_{\overline{EN}}$ = 2 V or 0.4 V	Full	- 1		1	µA
Dynamic Characteristics							
Transition Time	t_{TRANS}	V + = 2.7 V, $V_{NO/NC}$ = 1.5 V/0 V, 0 V/1.5 V R_L = 300 Ω, C_L = 35 pF	Room		80		ns
Break-Before-Make Time	t_{BBM}	V + = 2.7 V, $V_{X,Y,Z}$ = 1.5 V, V_S = 0 V, R_L = 300 Ω, C_L = 35 pF	Room Full	5	25		ns
Enable Turn-On Time	$t_{ON(\overline{EN})}$		Room		90		ns
Enable Turn-Off Time	$t_{OFF(\overline{EN})}$		Room		30		ns
Charge Injection[e]	Q	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room		9		pC
Off-Isolation[e,h]	OIRR	f = 1 MHz, R_L = 50 Ω	Room		- 78		dB
Crosstalk[e]	X_{TALK}		Room		- 83		dB
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz, V_S = 0 V, $V_{\overline{EN}}$ = 1.8 V	Room		5		pF
Drain Off Capacitance[e]	$C_{D(off)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 1.8 V	Room		10		pF
Drain On Capacitance[e]	$C_{D(on)}$	f = 1 MHz, V_D = 0 V, $V_{\overline{EN}}$ = 0 V	Room		15		pF
Power Supply							
Power Supply Current	I+	$V_{\overline{EN}}$ = V_A = 0 V or V +	Room			1	µA

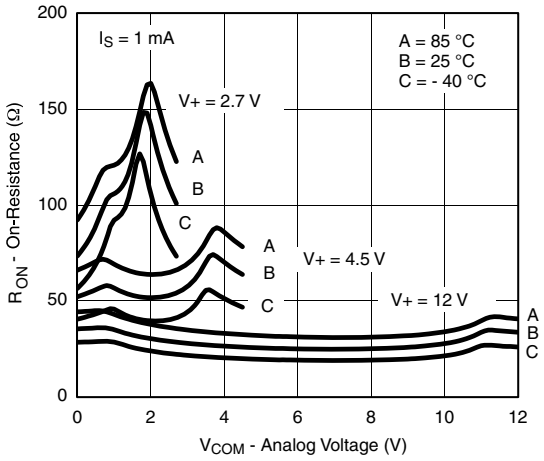
Notes:
a. Leakage parameters are guaranteed by worst case test condition and not subject to production test.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. ΔR_{DON} = R_{DON} Max - R_{DON} Min.
h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin.
i. R_{DON} flatness is measured as the difference between the minimum and maximum measured values across a defined Analog signal.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

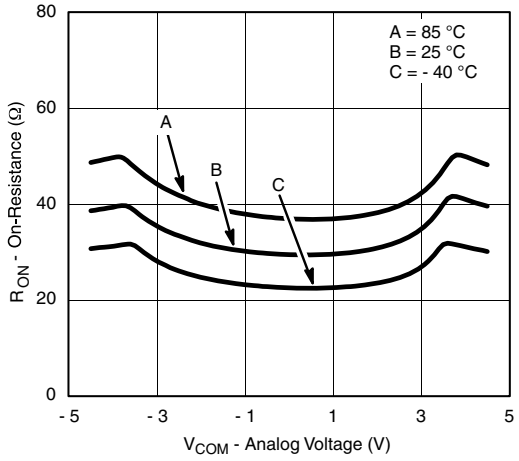
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



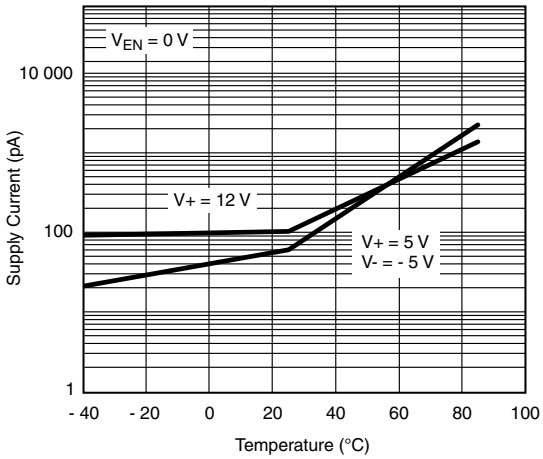
R_{ON} vs. V_{COM} and Supply Voltage



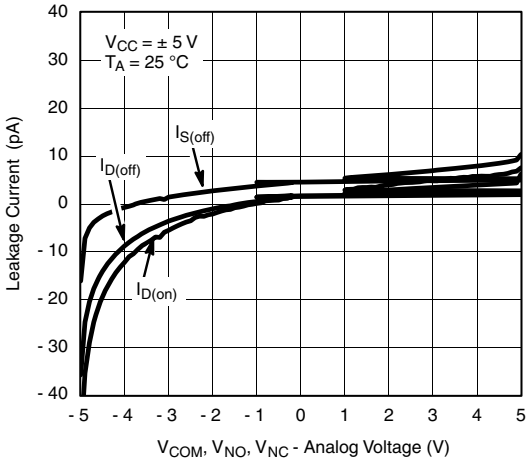
R_{ON} vs. Analog Voltage and Temperature



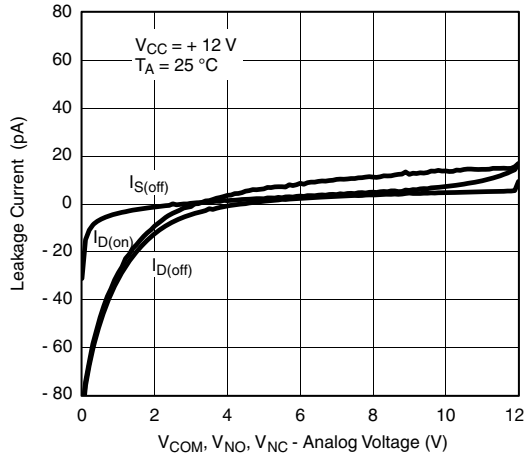
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Temperature

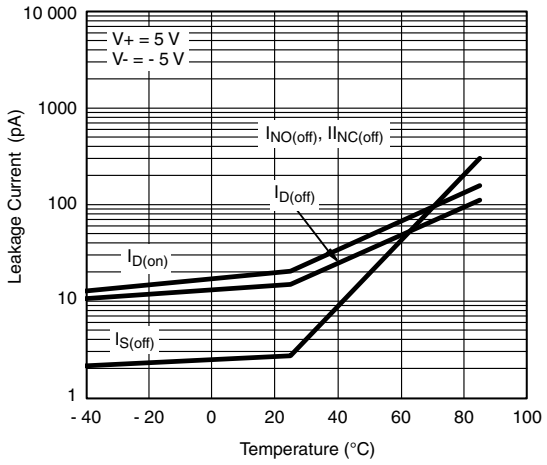


Leakage Current vs. Analog Voltage

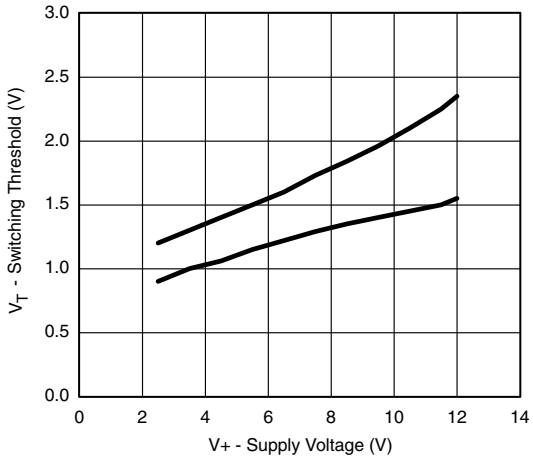


Leakage Current vs. Analog Voltage

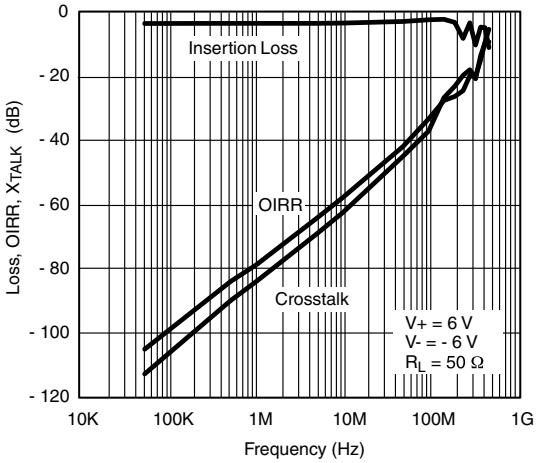
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



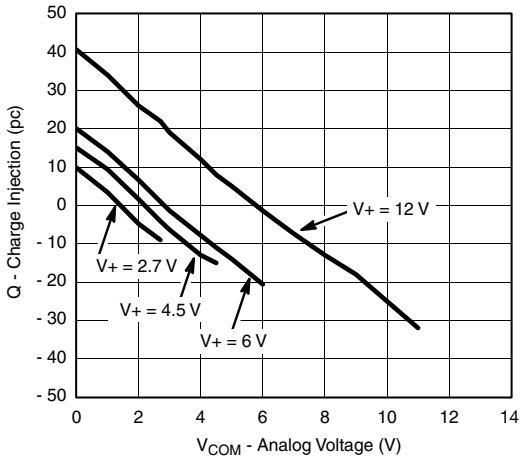
Leakage Current vs. Temperature



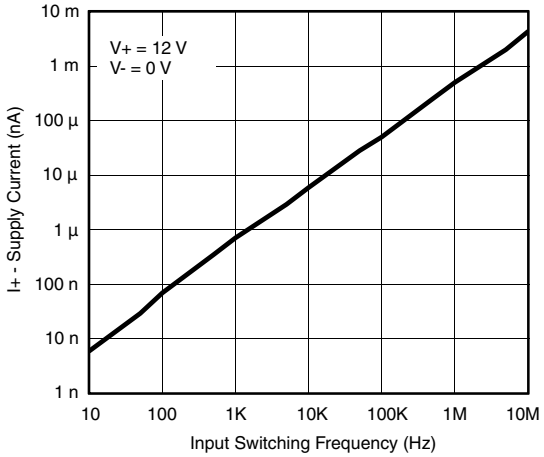
Switching Threshold vs. Supply Voltage



Insertion Loss, Off-Isolation Crosstalk vs. Frequency

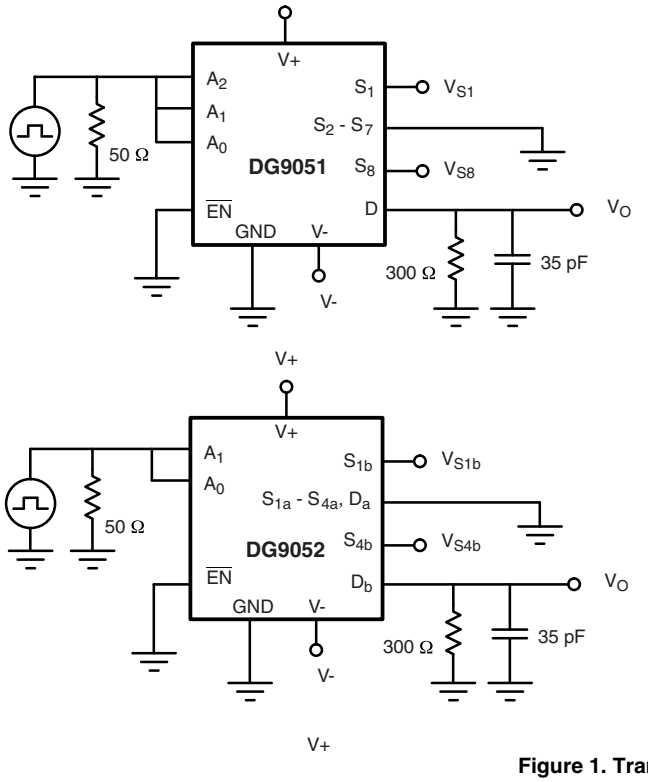


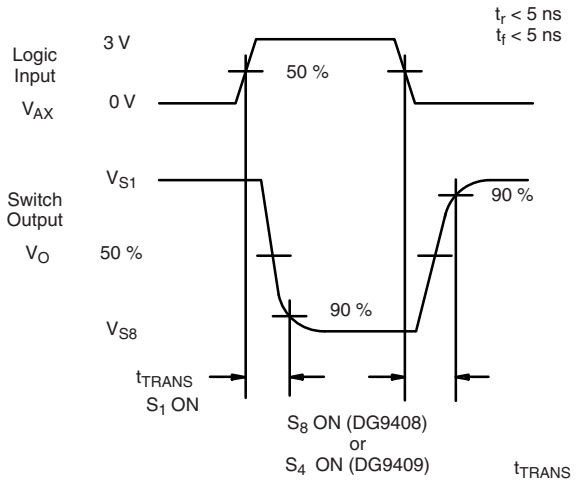
Charge Injection vs. Analog Voltage



Supply Current vs. Input Switching Frequency

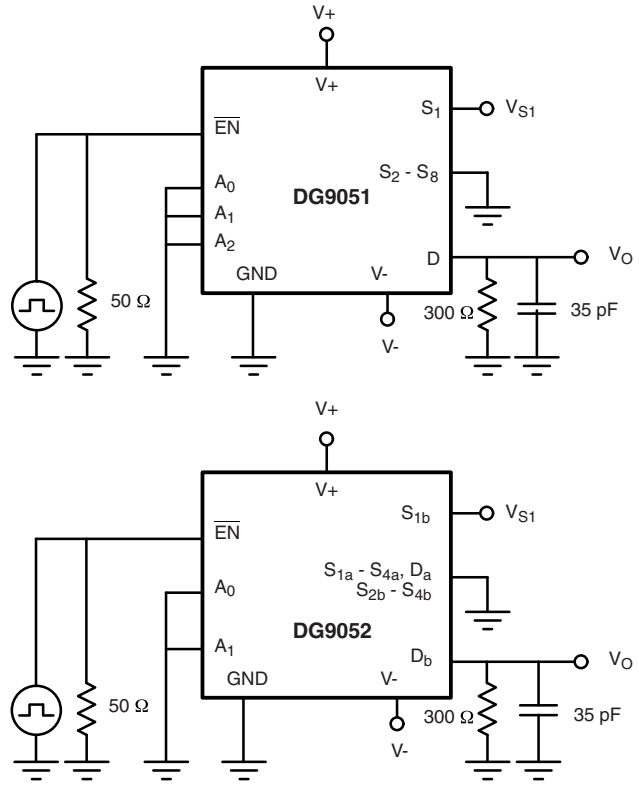
TEST CIRCUITS

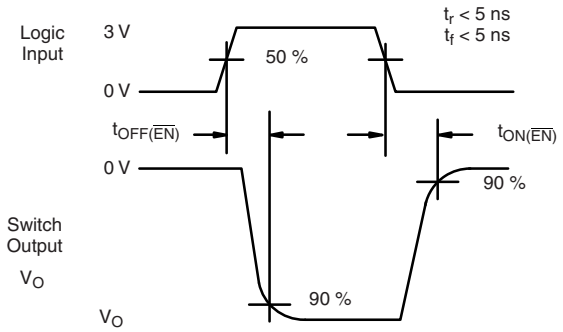




Return to Specifications:
Single Supply 12 V
Dual Supply V+ = 5 V, V- = - 5 V
Single Supply 5 V
Single Supply 3 V

Figure 1. Transition Time

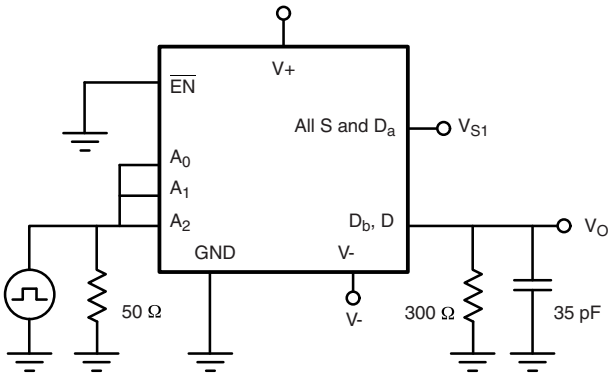


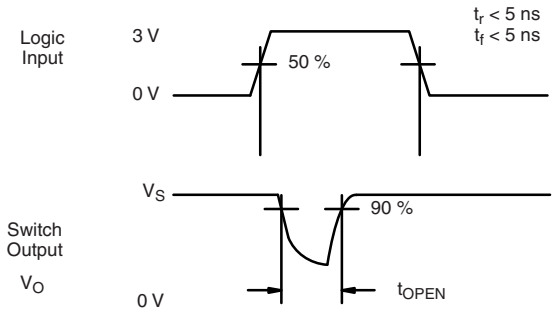


Return to Specifications:
Single Supply 12 V
Dual Supply V+ = 5 V, V- = - 5 V
Single Supply 5 V
Single Supply 3 V

Figure 2. Enable Switching Time

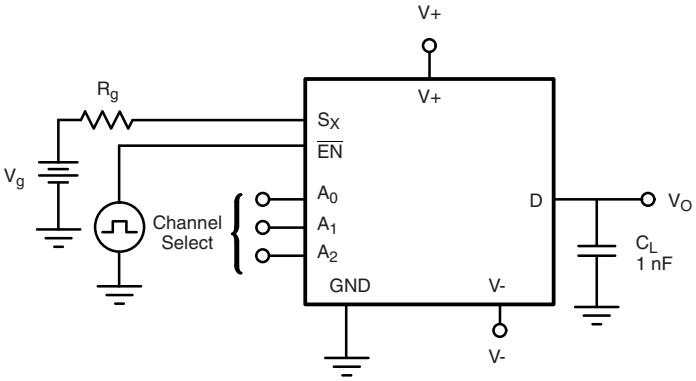
TEST CIRCUITS

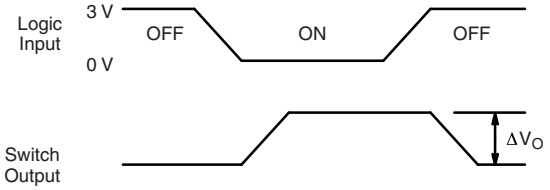




Return to Specifications:
Single Supply 12 V
Dual Supply V+ = 5 V, V- = - 5 V
Single Supply 5 V
Single Supply 3 V

Figure 3. Break-Before-Make Interval





ΔV_O is the measured voltage due to charge transfer error Q, when the channel turns off.

$Q = C_L \times \Delta V_O$

Figure 4. Charge Injection

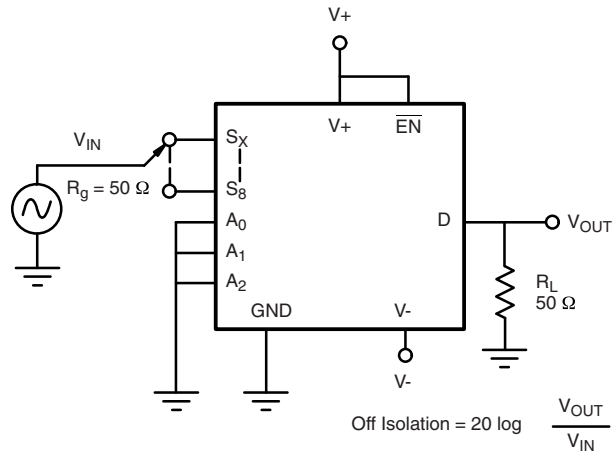


Figure 5. Off Isolation

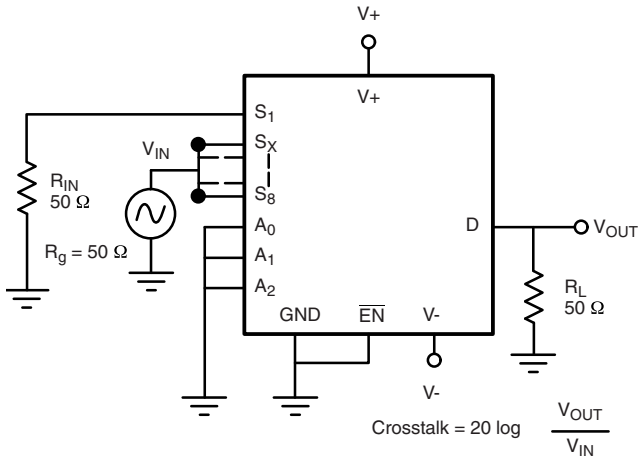


Figure 6. Crosstalk

TEST CIRCUITS

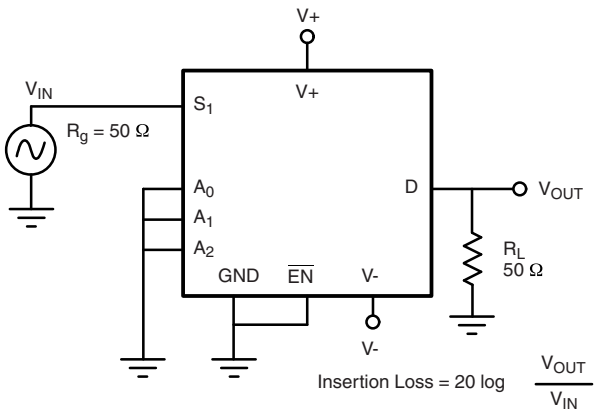


Figure 7. Insertion Loss

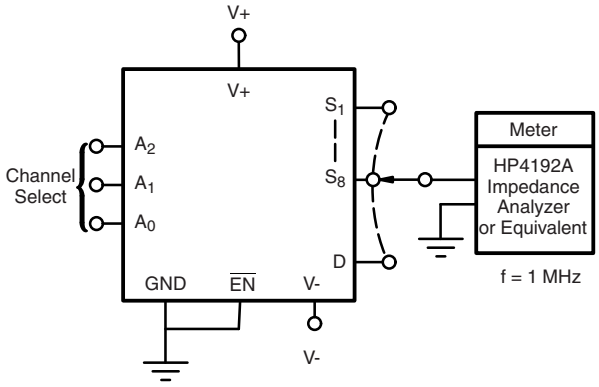
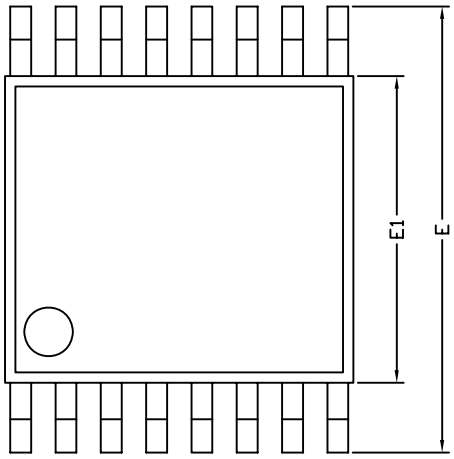
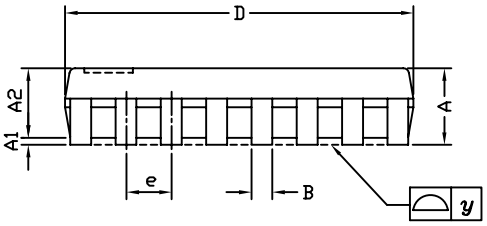


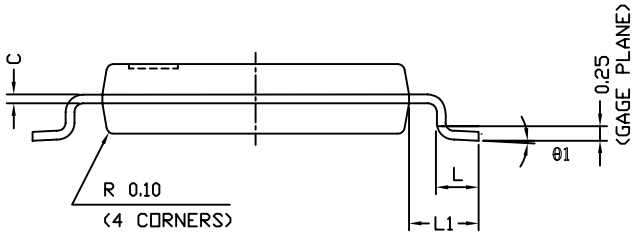
Figure 8. Source Drain Capacitance

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73410.

TSSOP: 16-LEAD

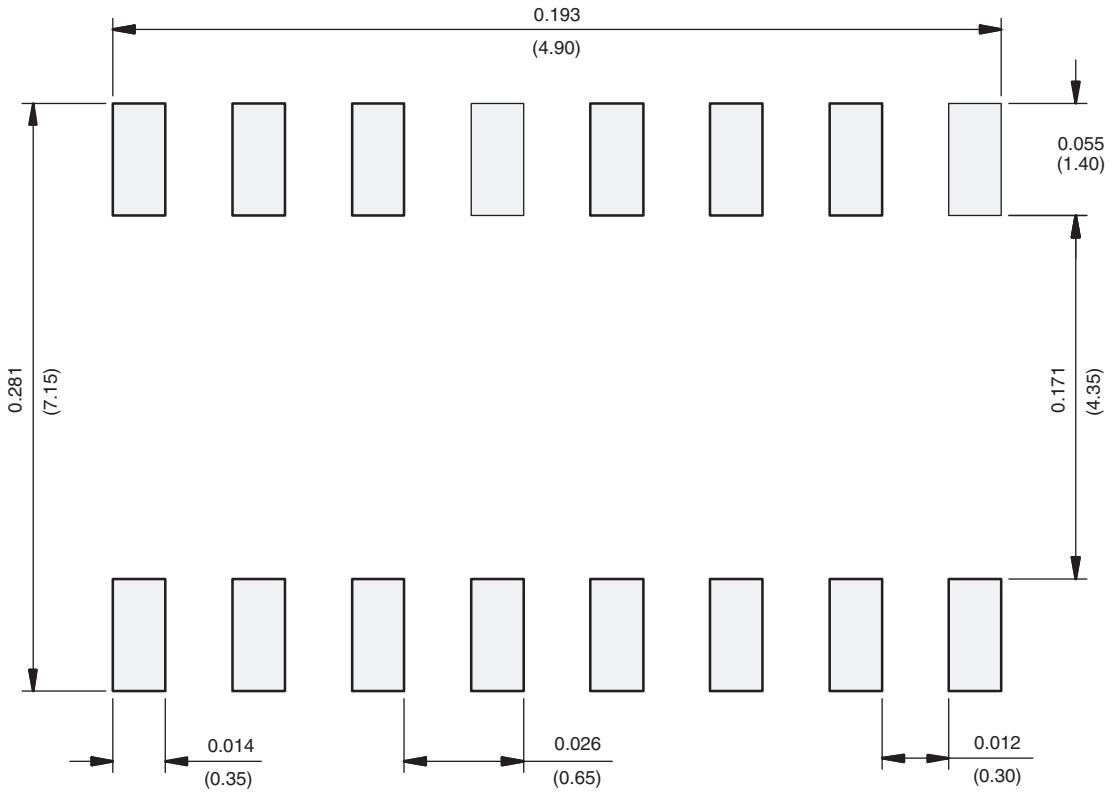






Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



Recommended Minimum Pads
Dimensions in inches (mm)

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