

Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	250
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$ 0.28
Q_g max. (nC)	68
Q_{gs} (nC)	11
Q_{gd} (nC)	35
Configuration	Single

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

ORDERING INFORMATION			
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHF644S-GE3	SiHF644STRL-GE3 ^a	SiHF644STRR-GE3 ^a
Lead (Pb)-free	IRF644SPbF	IRF644STRLPbF ^a	IRF644STRRPbF ^a

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-source voltage	V_{DS}		250	V
Gate-source voltage	V_{GS}		± 20	
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	14	A
		$T_C = 100\text{ }^\circ\text{C}$	8.5	
Pulsed drain current ^a	I_{DM}		56	W/ $^\circ\text{C}$
Linear derating factor			1.0	
Linear derating factor (PCB mount) ^e			0.025	
Single pulse avalanche energy ^b	E_{AS}		550	mJ
Avalanche current ^a	I_{AR}		14	A
Repetitive avalanche energy ^a	E_{AR}		13	mJ
Maximum power dissipation	$T_C = 25\text{ }^\circ\text{C}$		125	W
	$T_A = 25\text{ }^\circ\text{C}$		3.1	
Peak diode recovery dv/dt ^c	dv/dt		4.8	V/ns
Operating junction and storage temperature range	T_J, T_{stg}		-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d	for 10 s		300	

Notes

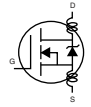

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 4.5\text{ mH}$, $R_g = 25\text{ }^\circ\Omega$, $I_{AS} = 14\text{ A}$ (see fig. 12)
- $I_{SD} \leq 14\text{ A}$, $di/dt \leq 150\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	40	
Maximum junction-to-case (drain)	R_{thJC}	-	1.0	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		250	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.34	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 200\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 8.4\text{ A}^b$	-	-	0.28	Ω
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 8.4\text{ A}^b$		6.7	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	1300	-	pF
Output capacitance	C_{oss}			-	330	-	
Reverse transfer capacitance	C_{rss}			-	85	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 7.9\text{ A}, V_{DS} = 200\text{ V}$, see fig. 6 and 13 ^b	-	-	68	nC
Gate-source charge	Q_{gs}			-	-	11	
Gate-drain charge	Q_{gd}			-	-	35	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 125\text{ V}, I_D = 7.9\text{ A}, R_g = 9.1\text{ }\Omega, R_D = 8.7\text{ }\Omega$, see fig. 10 ^b		-	11	-	ns
Rise time	t_r			-	24	-	
Turn-off delay time	$t_{d(off)}$			-	53	-	
Fall time	t_f			-	49	-	
Gate input resistance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal drain inductance	L_S			-	7.5	-	
Internal source inductance	R_g	$f = 1\text{ MHz}$, open drain		0.3	-	1.2	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	14	A
Pulsed diode forward current ^a	I_{SM}			-	-	56	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 14\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.8	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 7.9\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	250	500	ns
Body diode reverse recovery charge	Q_{rr}			-	2.3	4.6	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

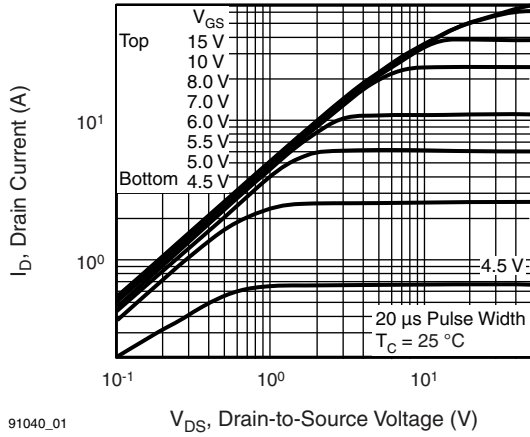


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

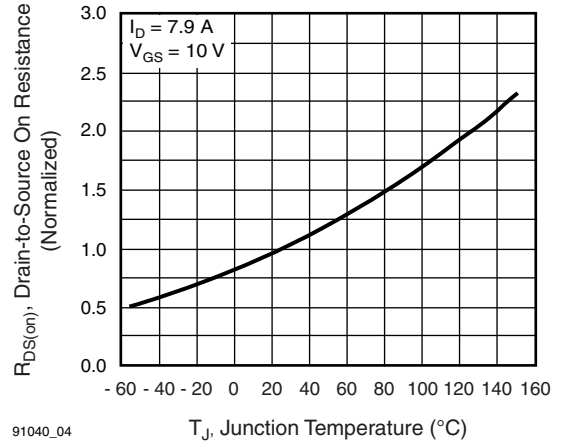


Fig. 4 - Normalized On-Resistance vs. Temperature

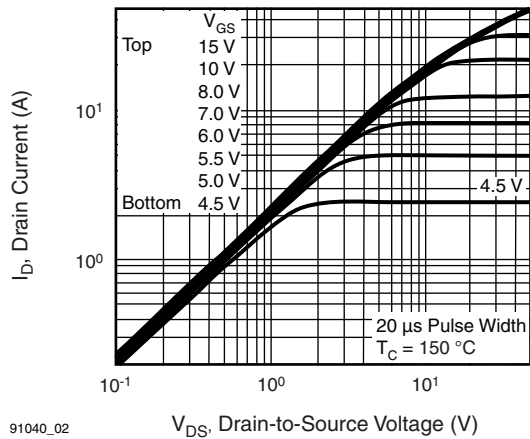


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

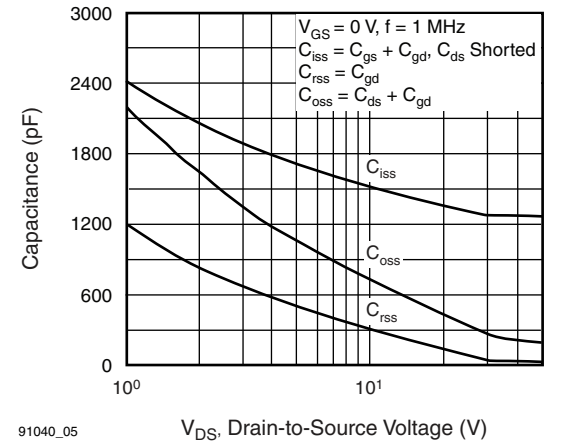


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

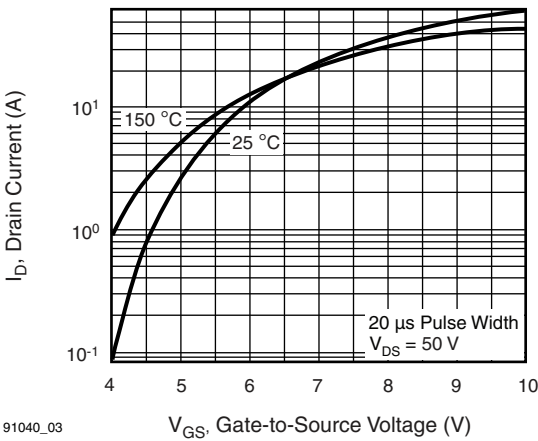


Fig. 3 - Typical Transfer Characteristics

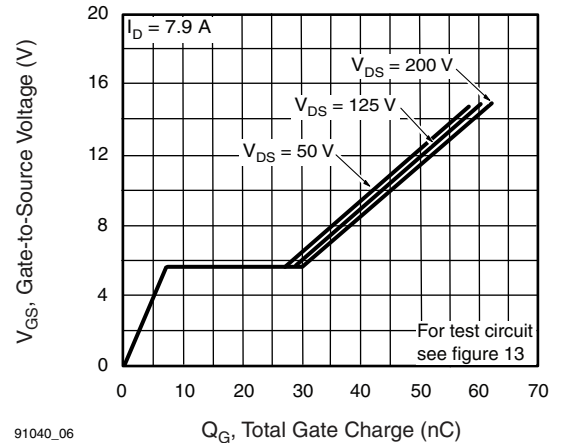


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

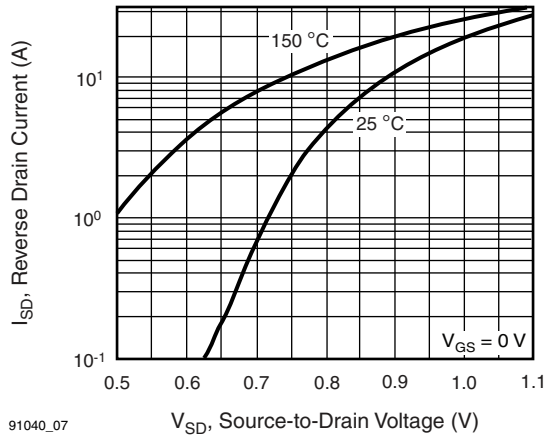


Fig. 7 - Typical Source-Drain Diode Forward Voltage

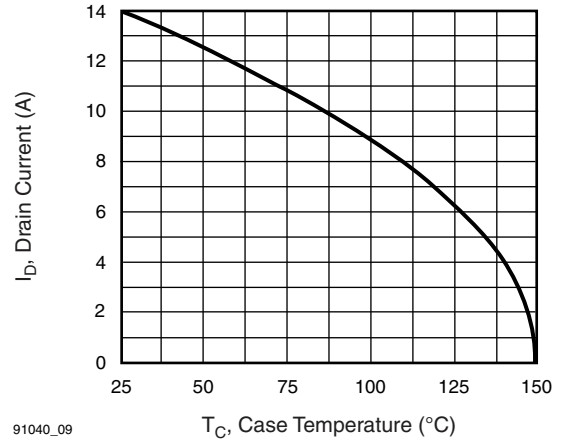


Fig. 9 - Maximum Drain Current vs. Case Temperature

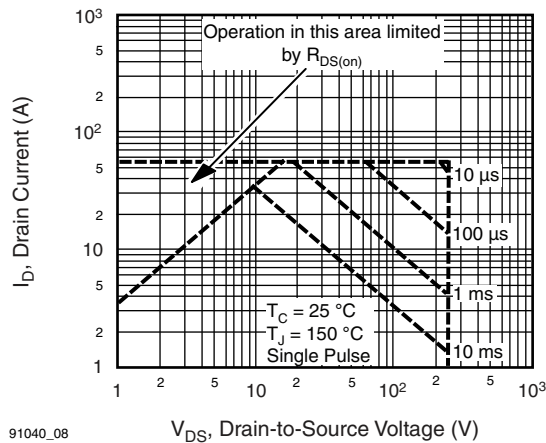


Fig. 8 - Maximum Safe Operating Area

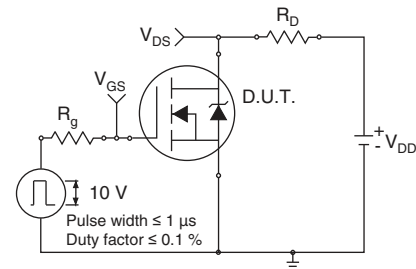


Fig. 10a - Switching Time Test Circuit

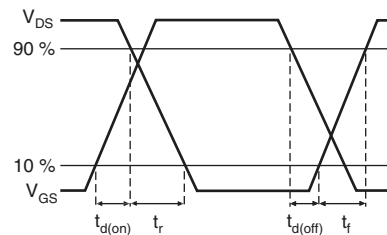


Fig. 10b - Switching Time Waveforms

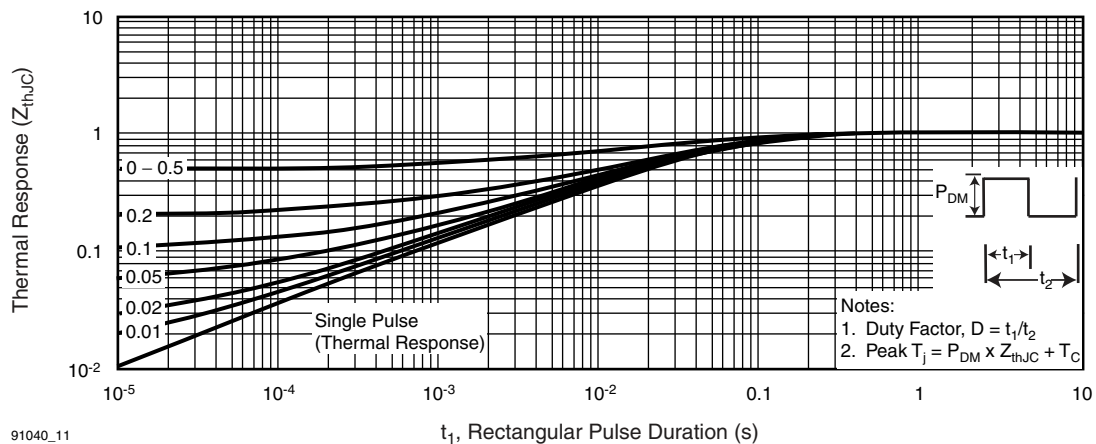


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

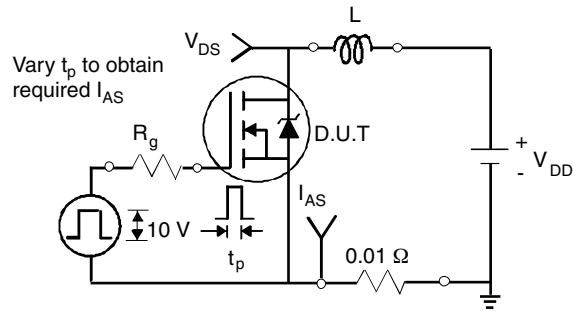


Fig. 12a - Unclamped Inductive Test Circuit

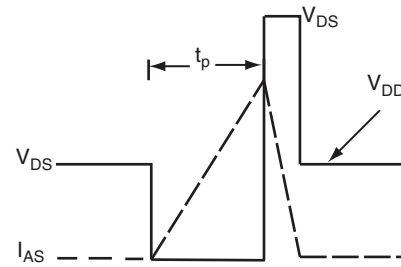


Fig. 12b - Unclamped Inductive Waveforms

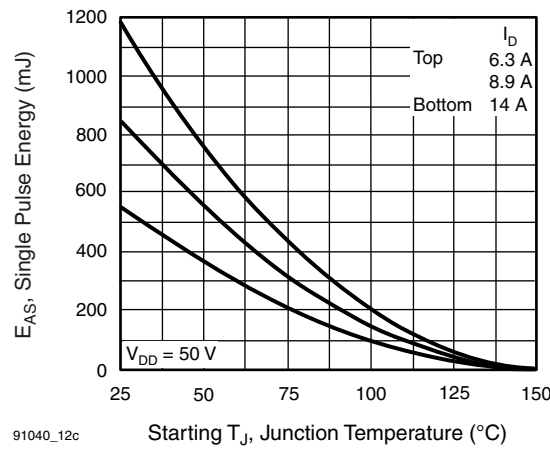


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

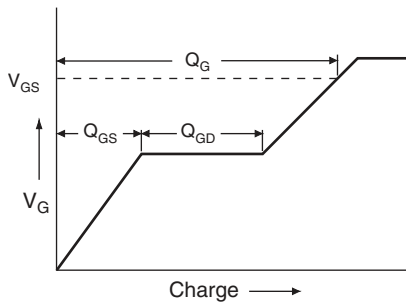


Fig. 13a - Basic Gate Charge Waveform

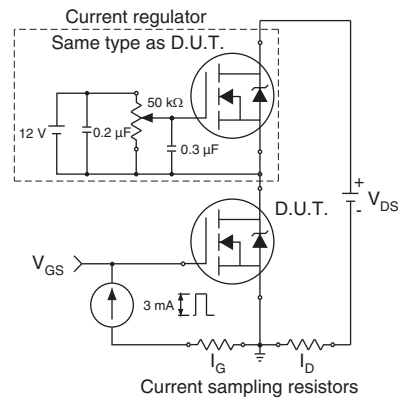
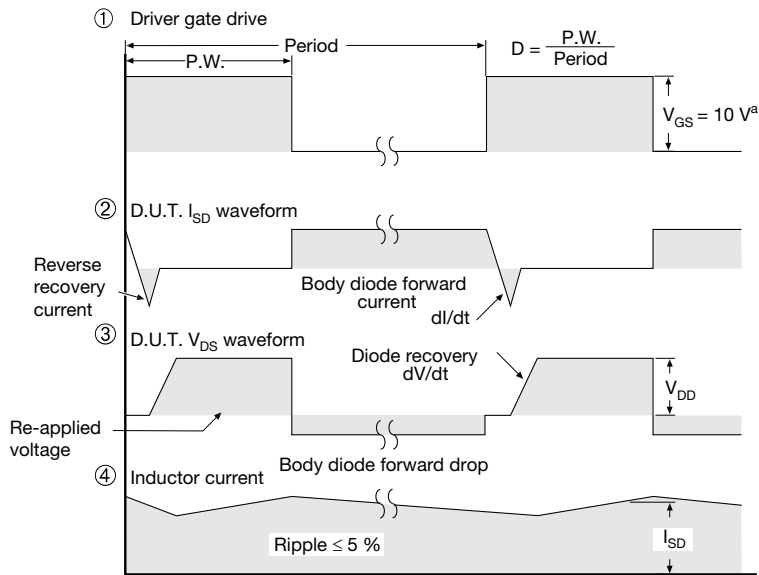
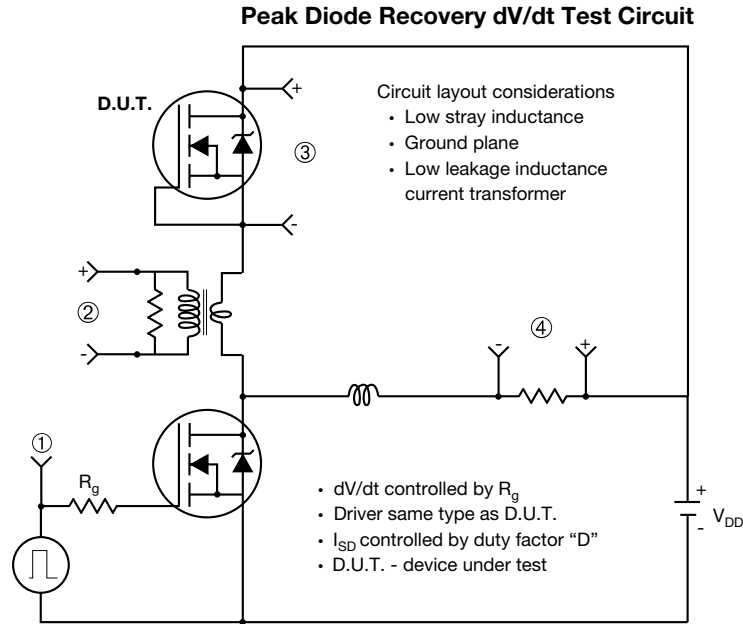


Fig. 13b - Gate Charge Test Circuit



Note
 a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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