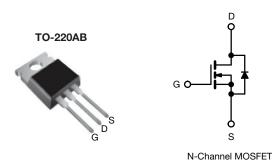
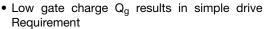
Vishay Siliconix

Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V)	500			
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V 0.28			
Q _g max. (nC)	130			
Q _{gs} (nC)	33			
Q _{gd} (nC)	59			
Configuration	Single			

FEATURES





• Improved gate, avalanche, and dynamic dV/dt ruggedness

RoHS*

- Fully characterized capacitance and avalanche voltage and current
- · Low t_{rr} and soft diode recovery
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- · High speed power switching
- ZVS and high frequency circuit
- · PWM inverters

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	IRFB17N50LPbF

ABSOLUTE MAXIMUM RATINGS (T _C	= 25 °C, unle	ess otherwis	e noted)			
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage		V_{DS}	500			
Gate-source voltage			V_{GS}	± 30	- V	
Continuous drain current	V -140V	$T_{\rm C} = 25 ^{\circ}{\rm C}$ $T_{\rm C} = 100 ^{\circ}{\rm C}$		16	А	
	V _{GS} at 10 V	T _C = 100 °C	ID	11		
Pulsed drain current ^a			I _{DM}	64		
Linear derating factor			1.8	W/°C		
Single pulse avalanche energy b		E _{AS}	390	mJ		
Repetitive avalanche current ^a			I _{AR}	16	А	
Repetitive avalanche energy ^a			E _{AR}	22	mJ	
Maximum power dissipation $T_C = 25 ^{\circ}C$			P_{D}	220	W	
Peak diode recovery dV/dt ^c			dV/dt	13	V/ns	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C		
Soldering recommendations (peak temperature) ^d For 10 s		10 s		300		
Mounting torque	6-32 or M3 screw			10	lbf ⋅ in	
Mounting torque				1.1	N · m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Starting T_J = 25 °C, L = 3.0 mH, R_g = 25 Ω , I_{AS} = 16 A (see fig. 12)
- c. $I_{SD} \le 16$ A, $dI/dt \le 347$ A/ μ s, $V_{DD} \le V_{DS}$, $T_J \le 150$ °C
- d. 1.6 mm from case



Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R _{thJA}	-	62		
Case-to-sink, flat, greased surface	R _{thCS}	0.50	-	°C/W	
Maximum junction-to-case (drain)	R _{thJC}	-	0.56		

PARAMETER	SYMBOL	TES	ST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static					•		
Drain-source breakdown voltage	V _{DS}	V _{GS}	= 0 V, I _D = 250 μA	500	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I _D = 1 mA	-	0.6	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} :	= V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V		-	_	± 100	nA
Zava gata valtaga dvain avvvant		V _{DS} :	= 500 V, V _{GS} = 0 V	-	-	50	μΑ
Zero gate voltage drain current	I _{DSS}	$V_{DS} = 400 \text{V}$	$V, V_{GS} = 0 V, T_{J} = 125 ^{\circ}C$	-	-	2.0	mA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 9.9 A ^b	-	0.28	0.32	Ω
Forward transconductance	9 _{fs}	V _{DS} :	= 50 V, I _D = 9.9 A ^b	11	-	-	S
Dynamic							
Input capacitance	C_{iss}		$V_{GS} = 0 V$	-	2760	-	
Output capacitance	C _{oss}	$V_{DS} = 25 \text{ V},$		-	325	-	1
Reverse transfer capacitance	C_{rss}	f = 1	.0 MHz, see fig. 5	-	37	-	nE
Output conscitance	0	$V_{GS} = 0 V$	$V_{DS} = 1.0 \text{ V}$, f = 1.0 MHz	-	3690	-	V V/°C V nA μA mA
Output capacitance	C _{oss}	$V_{GS} = 0 V$	V _{DS} = 400 V , f = 1.0 MHz	-	84	-	
Effective output capacitance	C _{oss} eff.	$V_{GS} = 0 V$	$V_{DS} = 0 \text{ V to } 400 \text{ V}^{\text{ c}}$	-	159	-	
Total gate charge	Qg		1 10 1 1/ 100 1/	-	-	130	
Gate-source charge	Q_gs	V _{GS} = 10 V	$I_D = 16 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 b	-	-	33	nC
Gate-drain charge	Q_{gd}		ground to	-	-	59	
Turn-on delay time	t _{d(on)}			-	21	-	
Rise time	t _r	V _{DD} :	= 250 V, I _D = 16 A,	-	51	-	ne
Turn-off delay time	$t_{d(off)}$	$V_{DD} = 250 \text{ V, } I_D = 16 \text{ A,}$ $R_g = 7.5 \Omega$, see fig. 10 b - 50		-	115		
Fall time	t _f	$H_{g} = 7.5 \Omega$, see fig. 10 $^{\circ}$ $ 0.50 0.50 0.50 0.50 0.50 0.50 0.50 -$					
Gate input resistance	R_{g}	f = 1	MHz, open drain	0.3	-	1.4	Ω
Drain-Source Body Diode Characteristic	cs						
Continuous source-drain diode current	I_S	MOSFET sym	bol	-	-	16	
Pulsed diode forward current ^a	I _{SM}	showing the integral revers p - n junction	ا کا لیا ہے۔ ان میں ان	-	-	64	А
Body diode voltage	V _{SD}	T _J = 25 °C	C, I _S = 16 A, V _{GS} = 0 V b	-	-	1.5	V
Dadie die de verseure verse de l'acc		T _J = 25 °C	-	-	170	250	
Body diode reverse recovery time	t _{rr}	T _J = 125 °C			220	330	ns
	Q _{rr}	T _J = 25 °C			470	710	r.C
Body diode reverse recovery charge		T _J = 125 °C]	-	810	1210	nC
Reverse recovery current	I _{RRM}		•	-	7.3	11	Α
Forward turn-on time	t _{on}	Intrinsic tu	ırn-on time is negligible (turn-	on is don	ninated b	y L _S and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

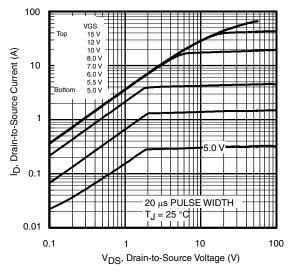


Fig. 1 - Typical Output Characteristics

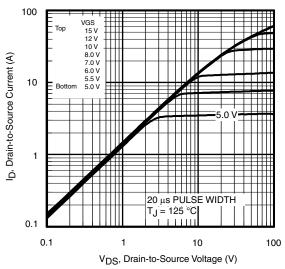


Fig. 2 - Typical Output Characteristics

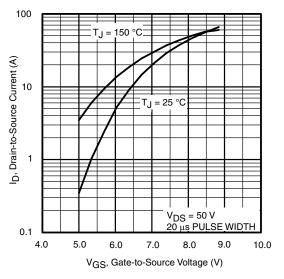


Fig. 3 - Typical Transfer Characteristics

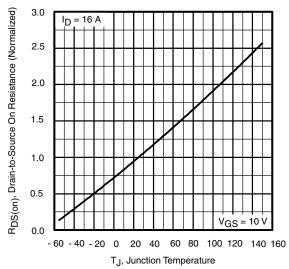


Fig. 4 - Normalized On-Resistance vs. Temperature



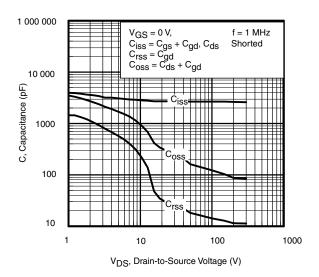


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

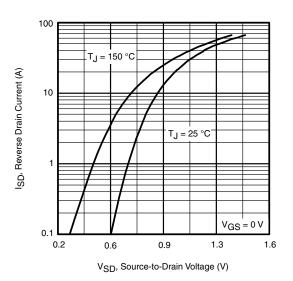


Fig. 7 - Typical Source-Drain Diode Forward Voltage

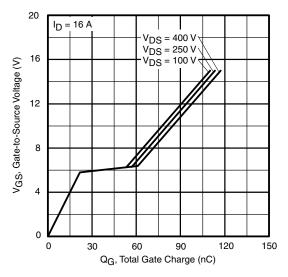


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

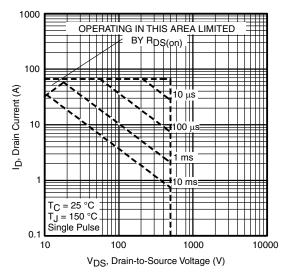


Fig. 8 - Maximum Safe Operating Area



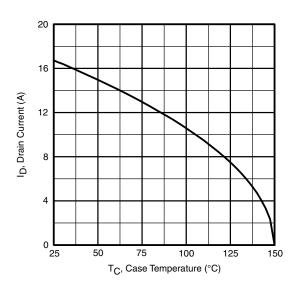


Fig. 9 - Maximum Drain Current vs. Case Temperature

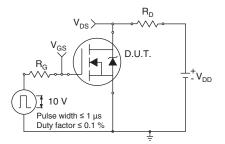


Fig. 10a - Switching Time Test Circuit

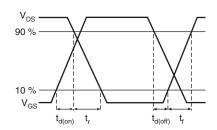


Fig. 10b - Switching Time Waveforms

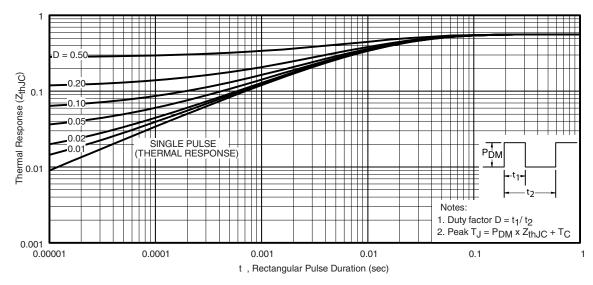


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

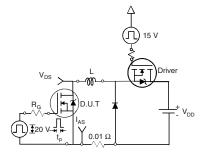


Fig. 12a - Unclamped Inductive Test Circuit

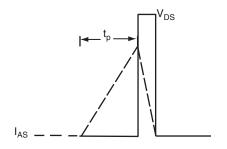


Fig. 12b - Unclamped Inductive Waveforms



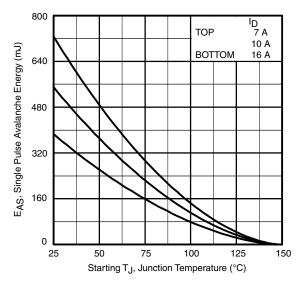


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

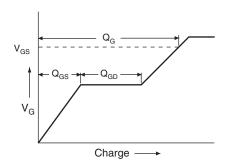


Fig. 13a - Basic Gate Charge Waveform

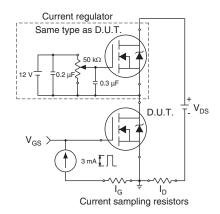
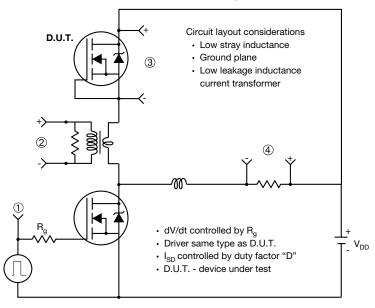


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



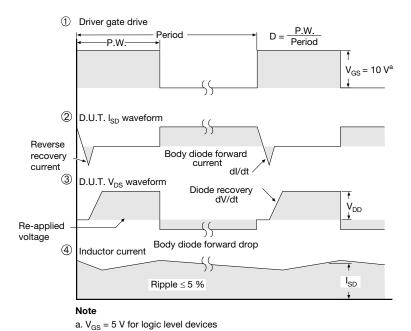


Fig. 14 - For N-Channel

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TO-220-1



DIM.	MILLIN	METERS	INCHES		
DIW.	MIN.	MAX.	MIN.	MAX.	
Α	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
Е	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	

Note

 \bullet $M^{\star}=0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



Revison: 14-Dec-15 1 Document Number: 66542



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