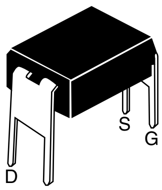
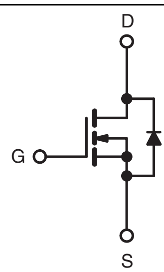
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	50	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.10
Q_g (Max.) (nC)	24	
Q_{gs} (nC)	7.1	
Q_{gd} (nC)	7.1	
Configuration	Single	

HVMDIP





N-Channel MOSFET

FEATURES

- For Automatic Insertion
- Compact, End Stackable
- Fast Switching
- Ease of Paralleling
- Excellent Temperature Stability
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS* COMPLIANT

DESCRIPTION

The HVMDIP technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HVMDIP design achieves very low on-state resistance combined with high transconductance and extreme device ruggedness. HVMDIPs feature all of the established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling, and temperature stability of the electrical parameters.
The HVMDIP 4 pin, dual-in-line package brings the advantages of HVMDIPs to high volume applications where automatic PC board insertion is desireable, such as circuit boards for computers, printers, telecommunications equipment, and consumer products. Their compatibility with automatic insertion equipment, low-profile and end stackable features represent the stat-of-the-art in power device packaging.

ORDERING INFORMATION	
Package	HVMDIP
Lead (Pb)-free	IRFD020PbF
	SiHFD020-E3
SnPb	IRFD020
	SiHFD020

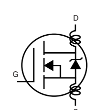
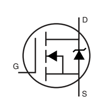
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage[a]			V_{DS}	50	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	2.4	A
		T_C = 100 °C		1.5	
Pulsed Drain Current[b]			I_{DM}	19	
Linear Derating Factor				0.0080	W/°C
Inductive Current, Clamped	L = 100 µH		I_{LM}	19	A
Unclamped Inductive Current (Avalanche Current)[c]			I_L	2.2	
Maximum Power Dissipation	T_C = 25 °C		P_D	1.0	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes
a. T_J = 25 °C to 150 °C
b. Repetitive rating; pulse width limited by maximum junction temperature.
c. V_{DD} = 25 V, starting T_J = 25 °C, L = 100 µH, R_g = 25 Ω
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V		-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = max. rating, V_{GS} = 0 V		-	-	250	μA
		V_{DS} = max. rating x 0.8, V_{GS} = 0 V, T_C = 125		-	-	1000	
On-State Drain Current[b]	$I_{D(on)}$	V_{GS} = 10 V	$V_{DS} > I_{D(on)} \times R_{DS(on)}$ max.	2.4	-	-	A
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 1.4 A	-	0.080	0.10	Ω
Forward Transconductance[b]	g_{fs}	V_{DS} = 20 V, I_D = 7.5 A		4.9	7.3	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz		-	400	-	pF
Output Capacitance	C_{oss}			-	260	-	
Reverse Transfer Capacitance	C_{rss}			-	44	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 15 A, V_{DS} = max. rating x 0.8	-	16	24	nC
Gate-Source Charge	Q_{gs}			-	4.7	7.1	
Gate-Drain Charge	Q_{gd}			-	4.7	7.1	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, I_D = 15 A, R_g = 18 Ω, R_D = 1.7 Ω		-	8.7	13	ns
Rise Time	t_r			-	55	83	
Turn-Off Delay Time	$t_{d(off)}$			-	16	24	
Fall Time	t_f			-	26	39	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.4	A
Pulsed Diode Forward Current[c]	I_{SM}			-	-	19	
Body Diode Voltage[a]	V_{SD}	T_C = 25 °C, I_S = 2.4 A, V_{GS} = 0 V		-	-	1.4	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 15 A, dI/dt = 100 A/μs		57	130	310	ns
Body Diode Reverse Recovery Charge	Q_{rr}			0.17	0.34	0.85	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

c. V_{DD} = 25 V, starting T_J = 25 °C, L = 100 μH, R_g = 25 Ω

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

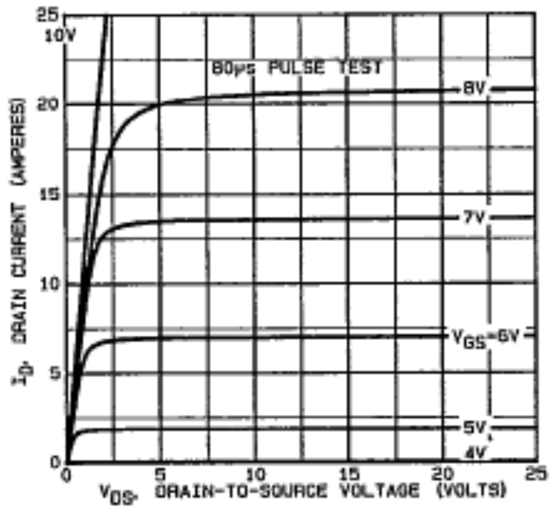


Fig. 1 - Typical Output Characteristics

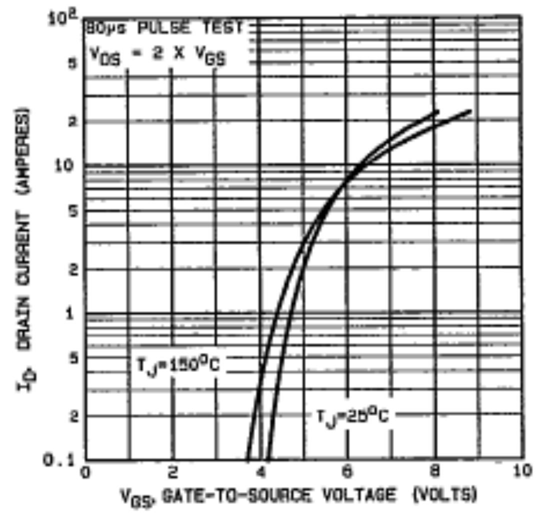


Fig. 3 - Typical Transfer Characteristics

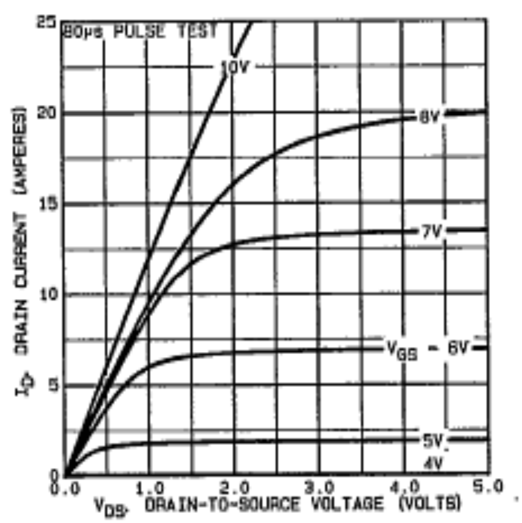


Fig. 2 - Typical Output Characteristics

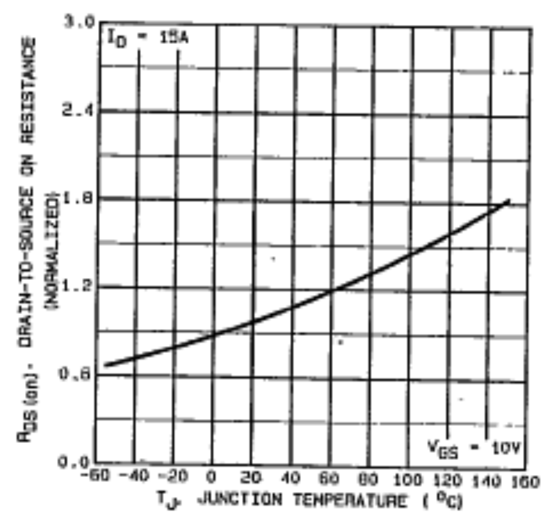


Fig. 4 - Normalized On-Resistance vs. Temperature

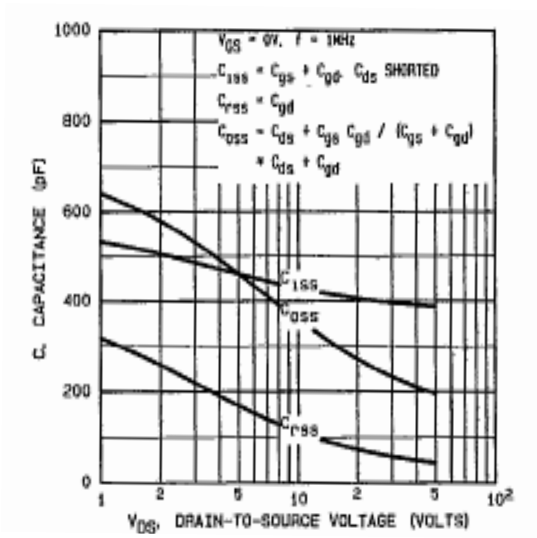


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

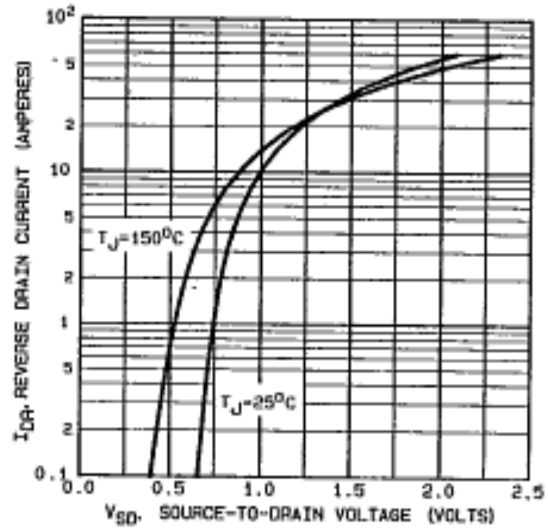


Fig. 7 - Typical Source-Drain Diode Forward Voltage

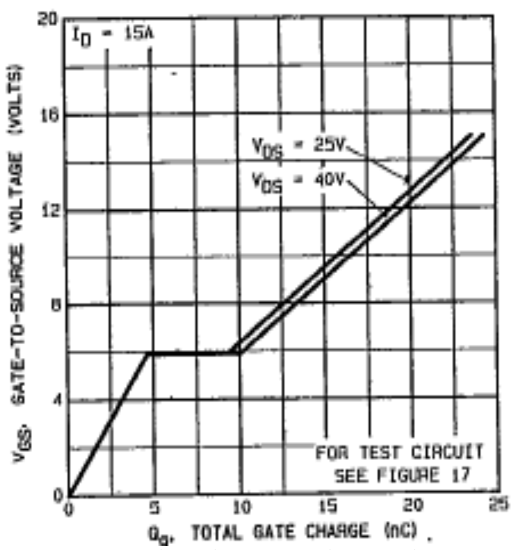


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

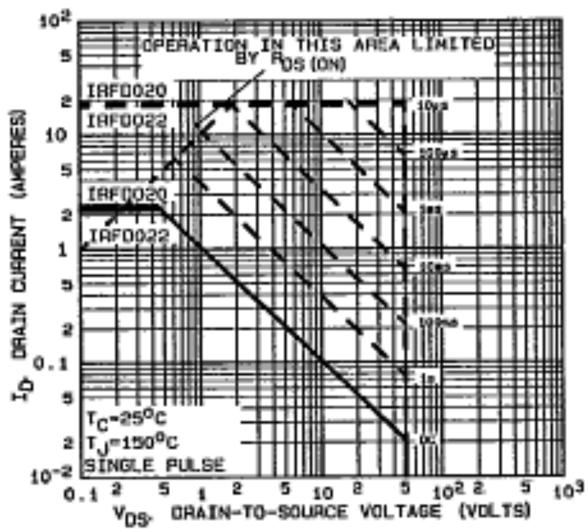


Fig. 8 - Maximum Safe Operating Area

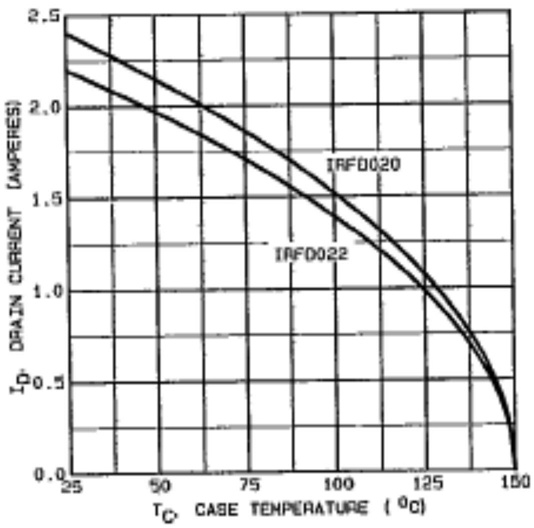


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

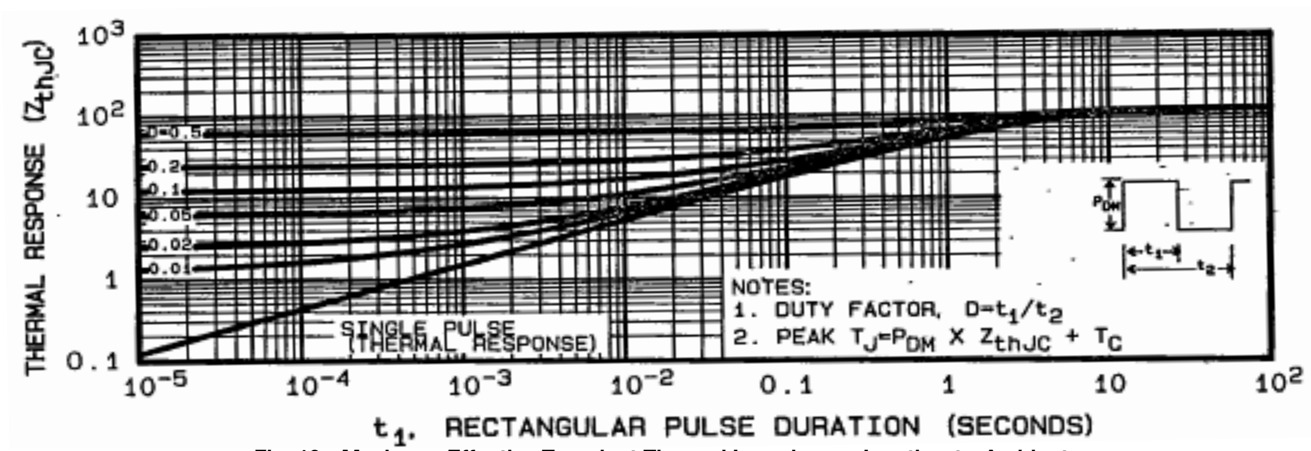


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

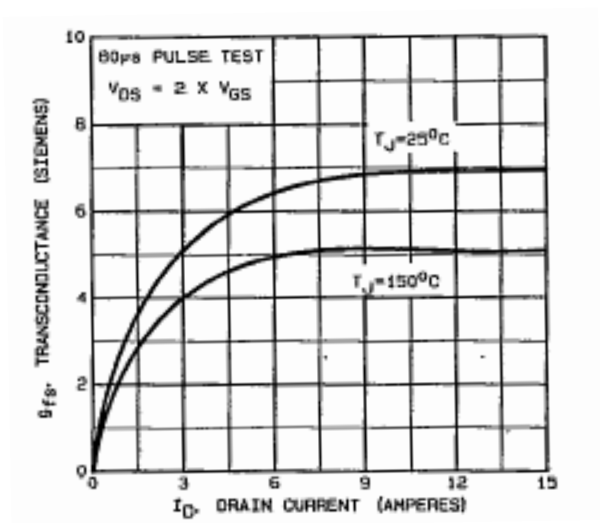


Fig. 11 - Typical Transconductance vs. Drain Current

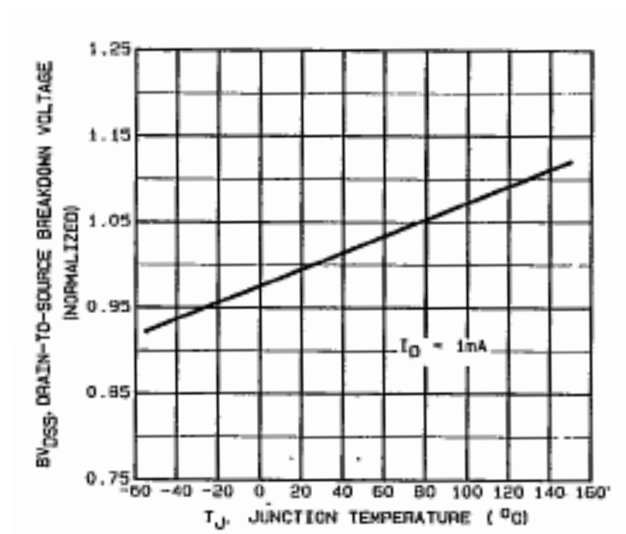


Fig. 12 - Breakdown Voltage vs. Temperature

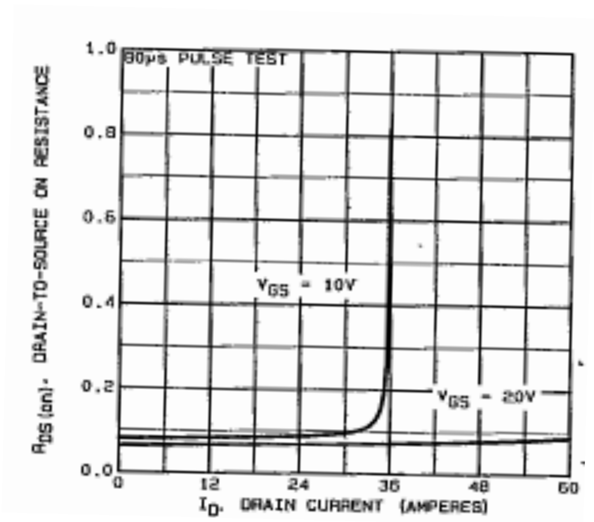


Fig. 13 - Typical on-Resistance vs. Drain Current

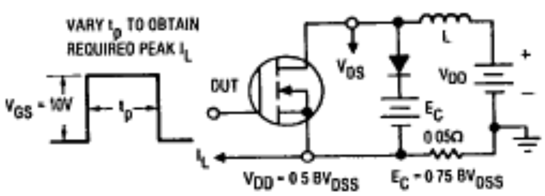


Fig. 14a - Clamped Inductive Test Circuit

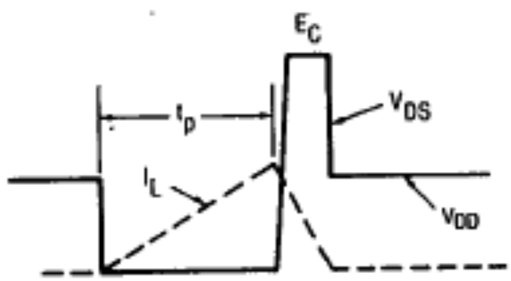


Fig. 14b - Clamped Inductive Waveforms

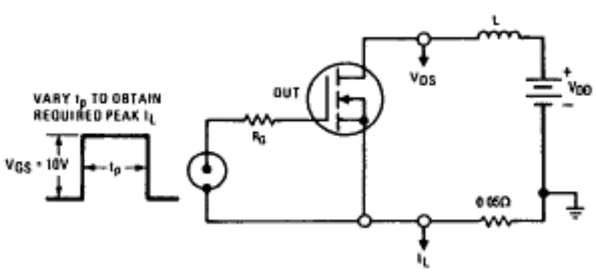


Fig. 15a - Unclamped Inductive Test Circuit

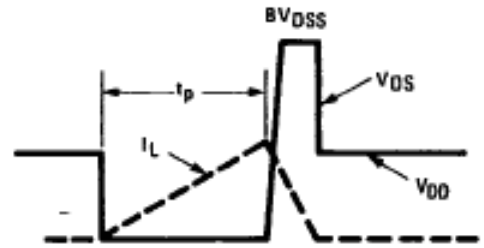


Fig. 15a - Unclamped Inductive Load Test Waveforms

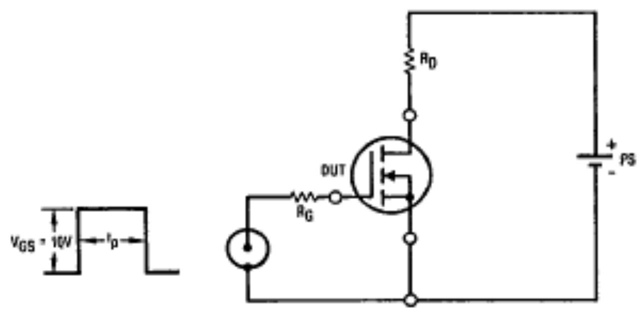


Fig. 16 - Switching Time Test Circuit

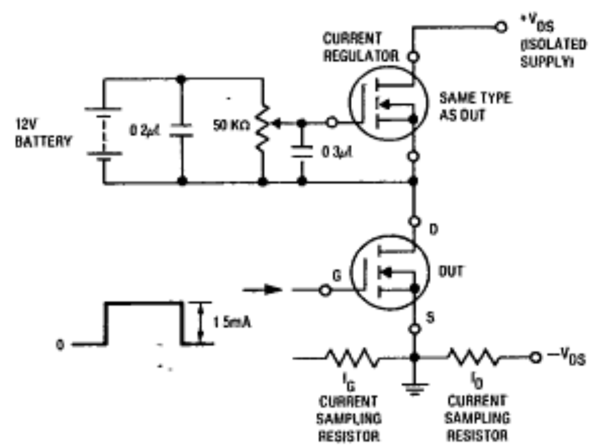


Fig. 17 - Gate Charge Test Circuit

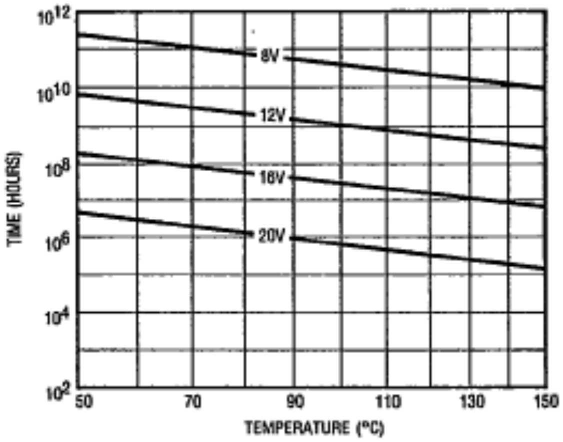


Fig. 18 - Typical Time to Accumulated 1 % Gate Failure

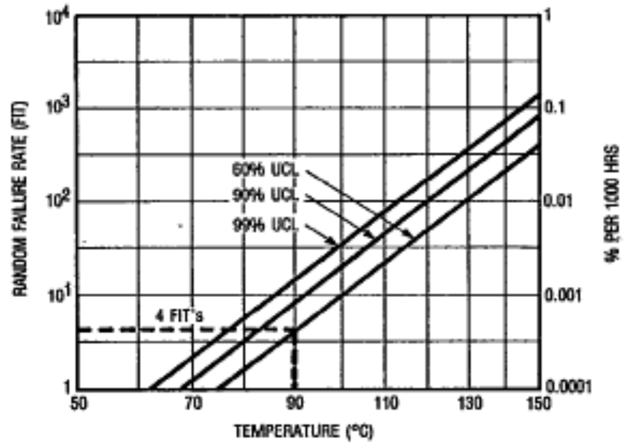


Fig. 19 - Typical High Temperature Reverse Bias (HTRB) Failure Rate

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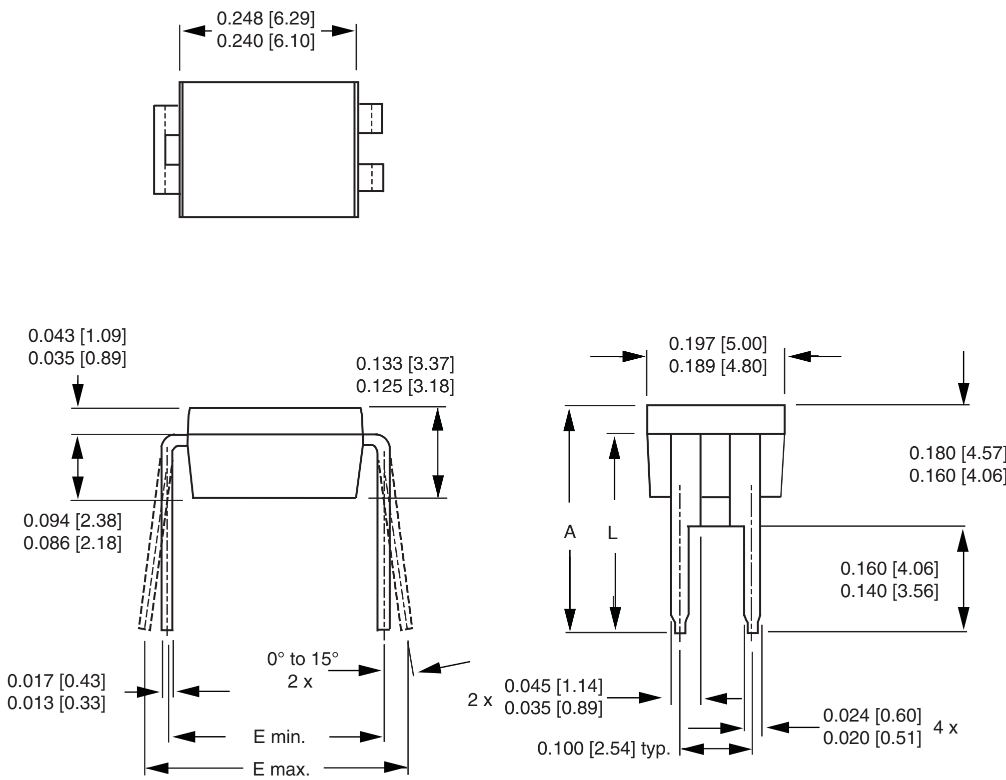
HVM DIP (High voltage)



	INCHES		MILLIMETERS	
DIM.	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36
ECN: X10-0386-Rev. B, 06-Sep-10 DWG: 5974				

Note

1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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