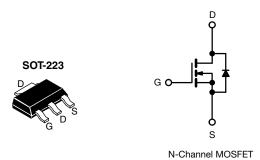


Vishay Siliconix

HALOGEN

FREE

Power MOSFET



Marking code: FC

PRODUCT SUMMA	RY	
V _{DS} (V)	200)
$R_{DS(on)}(\Omega)$	V _{GS} = 10 V	1.5
Q _g (Max.) (nC)	8.2	
Q _{gs} (nC)	1.8	
Q _{gd} (nC)	4.5	
Configuration	Sing	le

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dV/dt rating
- · Repetitive avalanche rated
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOT-223 package is designed for surface-mounting using vapor phase, infrared, or wave soldering techniques. Its unique package design allows for easy automatic pick-and-place as with other SOT or SOIC packages but has the added advantage of improved thermal performance due to an enlarged tab for heatsinking. Power dissipation of greater than 1.25 W is possible in a typical surface mount application.

ORDERING INFORMATION	
Package	SOT-223
Load (Dh) free and belonen free	SiHFL210TR-GE3 ^a
Lead (Pb)-free and halogen-free	IRFL210TRPbF-BE3 a, b
Lead (Pb)-free	IRFL210TRPbF ^a

Notes

- a. See device orientation
- b. "-BE3" denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS (T_C	= 25 °C, unl	ess otherwis	se noted)			
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-source voltage			V_{DS}	200	.,	
Gate-source voltage			V_{GS}	± 20	V	
Continuous dusin surrent	\/ at 10.\/	T _C = 25 °C T _C = 100 °C	1	0.96		
Continuous drain current	V _{GS} at 10 V	T _C = 100 °C	I _D	0.6	Α	
Pulsed drain current ^a		I _{DM}	7.7			
Linear derating factor				0.025	W/°C	
inear derating factor (PCB mount) e			0.017	VV/-C		
Single pulse avalanche energy b			E _{AS}	50	mJ	
Avalanche current a			I _{AR}	0.96	А	
Repetitive avalanche energy a			E _{AR}	0.31	mJ	
Maximum power dissipation	T _C =	25 °C	Б	3.1	10/	
Maximum power dissipation (PCB mount) e	T _A =	25 °C	P_{D}	2.0	W	
Peak diode recovery dv/dt c		dV/dt	5.0	V/ns		
Operating junction and storage temperature range		T _J , T _{stq} -55 to +150				
Soldering recommendations (peak temperature) d For 10 s		10 s	_	300	°C	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. $V_{DD} = 50$ V, starting $T_J = 25$ °C, L = 81 mH, $R_G = 25$ Ω , $I_{AS} = 0.96$ A (see fig. 12)
- c. $I_{SD} \leq 3.3$ A, $dI/dt \leq 70$ A/µs, $V_{DD} \leq V_{DS}$, $T_{J} \leq 150$ °C
- d. 1.6 mm from case
- e. When mounted on 1" square PCB (FR-4 or G-10 material)

Document Number: 91193



Vishay Siliconix

THERMAL RESISTANCE RAT	INGS				
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mount) ^a	R _{thJA}	-	-	40	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	-	60	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static					L	L	
Drain-source breakdown voltage	V _{DS}	V _{GS} :	= 0 V, I _D = 250 μA	200	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I _D = 1 mA	-	0.30	-	V/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-source leakage	I _{GSS}		V _{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	103 = 11, 103 = 1		25	μΑ		
			/, V _{GS} = 0 V, T _J = 125 °C	-	-	250	<u> </u>
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 0.58 A ^b	-	-	1.5	Ω
Forward transconductance	9 _{fs}	V _{DS} =	= 50 V, I _D = 0.58 A	0.51	-	-	S
Dynamic		1			1	ı	<u> </u>
Input capacitance	C _{iss}	4	$V_{GS} = 0 V$,		140	-	4
Output capacitance	C _{oss}	V _{DS} = 25 V, - 53 f = 1.0 MHz, see fig. 5		-	pF		
Reverse transfer capacitance	C _{rss}	1=1	.0 Miriz, see lig. 5	-	15	-	
Total gate charge	Qg		2 2 A V 160 V	-	-	8.2	
Gate-source charge	Q_{gs}	V _{GS} = 10 V		-	1.8	nC	
Gate-drain charge	Q_gd		Ŭ	-	-	4.5	
Turn-on delay time	t _{d(on)}			-	8.2	-	
Rise time	t _r	$V_{DD} = 100 \text{ V}, I_D = 3.3 \text{ A}, \\ R_g = 24 \ \Omega, R_D = 30 \ \Omega, \text{ see fig. } 10^{\text{ b}}$ - 17 - 14 - 8.9 -		-	ns		
Turn-off delay time	t _{d(off)}			-			
Fall time	t _f			-	8.9	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from		-	-11		
Internal source inductance	L _S	package and die contact	center of	-	6.0	-	– nH
Drain-Source Body Diode Characteristic	es						
Continuous source-drain diode current	I _S	MOSFET symbol showing the		-	=	0.96	A
Pulsed diode forward current ^a	I _{SM}	integral revers p - n junction		-	-	7.7	
Body diode voltage	V _{SD}	T _J = 25 °C,	$I_S = 0.96 \text{ A}, V_{GS} = 0 \text{ V}^{\text{ b}}$	-	-	2.0	V
Body diode reverse recovery time	t _{rr}	T 05 00 1	0.0 4 -11/-14 - 4.00 4 / - 6	-	150	310	ns
Body diode reverse recovery charge	Q _{rr}	$I_J = 25 ^{\circ}\text{C}, I_F$	= 3.3 A, dl/dt = 100 A/µs b	-	0.60	1.4	μC
Forward turn-on time	t _{on}	Intrinsic tu	ırn-on time is negligible (turn	on is dor	ninated b	v L _s and	L _D)

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width \leq 300 µs; duty cycle \leq 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

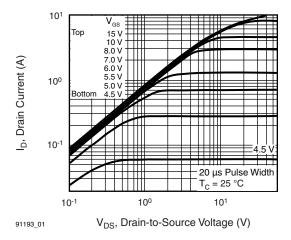


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

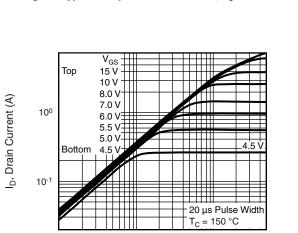


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

V_{DS}, Drain-to-Source Voltage (V)

10⁻¹

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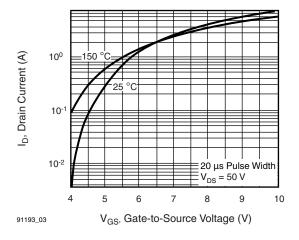


Fig. 3 - Typical Transfer Characteristics

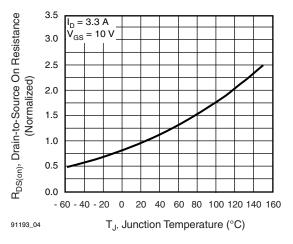


Fig. 4 - Normalized On-Resistance vs. Temperature

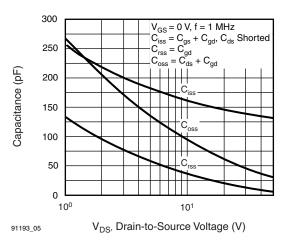


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

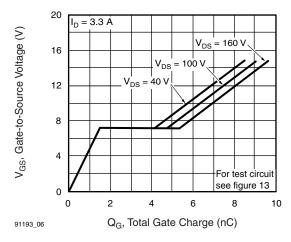


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



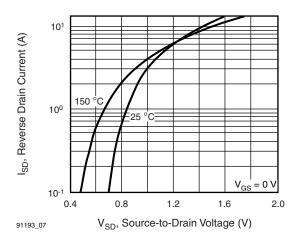


Fig. 7 - Typical Source-Drain Diode Forward Voltage

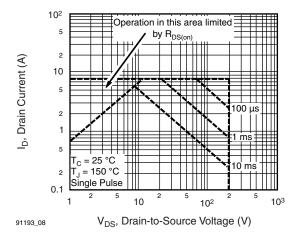


Fig. 8 - Maximum Safe Operating Area

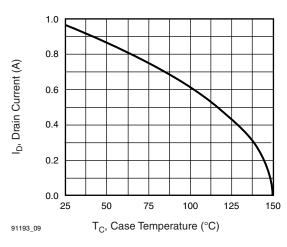


Fig. 9 - Maximum Drain Current vs. Case Temperature

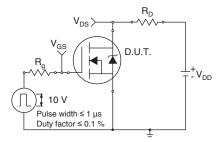


Fig. 10a - Switching Time Test Circuit

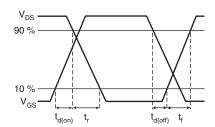


Fig. 10b - Switching Time Waveforms

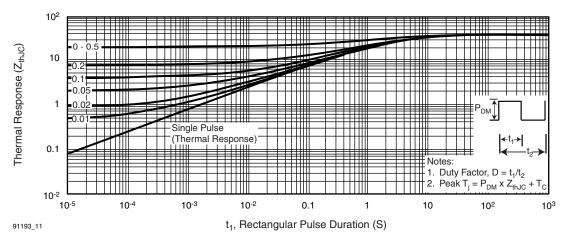


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case



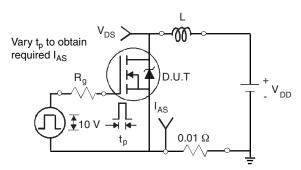


Fig. 12a - Unclamped Inductive Test Circuit

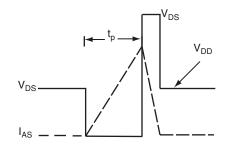


Fig. 12b - Unclamped Inductive Waveforms

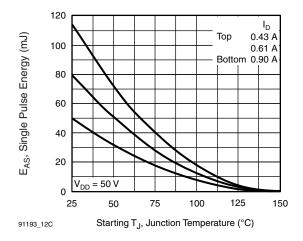


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

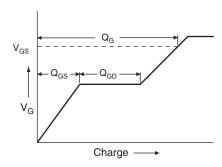


Fig. 13a - Basic Gate Charge Waveform

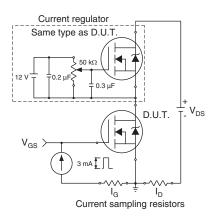
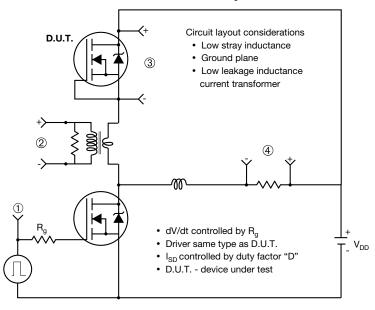


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



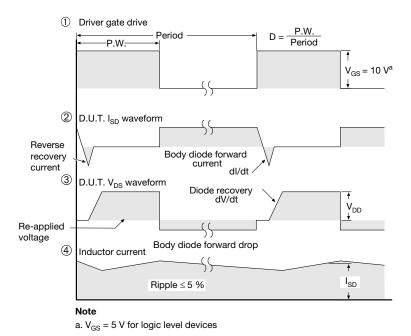


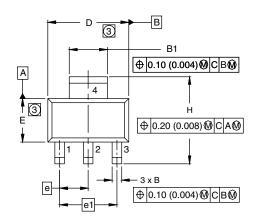
Fig. 14 - For N-Channel

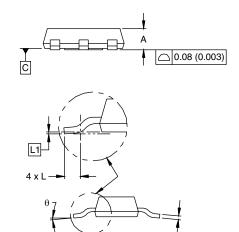
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Vishay Siliconix

SOT-223 (HIGH VOLTAGE)





DIM.	MILLI	METERS	INCHES		
	MIN.	MAX.	MIN.	MAX.	
Α	1.55	1.80	0.061	0.071	
В	0.65	0.85	0.026	0.033	
B1	2.95	3.15	0.116	0.124	
С	0.25	0.35	0.010	0.014	
D	6.30	6.70	0.248	0.264	
E	3.30	3.70	0.130	0.146	
е	2.30 BSC		0.0905 BSC		
e1	4.60	O BSC	0.181	BSC	
Н	6.71	7.29	0.264	0.287	
L	0.91	-	0.036	=	
L1	0.061 BSC		0.0024	BSC	
θ	-	10'	-	10'	

ECN: S-82109-Rev. A, 15-Sep-08

DWG: 5969

Notes

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension do not include mold flash.
- 4. Outline conforms to JEDEC outline TO-261AA.



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