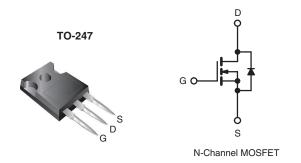


Vishay Siliconix

COMPLIANT

Power MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	500		
$R_{DS(on)}\left(\Omega\right)$	V _{GS} = 10 V 0.27		
Q _g (Max.) (nC)	120		
Q _{gs} (nC)	32		
Q _{gd} (nC)	49		
Configuration	Single		



FEATURES

- · Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30 V V_{GS} Rating
- Reduced C_{iss}, C_{oss}, C_{rss}
- Isolated Central Mounting Hole
- · Dynamic dV/dt Rating
- · Repetitive Avalanche Rated
- Lead (Pb)-free Available

DESCRIPTION

This new series of low charge Power MOSFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing advanced Power MOSFETs technology the device improvements allow for reduced gate drive requirements, faster switching speeds and increased total system savings. These device improvements combined with the proven ruggedness and reliability of Power MOSFETs offer the designer a new standard in power transistors for switching applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because its isolated mounting hole.

ORDERING INFORMATION	
Package	TO-247
Load (Dh) from	IRFP460LCPbF
Lead (Pb)-free	SiHFP460LC-E3
SnPb	IRFP460LC
	SiHFP460LC

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	7 V
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	I _D	20	
Continuous Diam Current	VGS at 10 V	T _C = 100 °C	טי	12	Α
Pulsed Drain Current ^a	•		I _{DM}	80	
Linear Derating Factor				2.2	W/°C
Single Pulse Avalanche Energy ^b			E _{AS}	960	mJ
Repetitive Avalanche Current ^a			I _{AR}	20	Α
Repetitive Avalanche Energy ^a			E _{AR}	28	mJ
Maximum Power Dissipation	T _C =	25 °C	P_{D}	280	W
Peak Diode Recovery dV/dtc			dV/dt	3.5	V/ns
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 150	°C	
Soldering Recommendations (Peak Temperature) for 10 s			300 ^d	1	
Mounting Torque	6 22 or l	M2 corow		10	lbf ⋅ in
Mounting Torque	6-32 or M3 screw			1.1	N⋅m

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. V_{DD} = 25 V, starting T_J = 25 °C, L = 4.3 mH, R_G = 25 Ω , I_{AS} = 20 A (see fig. 12). c. I_{SD} \leq 20 A, dI/dt \leq 160 A/µs, V_{DD} \leq V_{DS}, T_J \leq 150 °C.
- d. 1.6 mm from case.
- * Pb containing terminations are not RoHS compliant, exemptions may apply

IRFP460LC, SiHFP460LC

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THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R _{thJA}	-	-	
Case-to-Sink, Flat, Greased Surface	R _{thCS}	0.24	-	°C/W
Maximum Junction-to-Case (Drain)	R _{thJC}	-	0.45	

SPECIFICATIONS $T_J = 25 ^{\circ}C$,	unless other	wise noted		T			,
PARAMETER	SYMBOL	TEST	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$	V, I _D = 250 μA	500	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference t	to 25 °C, I _D = 1 mA	-	0.59	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V$	' _{GS} , I _D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _G	_S = ± 20 V	-	-	± 100	nA
Zava Cata Valtaga Dvain Current		V _{DS} = 50	00 V, V _{GS} = 0 V	-	-	25	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 400 V, V	/ _{GS} = 0 V, T _J = 125 °C	-	-	250	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 12 A ^b	-	-	0.27	Ω
Forward Transconductance	9 _{fs}	V _{DS} = 5	50 V, I _D = 12 A ^b	12	-	-	S
Dynamic					•	•	
Input Capacitance	C _{iss}	V	r _{GS} = 0 V,	-	3600	-	
Output Capacitance	C _{oss}	V	os = 25 V,	-	440	-	pF
Reverse Transfer Capacitance	C _{rss}	f = 1.0	f = 1.0 MHz, see fig. 5		39	-	1
Total Gate Charge	Qg			-	-	120	
Gate-Source Charge	Q_{gs}	V _{GS} = 10 V	$I_D = 20 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 ^b	-	-	32	nC
Gate-Drain Charge	Q _{gd}		See lig. 6 and 16	-	-	49	
Turn-On Delay Time	t _{d(on)}			-	18	-	
Rise Time	t _r	$V_{DD} = 2$	250 V, I _D = 20 A	-	77	-]]
Turn-Off Delay Time	t _{d(off)}	$R_G = 4.3 \Omega$, $R_D = 12 \Omega$, see fig. 10^b		-	40	-	ns
Fall Time	t _f			-	43	-	-
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") fro	om (-	5.0	-	
Internal Source Inductance	L _S	package and ce die contact	nter of	-	13	-	nH
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	MOSFET symbo	MOSFET symbol		-	20	_
Pulsed Diode Forward Current ^a	I _{SM}	integral reverse p - n junction diode		-	-	80	A
Body Diode Voltage	V _{SD}	T _J = 25 °C, I ₅	_S = 20 A, V _{GS} = 0 V ^b	-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T 05 00 1	00 A dI/d+ 400 A/h	-	570	860	ns
Body Diode Reverse Recovery Charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}, I_F = 20 \text{A}, \text{dI/dt} = 100 \text{A/}\mu\text{s}^b$		-	6.6	9.9	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)			L _D)		

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11). b. Pulse width \leq 300 μ s; duty cycle \leq 2 %.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

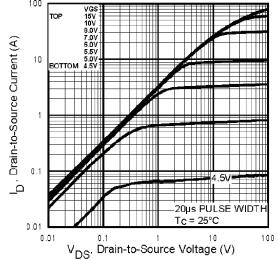


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

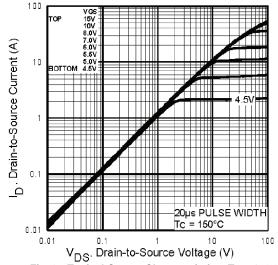


Fig. 2 - Typical Output Characteristics, T_C = 150 °C

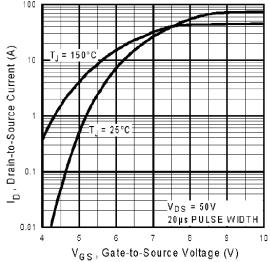


Fig. 3 - Typical Transfer Characteristics

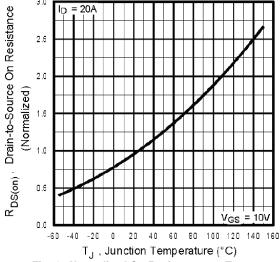


Fig. 4 - Normalized On-Resistance vs. Temperature

IRFP460LC, SiHFP460LC

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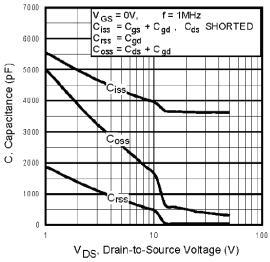


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

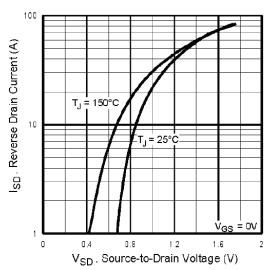


Fig. 7 - Typical Source-Drain Diode Forward Voltage

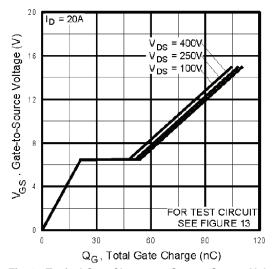


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

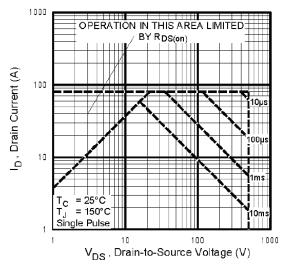


Fig. 8 - Maximum Safe Operating Area



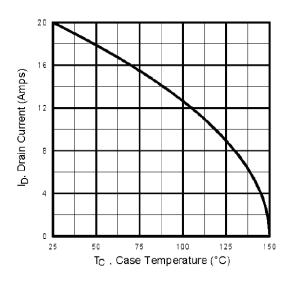


Fig. 9 - Maximum Drain Current vs. Case Temperature

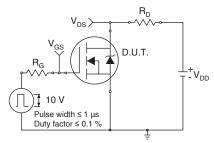


Fig. 10a - Switching Time Test Circuit

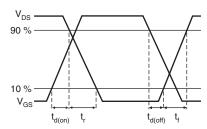


Fig. 10b - Switching Time Waveforms

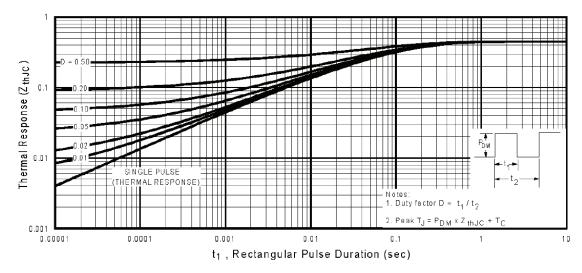


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

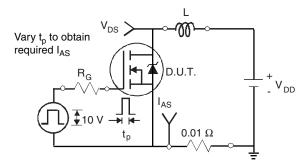


Fig. 12a - Unclamped Inductive Test Circuit

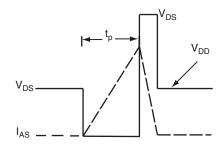


Fig. 12b - Unclamped Inductive Waveforms

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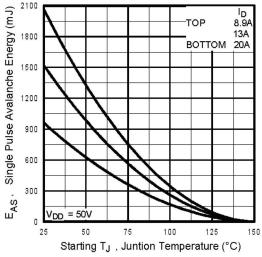


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

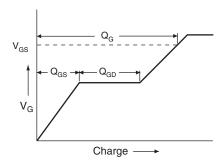


Fig. 13a - Basic Gate Charge Waveform

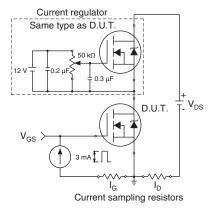
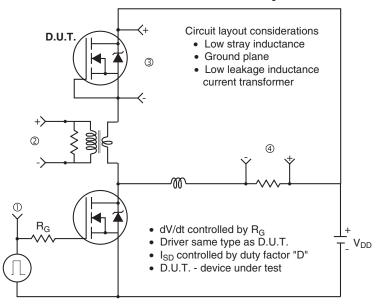
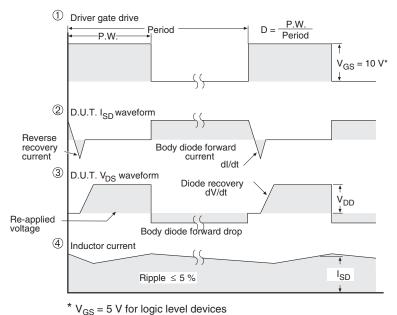


Fig. 13b - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit





o v for logic level devices

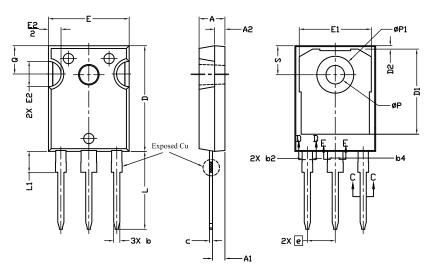
Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?91235.

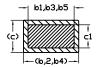


TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9







Section C--C,D--D,E--E

	MILLIN	IETERS	
DIM.	MIN.	MAX.	NOTES
Α	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
С	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
е	5.44	BSC	
L	14.90	15.40	
L1	3.96	4.16	6
ØΡ	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	
L		I	1

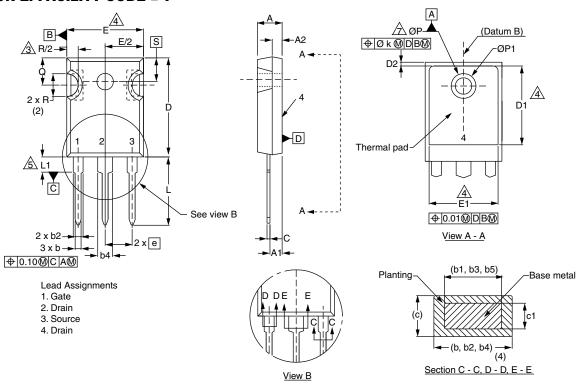
Notes

- (1) Package reference: JEDEC® TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition

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VERSION 2: FACILITY CODE = Y



	MILLIMETERS		
DIM.	MIN.	MAX.	NOTES
Α	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
С	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

	MILLIN		
DIM.	MIN.	MAX.	NOTES
D2	0.51	1.30	
Е	15.29	15.87	
E1	13.72	-	
е	5.46	BSC	
Øk	0.254		
L	14.20	16.25	
L1	3.71	4.29	
ØР	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

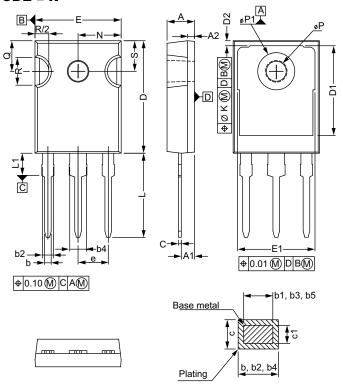
Notes

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c

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VERSION 3: FACILITY CODE = N



	MILLIM	IETERS
DIM.	MIN.	MAX.
Α	4.65	5.31
A1	2.21	2.59
A2	1.17	1.37
b	0.99	1.40
b1	0.99	1.35
b2	1.65	2.39
b3	1.65	2.34
b4	2.59	3.43
b5	2.59	3.38
С	0.38	0.89
c1	0.38	0.84
D	19.71	20.70
D1	13.08	-

	MILLIMETERS		
DIM.	MIN.	MAX.	
D2	0.51	1.35	
E	15.29	15.87	
E1	13.46	-	
е	5.46	BSC	
k	0.254		
L	14.20	16.10	
L1	3.71	4.29	
N	7.62 BSC		
Р	3.56	3.66	
P1	=	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E20-0545-Rev. F, 19-Oct-2020

DWG: 5971

Notes

- ⁽¹⁾ Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")



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