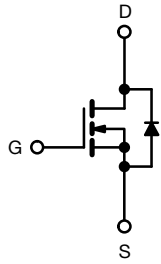
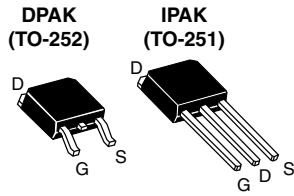


Power MOSFET



N-Channel MOSFET

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- Power factor correction

TYPICAL SMPS TOPOLOGIES

- Low power single transistor flyback

PRODUCT SUMMARY	
V_{DS} (V)	600
$R_{DS(on)}$ max. (Ω)	$V_{GS} = 10\text{ V}$ 7.0
Q_g max. (nC)	14
Q_{gs} (nC)	2.7
Q_{gd} (nC)	8.1
Configuration	Single

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFR1N60A-GE3	SiHFR1N60ATRL-GE3 ^a	SiHFR1N60ATR-GE3 ^a	SiHFU1N60A-GE3
	IRFR1N60APbF-BE3 ^{ab}	IRFR1N60ATRPbF-BE3 ^{ab}	SiHFR1N60ATRR-GE3 ^a	-
Lead (Pb)-free	IRFR1N60APbF	IRFR1N60ATRLPbF ^a	IRFR1N60ATRPbF ^a	IRFU1N60APbF

Notes

- See device orientation
- “-BE3” denotes alternate manufacturing location

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL		LIMIT	UNIT	
Drain-source voltage	V_{DS}		600	V	
Gate-source voltage	V_{GS}		± 30		
Continuous drain current	V_{GS} at 10 V	$T_C = 25\text{ }^\circ\text{C}$	1.4	A	
		$T_C = 100\text{ }^\circ\text{C}$	0.89		
Pulsed drain current ^a	I_{DM}		5.6		
Linear derating factor			0.28	W/ $^\circ\text{C}$	
Single pulse avalanche energy ^b	E_{AS}		93	mJ	
Repetitive avalanche current ^a	I_{AR}		1.4	A	
Repetitive avalanche energy ^a	E_{AR}		3.6	mJ	
Maximum power dissipation	$T_A = 25\text{ }^\circ\text{C}$		P_D	36	W
Peak diode recovery dV/dt ^c	dV/dt		3.8	V/ns	
Operating junction and storage temperature range	T_J, T_{stg}		-55 to +150	$^\circ\text{C}$	
Soldering recommendations (peak temperature) ^d	for 10 s		300		

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 95\text{ mH}$, $R_g = 25\text{ }^\circ\Omega$, $I_{AS} = 1.4\text{ A}$ (see fig. 12)
- $I_{SD} \leq 1.4\text{ A}$, $dI/dt \leq 180\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	110	°C/W
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	50	
Maximum junction-to-case (drain)	R_{thJC}	-	3.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	600	-	-	V	
V_{DS} temperature coefficient	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0		
Gate-source threshold voltage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$	-	-	± 100	nA	
Gate-source leakage	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA	
Zero gate voltage drain current		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250		
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 0.84\text{ A}^b$	-	-	7.0	Ω	
Drain-source on-state resistance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 0.84\text{ A}$	0.88	-	-	S	
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5	-	229	-	pF	
Output capacitance	C_{oss}		-	32.6	-		
Reverse transfer capacitance	C_{rss}		-	2.4	-		
Output capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	320	-	
Effective output capacitance			$C_{oss\text{ eff.}}$	$V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$	-	11.5	-
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 1.4\text{ A}, V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	14	nC
Gate-source charge	Q_{gs}			-	-	2.7	
Gate-drain charge	Q_{gd}			-	-	8.1	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 1.4\text{ A}, R_g = 2.15\text{ }\Omega, R_D = 178\text{ }\Omega$, see fig. 10 ^b	-	9.8	-	ns	
Rise time	t_r		-	14	-		
Turn-off delay time	$t_{d(off)}$		-	18	-		
Fall time	t_f		-	20	-		
Drain-source body diode characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	1.4	A	
Pulsed diode forward current ^a	I_{SM}		-	-	5.6		
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 1.4\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	1.6	V	
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 1.4\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	290	440	ns	
Body diode reverse recovery charge	Q_{rr}		-	510	760	μC	
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

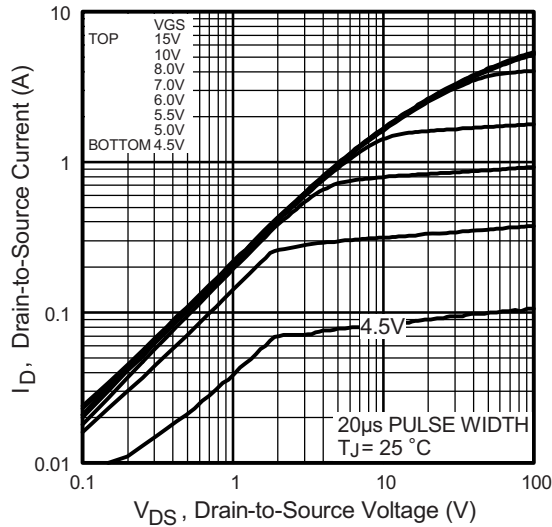


Fig. 1 - Typical Output Characteristics

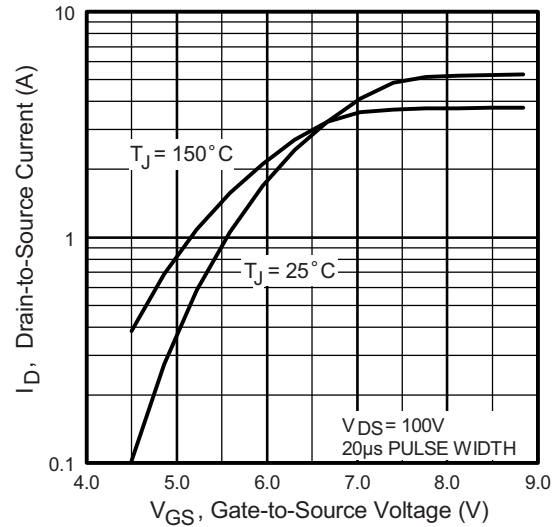


Fig. 2 - Typical Transfer Characteristics

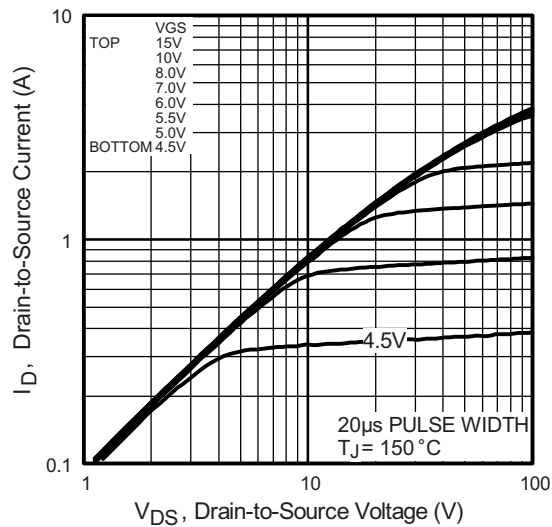


Fig. 1 - Typical Output Characteristics

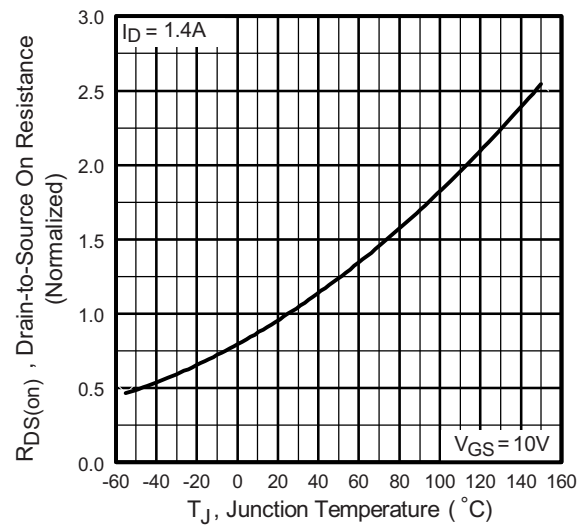


Fig. 3 - Normalized On-Resistance vs. Temperature

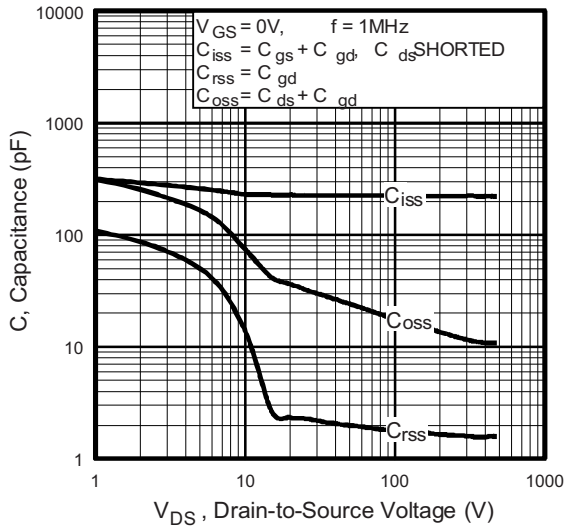


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

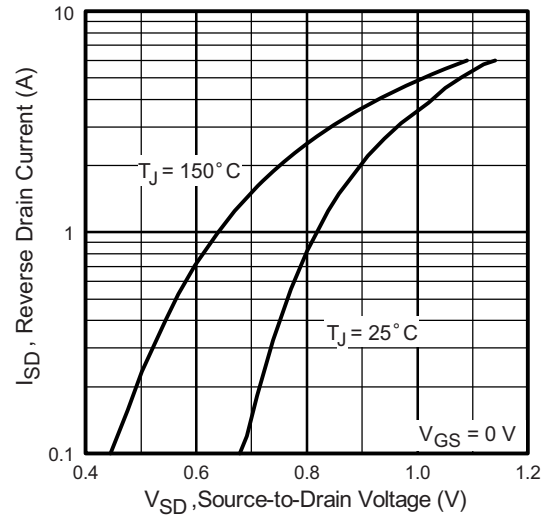


Fig. 6 - Typical Source-Drain Diode Forward Voltage

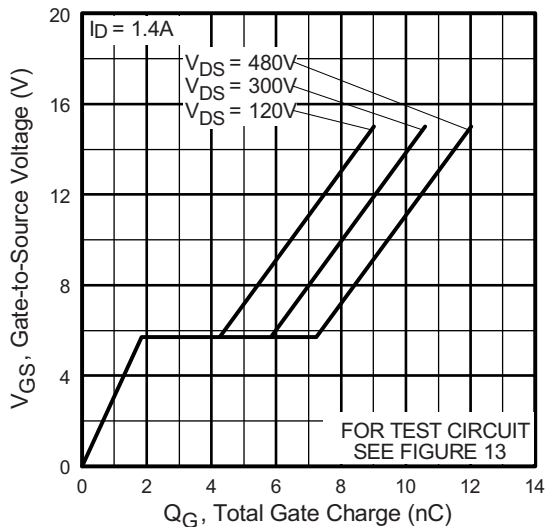


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

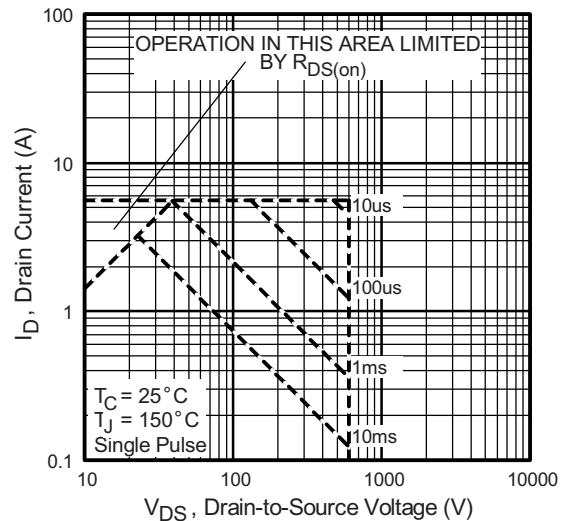


Fig. 7 - Maximum Safe Operating Area

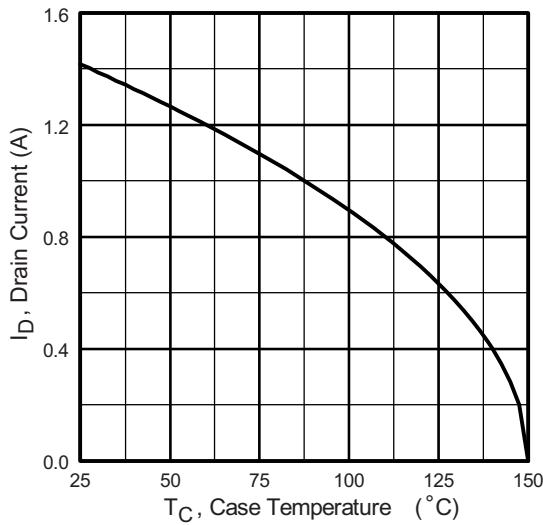


Fig. 8 - Maximum Drain Current vs. Case Temperature

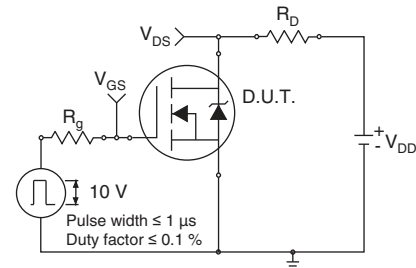


Fig. 10a - Switching Time Test Circuit

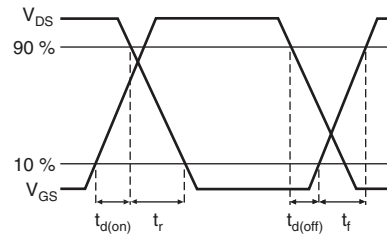


Fig. 10b - Switching Time Waveforms

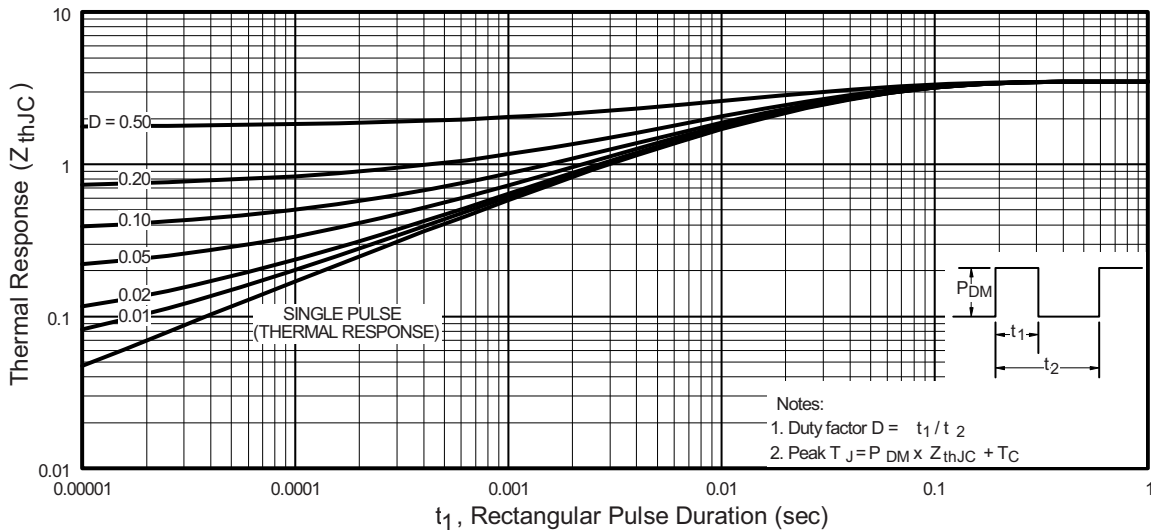


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

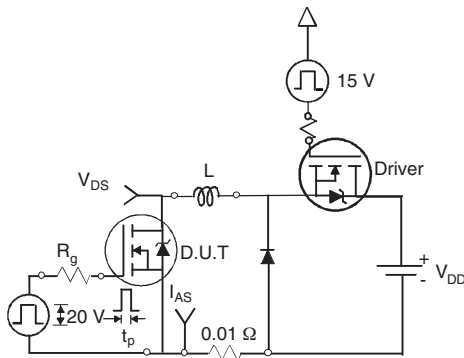


Fig. 12a - Unclamped Inductive Test Circuit

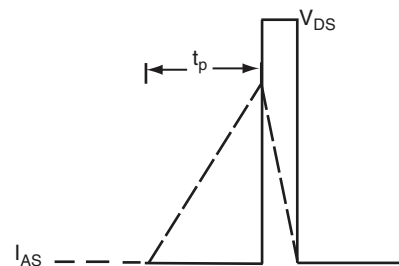


Fig. 12b - Unclamped Inductive Waveforms

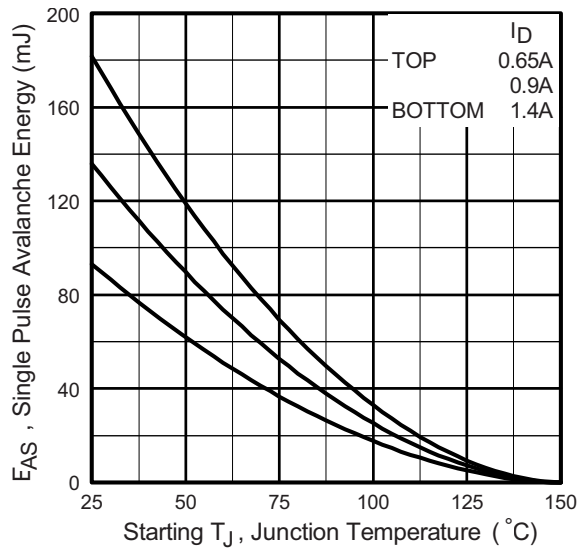


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

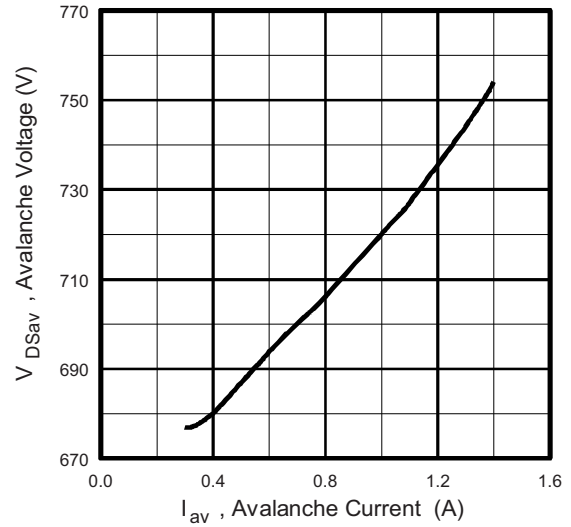


Fig. 12d - Basic Gate Charge Waveform

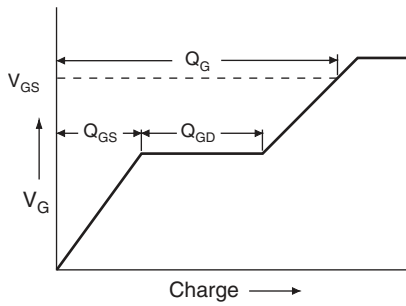


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

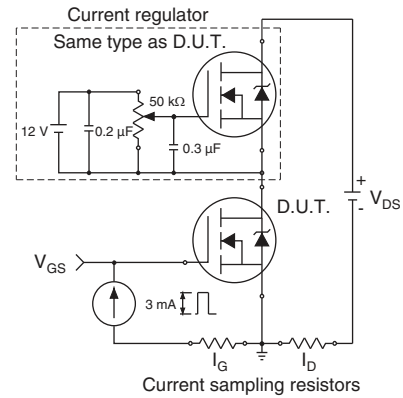
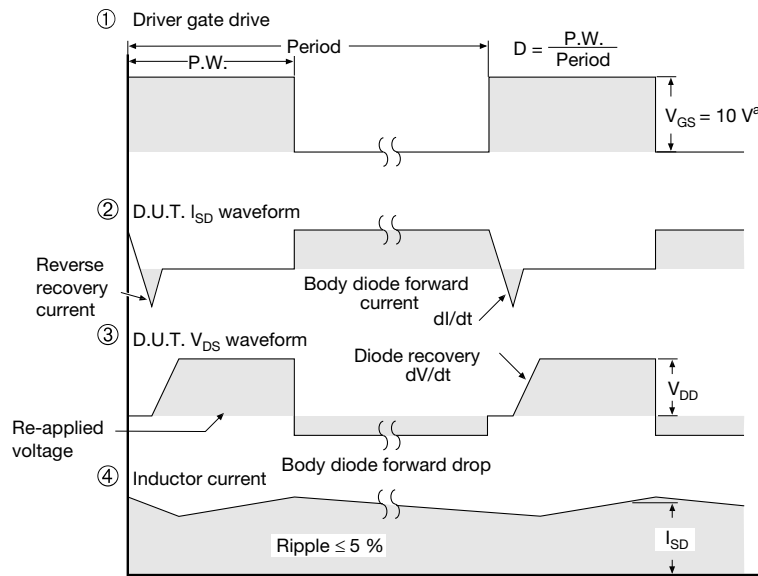
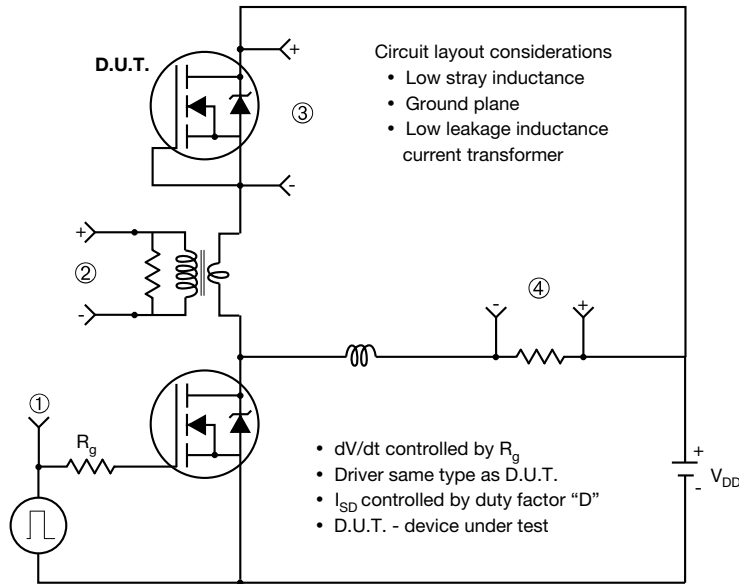


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

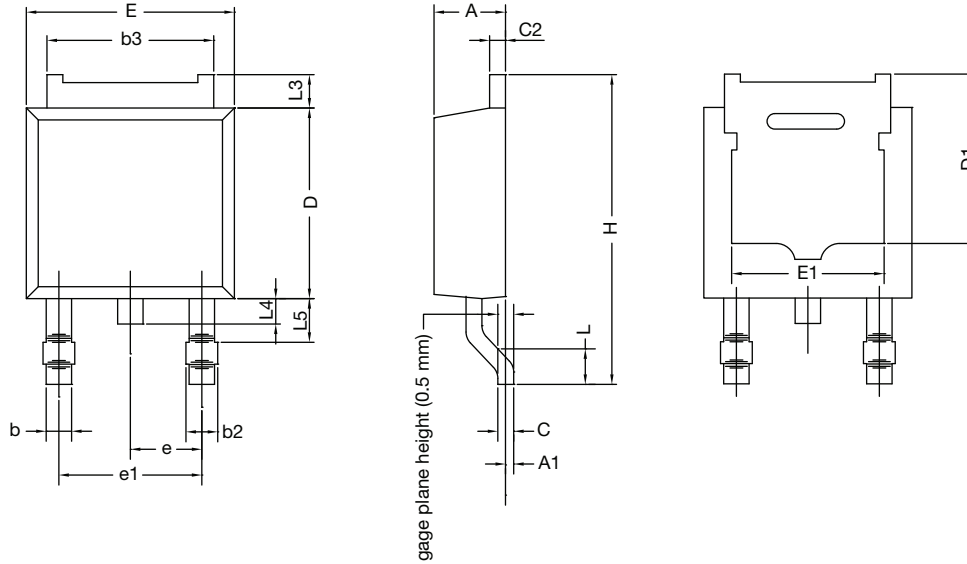
Fig. 10 - For N-Channel

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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
$\theta 1$	0°	15°
$\theta 2$	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019
 DWG: 5347

TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

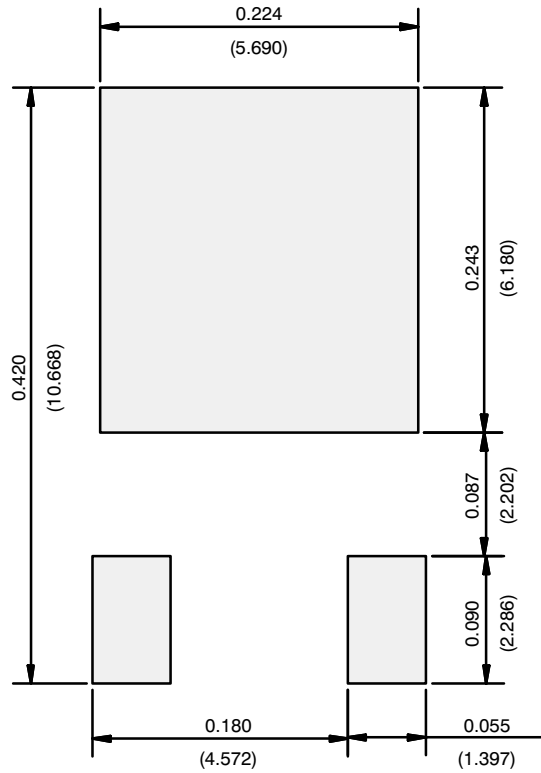
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
theta1	0'	15'	0'	15'
theta2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08
DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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