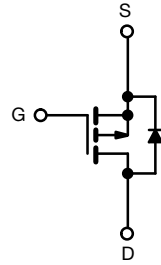


## Power MOSFET



P-Channel MOSFET

### FEATURES

- Advanced process technology
- Fully avalanche rated
- Surface-mount (IRFR9310, SiHFR9310)
- Straight lead (IRFU9310, SiHFU9310)
- P-channel
- Fast switching
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### DESCRIPTION

Third generation power MOSFETs from Vishay utilize advanced processing techniques to achieve low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The DPAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU/SiHFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 W are possible in typical surface-mount applications.

### PRODUCT SUMMARY

$V_{DS}$ (V)	-400	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = -10$ V	7.0
$Q_g$ (Max.) (nC)	13	
$Q_{gs}$ (nC)	3.2	
$Q_{gd}$ (nC)	5.0	
Configuration	Single	

### ORDERING INFORMATION

Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFR9310-GE3	SiHFR9310TRL-GE3	SiHFR9310TR-GE3	SiHFR9310TRR-GE3	SiHFU9310-GE3
Lead (Pb)-free	-	IRFR9310TRLPbF-BE3	-	-	-
Lead (Pb)-free	IRFR9310PbF	IRFR9310TRLPbF <sup>a</sup>	IRFR9310TRPbF <sup>a</sup>	IRFR9310TRRPbF <sup>a</sup>	IRFU9310PbF

#### Note

- a. See device orientation

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	400	V
Gate-source voltage	$V_{GS}$	$\pm 20$	
Continuous drain current	$I_D$	$T_C = 25$ °C	-1.8
		$T_C = 100$ °C	-1.1
Pulsed drain current <sup>a</sup>	$I_{DM}$	-7.2	A
Linear derating factor		0.40	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	92	mJ
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	-1.8	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	5.0	mJ
Maximum power dissipation	$P_D$	50	W
Peak diode recovery $dV/dt$ <sup>c</sup>	$dV/dt$	-24	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	

#### Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
 b. Starting  $T_J = 25$  °C,  $L = 57$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = -1.8$  A (see fig. 12)  
 c.  $I_{SD} \leq -1.1$  A,  $dI/dt \leq 450$  A/ $\mu$ s,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150$  °C  
 d. 1.6 mm from case



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	-	110	°C/W
Maximum junction-to-ambient (PCB mount) <sup>a</sup>	$R_{thJA}$	-	-	50	
Maximum junction-to-case (drain)	$R_{thJC}$	-	-	2.5	

**Note**

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$		-400	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = -1\text{ mA}$		-	-0.41	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$		-2.0	-	-4.0	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -400\text{ V}, V_{GS} = 0\text{ V}$		-	-	-100	$\mu\text{A}$
		$V_{DS} = -320\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	-500	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -1.1\text{ A}^b$	-	-	7.0	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = -50\text{ V}, I_D = -1.1\text{ A}$		0.91	-	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$		-	270	-	pF
Output capacitance	$C_{oss}$			-	50	-	
Reverse transfer capacitance	$C_{rss}$			-	8.0	-	
Total gate charge	$Q_g$	$V_{GS} = -10\text{ V}$	$I_D = -1.1\text{ A}, V_{DS} = -320\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	13	nC
Gate-source charge	$Q_{gs}$			-	-	3.2	
Gate-drain charge	$Q_{gd}$			-	-	5.0	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -200\text{ V}, I_D = -1.1\text{ A}, R_g = 21\text{ }\Omega, R_D = 180\text{ }\Omega, \text{ see fig. 10}^b$		-	11	-	ns
Rise time	$t_r$			-	10	-	
Turn-off delay time	$t_{d(off)}$			-	25	-	
Fall time	$t_f$			-	24	-	
Internal drain inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact <sup>c</sup>		-	4.5	-	nH
Internal source inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p-n junction diode		-	-	-1.9	A
Pulsed diode forward current <sup>a</sup>	$I_{SM}$			-	-	-7.6	
Body diode voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = -1.1\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	-4.0	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = -1.1\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	170	260	ns
Body diode reverse recovery charge	$Q_{rr}$			-	640	960	nC
Forward turn-on time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$
- c. This is applied for IPAK,  $L_S$  of DPAK is measured between lead and center of die contact



## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

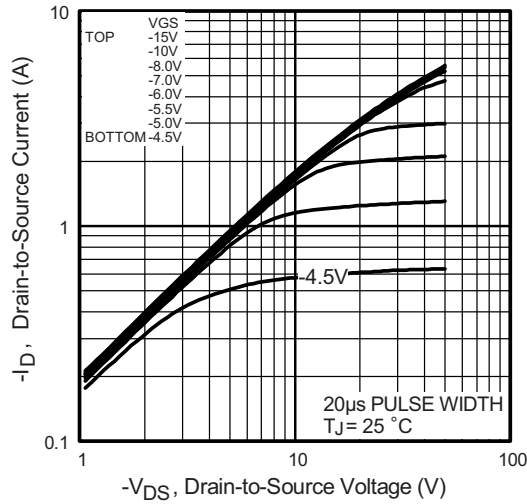


Fig. 1 - Typical Output Characteristics

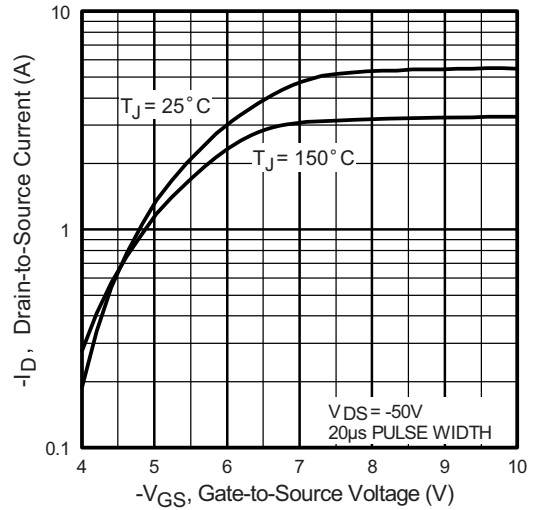


Fig. 2 - Typical Transfer Characteristics

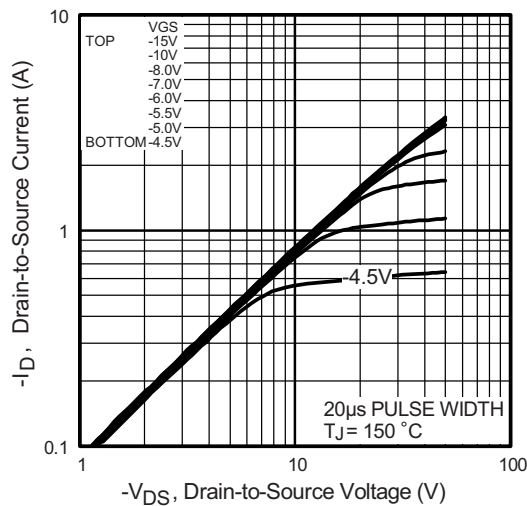


Fig. 1 - Typical Output Characteristics

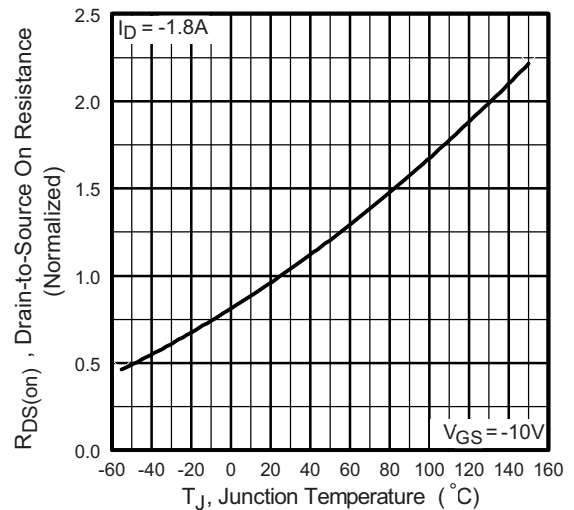


Fig. 3 - Normalized On-Resistance vs. Temperature

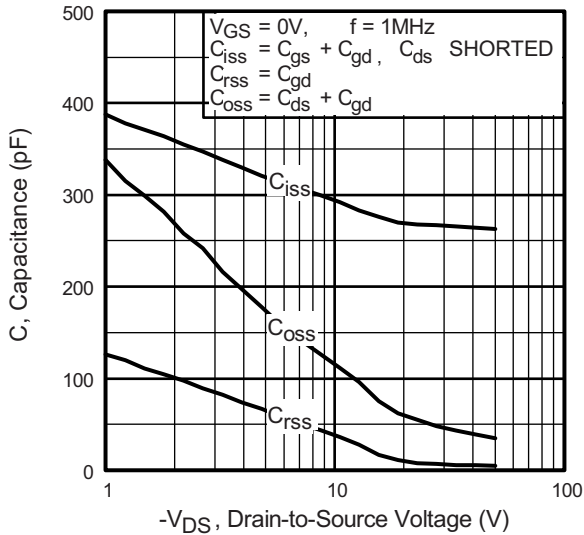


Fig. 4 - Typical Capacitance vs. Drain-to-Source Voltage

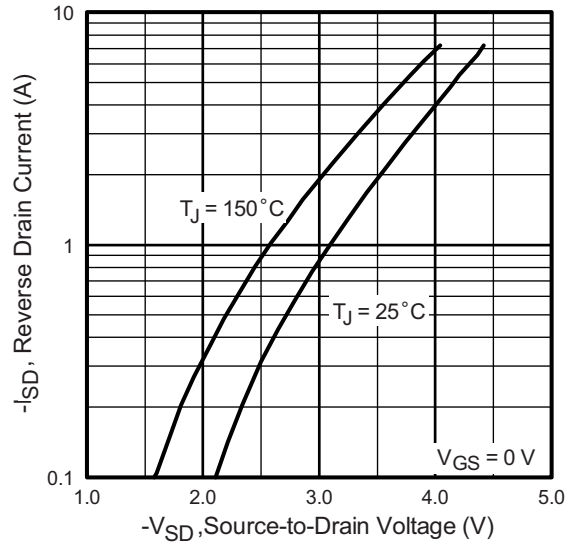


Fig. 6 - Typical Source-Drain Diode Forward Voltage

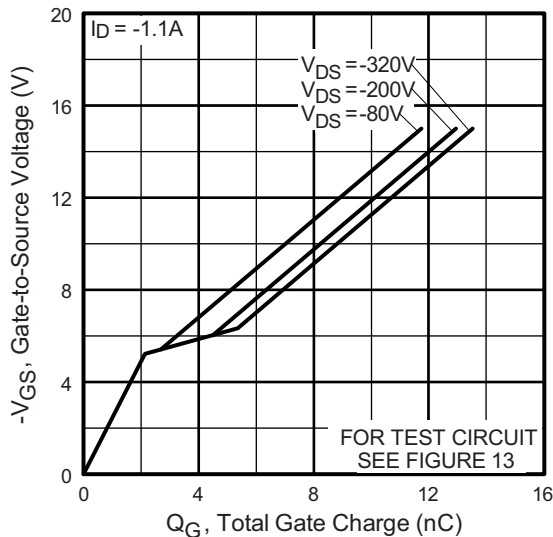


Fig. 5 - Typical Gate Charge vs. Gate-to-Source Voltage

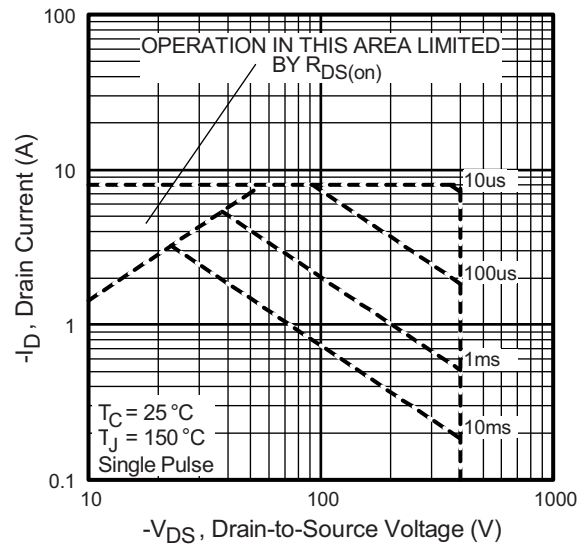


Fig. 7 - Maximum Safe Operating Area

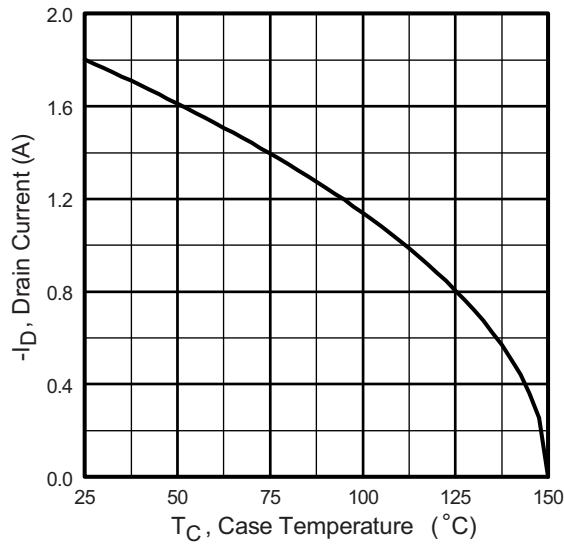


Fig. 8 - Maximum Drain Current vs. Case Temperature

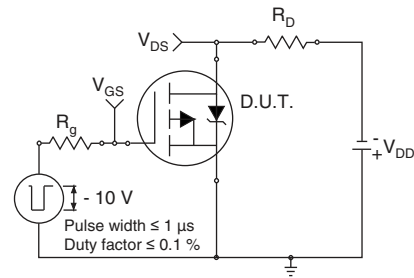


Fig. 10a - Switching Time Test Circuit

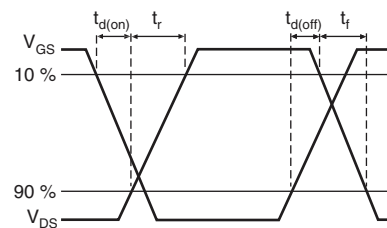


Fig. 10b - Switching Time Waveforms

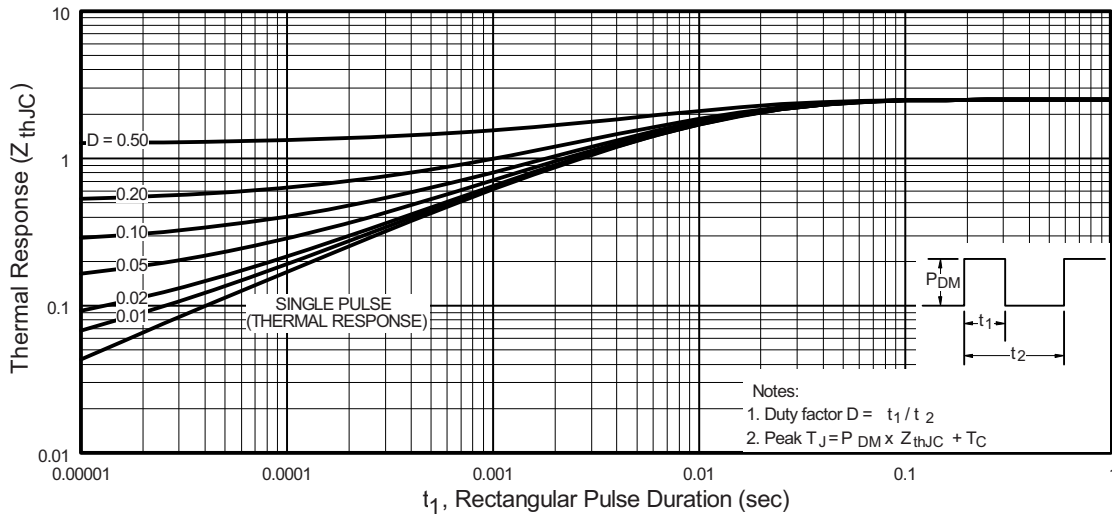


Fig. 9 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

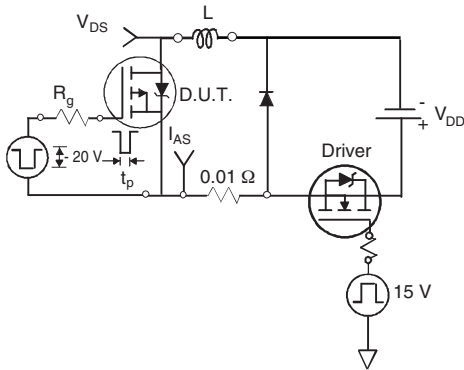


Fig. 12a - Unclamped Inductive Test Circuit

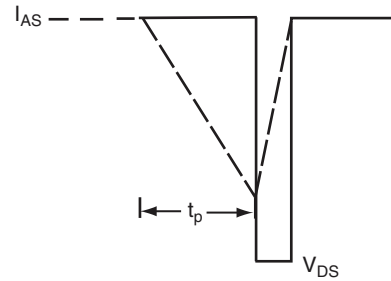


Fig. 12b - Unclamped Inductive Waveforms

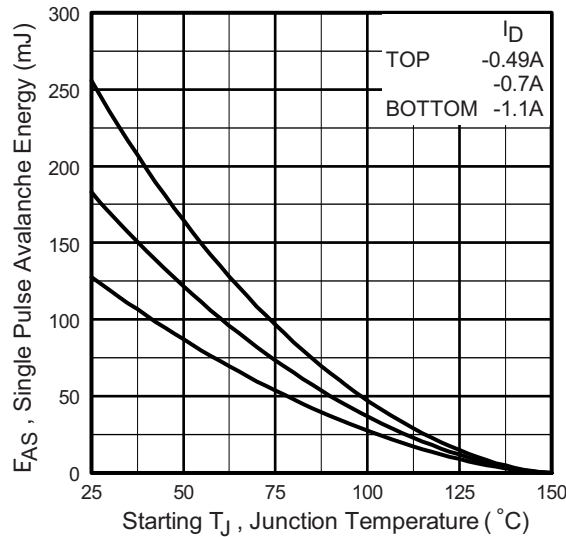


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

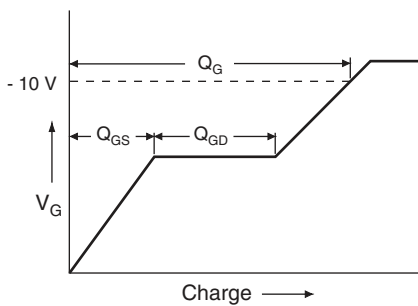


Fig. 13a - Basic Gate Charge Waveform

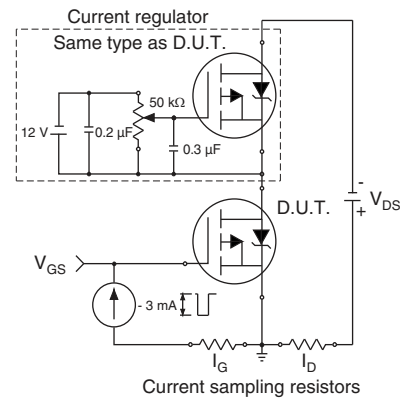
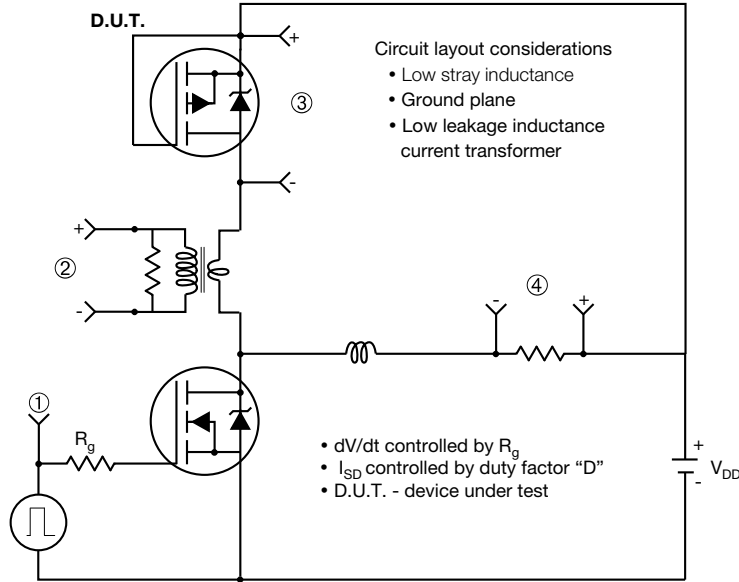


Fig. 13b - Gate Charge Test Circuit

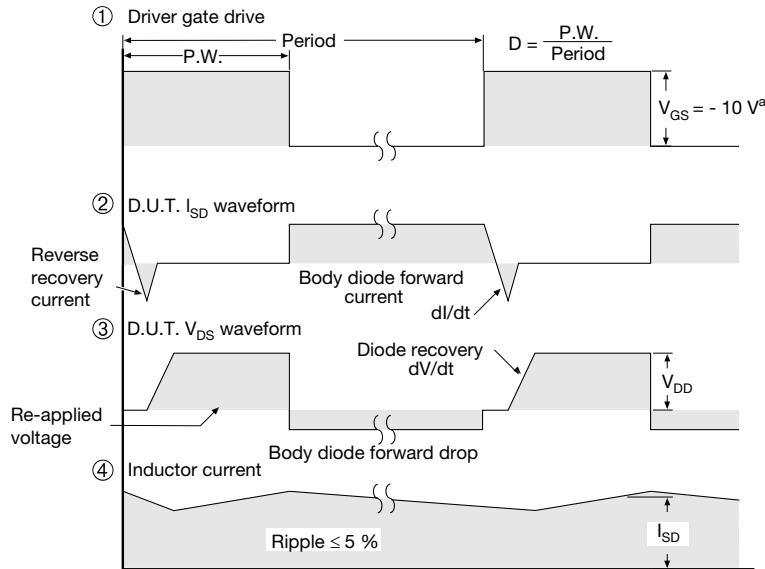
### Peak Diode Recovery dV/dt Test Circuit



- Circuit layout considerations
- Low stray inductance
  - Ground plane
  - Low leakage inductance current transformer

- dV/dt controlled by  $R_g$
- $I_{SD}$  controlled by duty factor "D"
- D.U.T. - device under test

**Note**  
• Compliment N-Channel of D.U.T. for driver



**Note**  
a.  $V_{GS} = -5\text{ V}$  for logic level and  $-3\text{ V}$  drive devices

**Fig. 10 - For P-Channel**

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# TO-252AA Case Outline

## VERSION 1: FACILITY CODE = Y



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

### Note

- Dimension L3 is for reference only





VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E19-0649-Rev. Q, 16-Dec-2019  
DWG: 5347

### TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

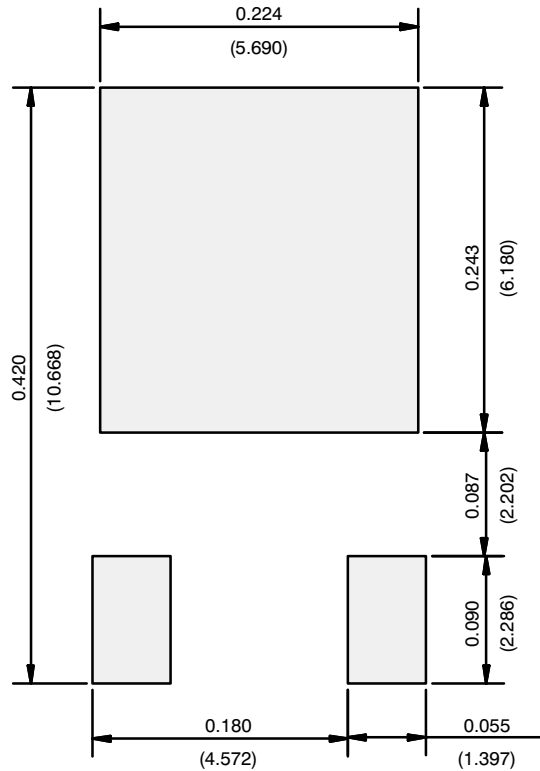
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
theta1	0'	15'	0'	15'
theta2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08  
 DWG: 5968

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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