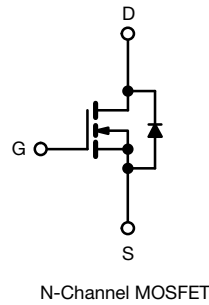
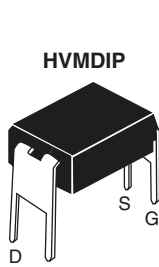


Power MOSFET



N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- For automatic insertion
- End stackable
- Logic-level gate drive
- $R_{DS(on)}$ specified at $V_{GS} = 4\text{ V}$ and 5 V
- $175\text{ }^\circ\text{C}$ operating temperature
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRODUCT SUMMARY

V_{DS} (V)	100	
$R_{DS(on)}$ (Ω)	$V_{GS} = 5.0\text{ V}$	0.27
Q_g (Max.) (nC)	12	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	7.1	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 W.

ORDERING INFORMATION

Package	HVMDIP
Lead (Pb)-free	IRLD120PbF

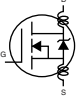

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	100	V
Gate-source voltage	V_{GS}	± 10	
Continuous drain current	I_D	$T_A = 25\text{ }^\circ\text{C}$	1.3
		$T_A = 100\text{ }^\circ\text{C}$	0.94
Pulsed drain current ^a	I_{DM}	10	A
Linear derating factor		0.0083	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	690	mJ
Repetitive avalanche current ^a	I_{AR}	1.3	A
Repetitive avalanche energy ^a	E_{AR}	0.13	mJ
Maximum power dissipation	P_D	1.3	W
Peak diode recovery dv/dt ^c	dV/dt	5.5	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$
Soldering rRecommendations (peak temperature) ^d	For 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 153\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.6\text{ A}$ (see fig. 12)
- $I_{SD} \leq 9.2\text{ A}$, $dI/dt \leq 110\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^\circ\text{C}$
- 1.6 mm from case

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$		-	0.12	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10\text{ V}$		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ °C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5.0\text{ V}$	$I_D = 0.78\text{ A}^b$	-	-	0.27	Ω
		$V_{GS} = 4.0\text{ V}$	$I_D = 0.65\text{ A}^b$	-	-	0.38	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 0.78\text{ A}^b$		1.9	-	-	S
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	490	-	μF
Output Capacitance	C_{oss}			-	150	-	
Reverse Transfer Capacitance	C_{rss}			-	30	-	
Total Gate Charge	Q_g	$V_{GS} = 5.0\text{ V}$	$I_D = 9.2\text{ A}, V_{DS} = 80\text{ V}$, see fig. 6 and 13 ^b	-	-	12	nC
Gate-Source Charge	Q_{gs}			-	-	3.0	
Gate-Drain Charge	Q_{gd}			-	-	7.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 9.2\text{ A}, R_g = 9.0\text{ }\Omega, R_D = 5.2\text{ }\Omega$, see fig. 10 ^b		-	9.8	-	ns
Rise Time	t_r			-	64	-	
Turn-Off Delay Time	$t_{d(off)}$			-	21	-	
Fall Time	t_f			-	27	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L_S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	1.3	A
Pulsed Diode Forward Current ^a	I_{SM}			-	-	10	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ °C}, I_S = 1.3\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}, I_F = 9.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	130	140	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.83	1.0	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

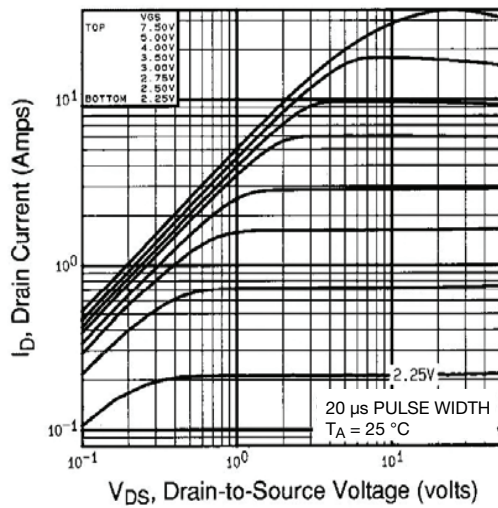


Fig. 1 - Typical Output Characteristics, $T_A = 25\text{ }^\circ\text{C}$

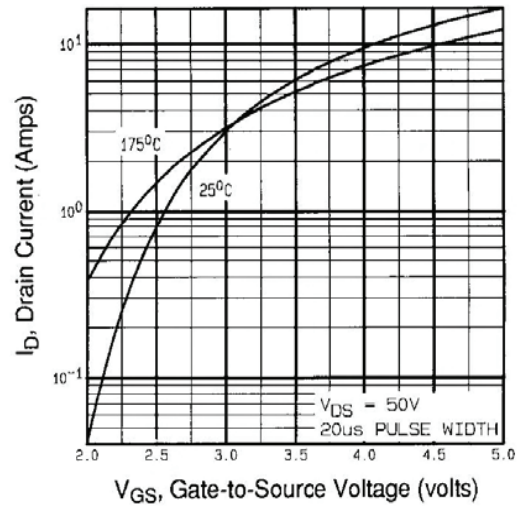


Fig. 3 - Typical Transfer Characteristics

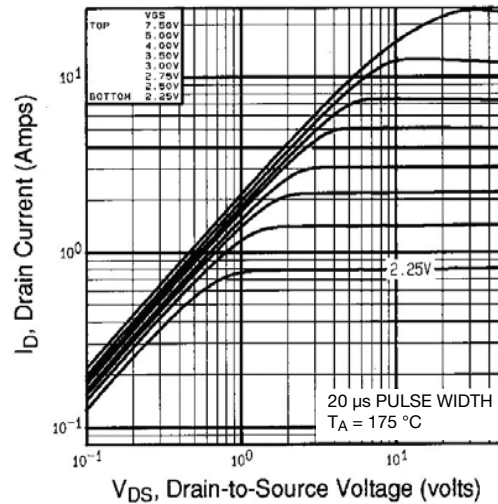


Fig. 2 - Typical Output Characteristics, $T_A = 175\text{ }^\circ\text{C}$

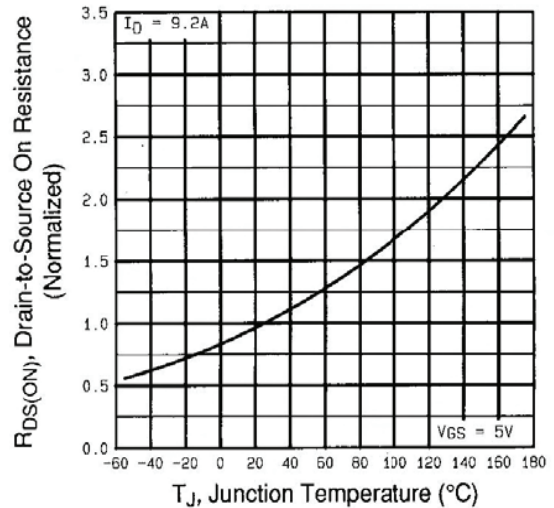


Fig. 4 - Normalized On-Resistance vs. Temperature

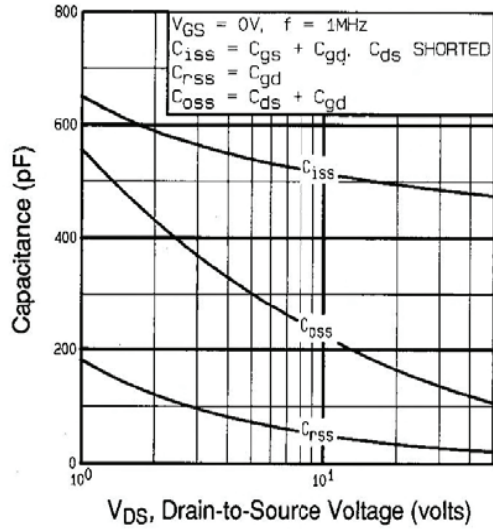


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

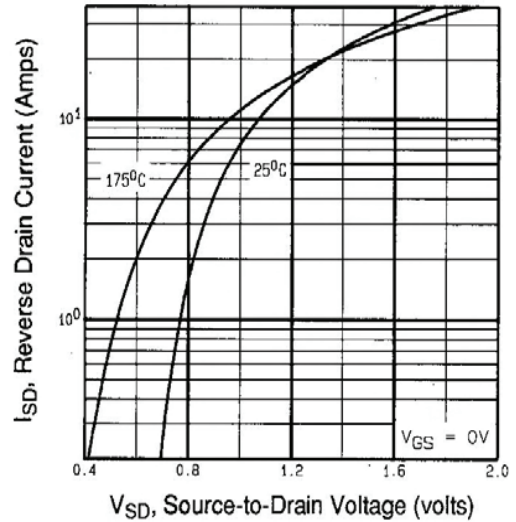


Fig. 7 - Typical Source-Drain Diode Forward Voltage

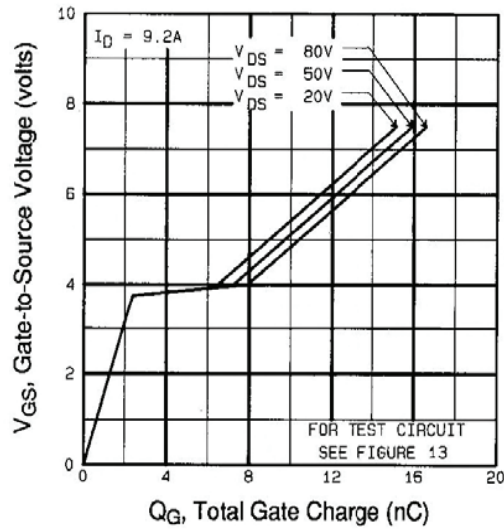


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

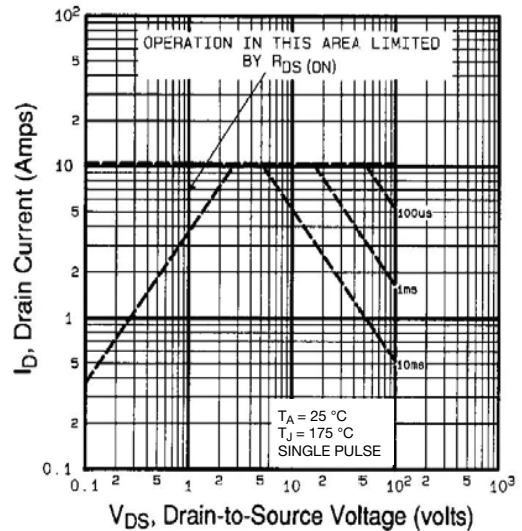


Fig. 8 - Maximum Safe Operating Area

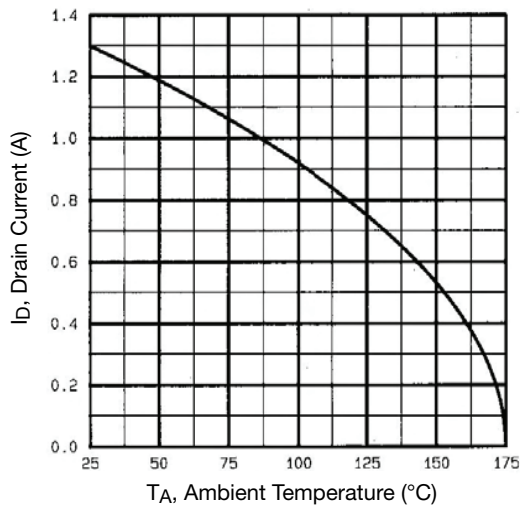


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

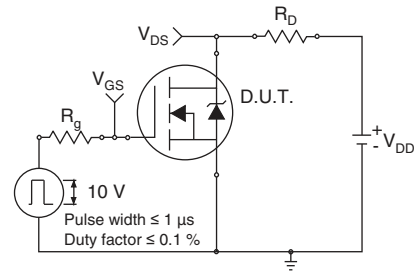


Fig. 10a - Switching Time Test Circuit

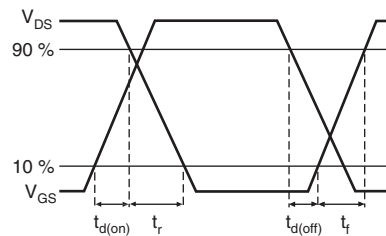


Fig. 10b - Switching Time Waveforms

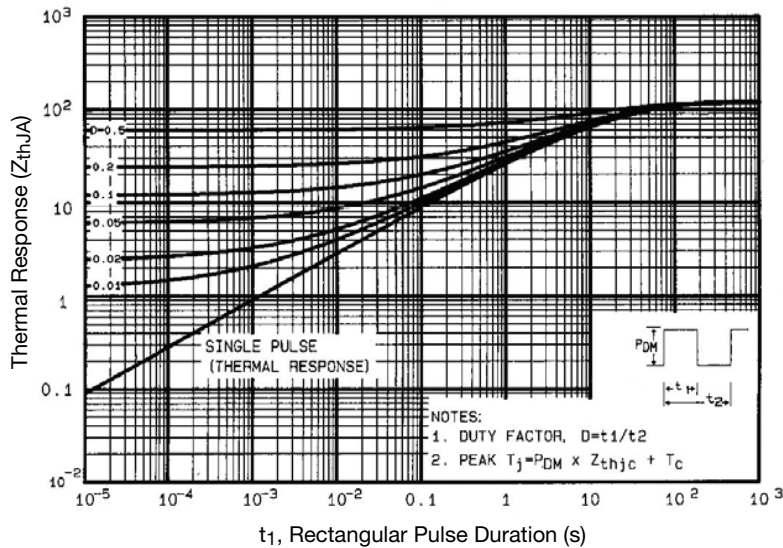


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

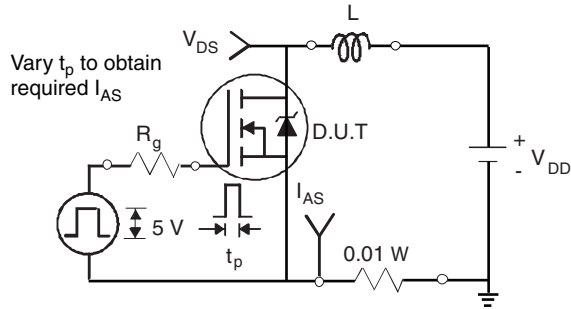


Fig. 12a - Unclamped Inductive Test Circuit

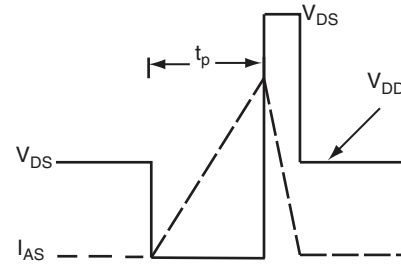


Fig. 12b - Unclamped Inductive Waveforms

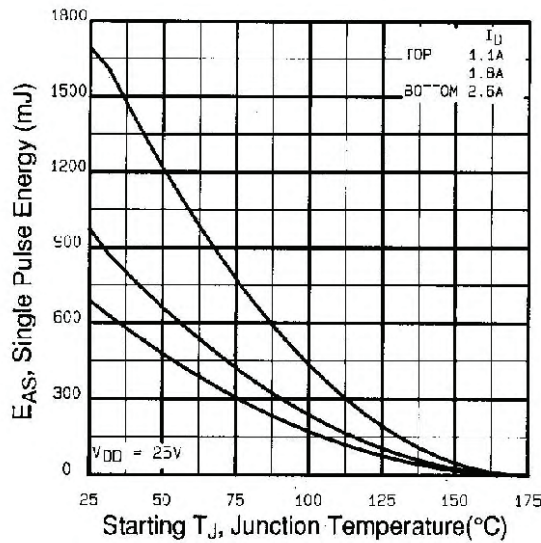


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

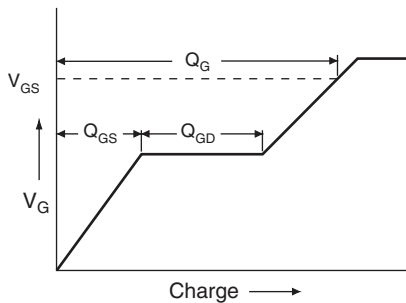


Fig. 13a - Basic Gate Charge Waveform

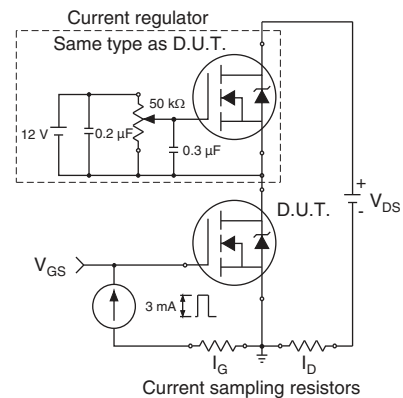
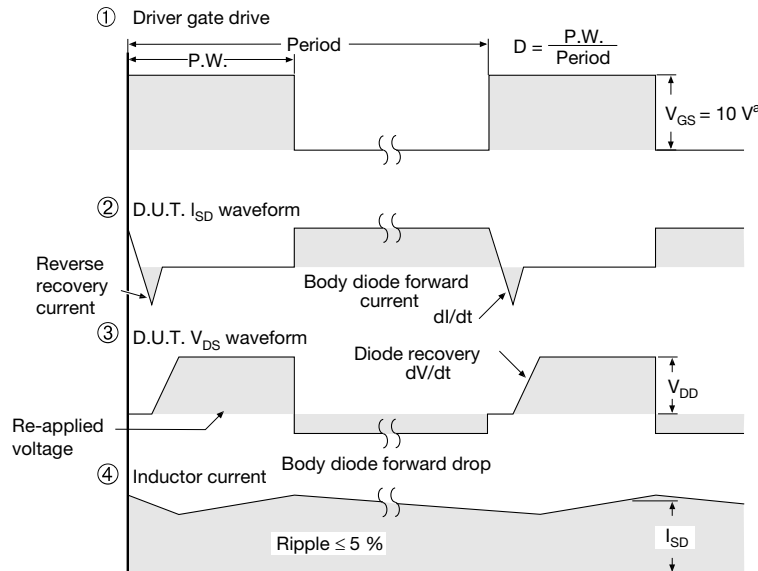
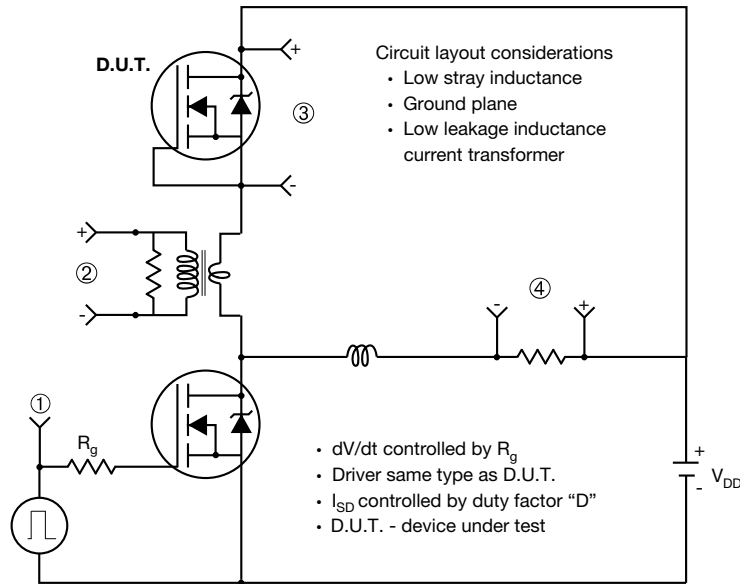


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

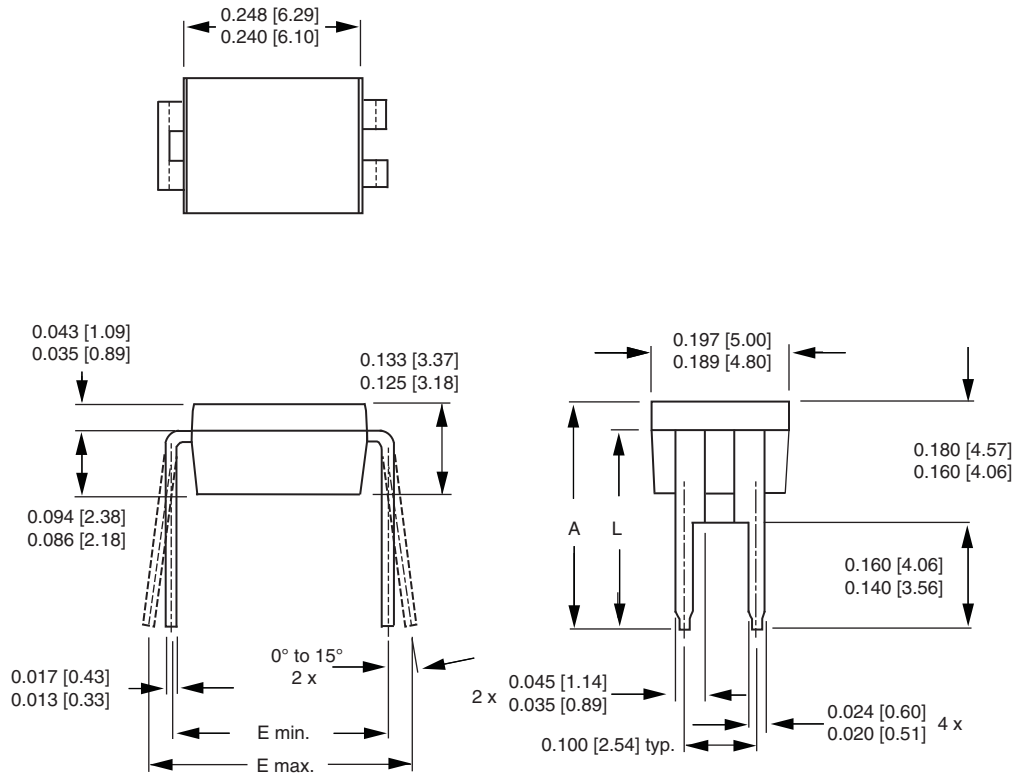


Note
a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

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HVM DIP (High voltage)



DIM.	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.310	0.330	7.87	8.38
E	0.300	0.425	7.62	10.79
L	0.270	0.290	6.86	7.36

ECN: X10-0386-Rev. B, 06-Sep-10
DWG: 5974

Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.



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