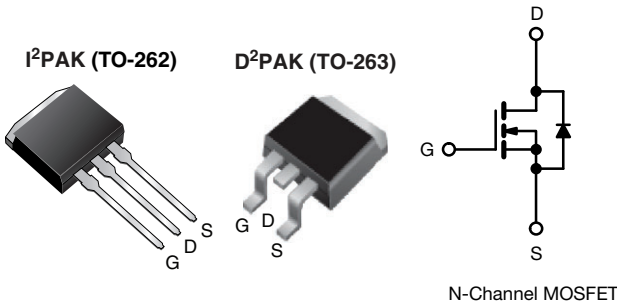


Power MOSFET



FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Logic-level gate drive
- $R_{DS(on)}$ specified at $V_{GS} = 4\text{ V}$ and 5 V
- 175°C operating temperature
- Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ (Ω)	$V_{GS} = 5\text{ V}$ 0.10
Q_g max. (nC)	18
Q_{gs} (nC)	4.5
Q_{gd} (nC)	12
Configuration	Single

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

The through-hole version (IRLZ24L, SiHLZ24L) is available for low profile application.

ORDERING INFORMATION		
Package	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and halogen-free	SiHLZ24S-GE3	SiHLZ24L-GE3
Lead (Pb)-free	IRLZ24SPbF	IRLZ24LPbF

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 10	
Continuous drain current	V_{GS} at 5 V	$T_C = 25^\circ\text{C}$	A
		$T_C = 100^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	68	W/ $^\circ\text{C}$
Linear derating factor		0.40	
Linear derating factor (PCB mount) ^e		0.025	
Single pulse avalanche energy ^b	E_{AS}	110	mJ
Maximum power dissipation	P_D	$T_C = 25^\circ\text{C}$	W
		$T_A = 25^\circ\text{C}$	
Peak diode recovery dv/dt ^c	dv/dt	4.5	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Soldering recommendations (peak temperature) ^d	For 10 s	300	

Notes

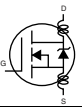

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$, starting $T_J = 25^\circ\text{C}$, $L = 444\ \mu\text{H}$, $R_g = 25\ \Omega$, $I_{AS} = 17\text{ A}$ (see fig. 12)
- $I_{SD} \leq 17\text{ A}$, $di/dt \leq 140\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Maximum junction-to-ambient (PCB mount) ^a	R_{thJA}	-	40	
Maximum junction-to-case (drain)	R_{thJC}	-	2.5	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.060	-	V/°C
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.0	-	2.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 10\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 5\text{ V}$	$I_D = 10\text{ A}^b$	-	-	0.10	Ω
		$V_{GS} = 4\text{ V}$	$I_D = 8.5\text{ A}^b$	-	-	0.14	
Forward transconductance	g_{fs}	$V_{DS} = 25\text{ V}, I_D = 10\text{ A}^b$		7.3	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5		-	870	-	μF
Output capacitance	C_{oss}			-	360	-	
Reverse transfer capacitance	C_{rss}			-	53	-	
Total gate charge	Q_g	$V_{GS} = 5\text{ V}$	$I_D = 17\text{ A}, V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^b	-	-	18	nC
Gate-source charge	Q_{gs}			-	-	4.5	
Gate-drain charge	Q_{gd}			-	-	12	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, I_D = 17\text{ A}, R_g = 9\text{ }\Omega, R_D = 1.7\text{ }\Omega$, see fig. 10 ^b		-	11	-	ns
Rise time	t_r			-	110	-	
Turn-off delay time	$t_{d(off)}$			-	23	-	
Fall time	t_f			-	41	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	17	A
Pulsed diode forward current ^a	I_{SM}			-	-	68	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 17\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	110	260	ns
Body diode reverse recovery charge	Q_{rr}			-	0.49	1.5	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

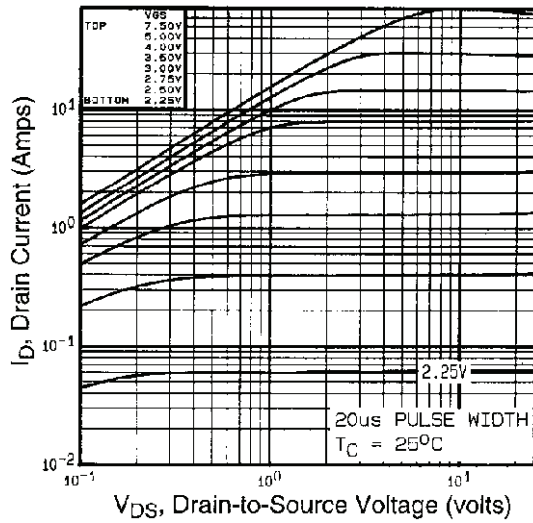


Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

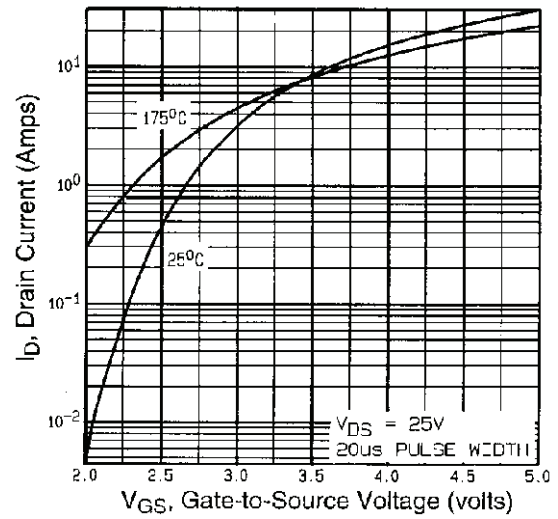


Fig. 3 - Typical Transfer Characteristics

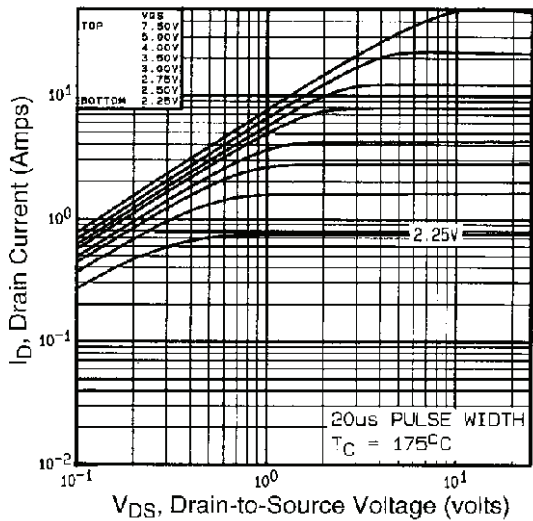


Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ\text{C}$

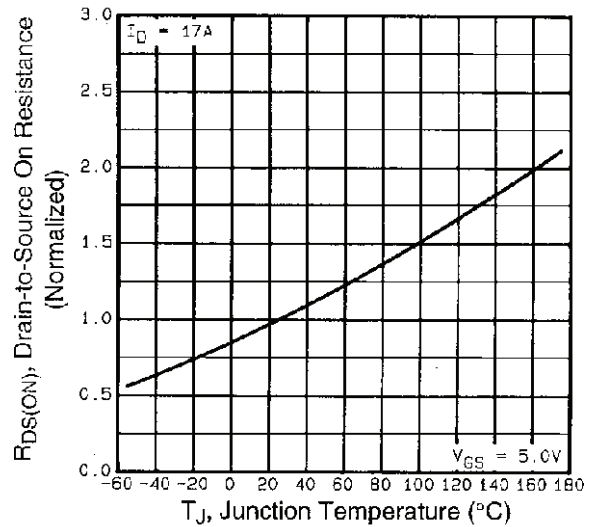


Fig. 4 - Normalized On-Resistance vs. Temperature

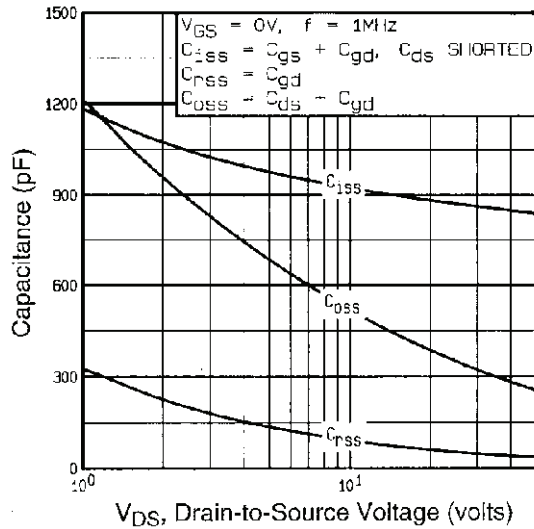


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

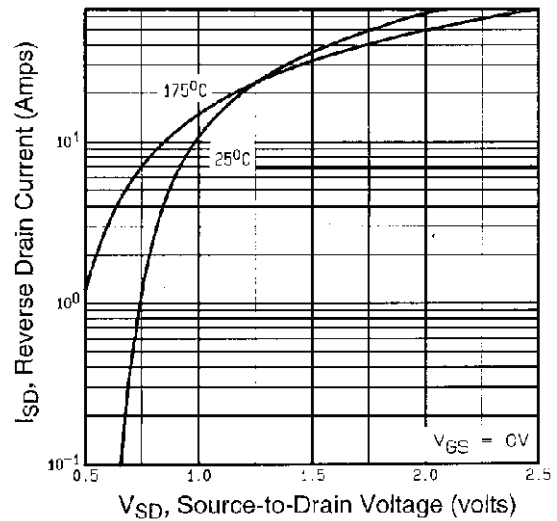


Fig. 7 - Typical Source-Drain Diode Forward Voltage

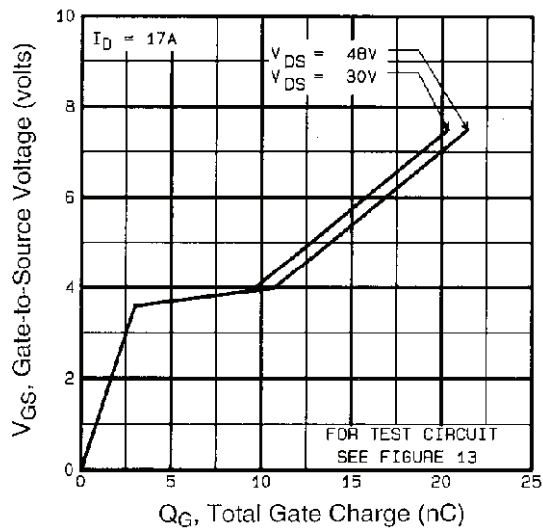


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

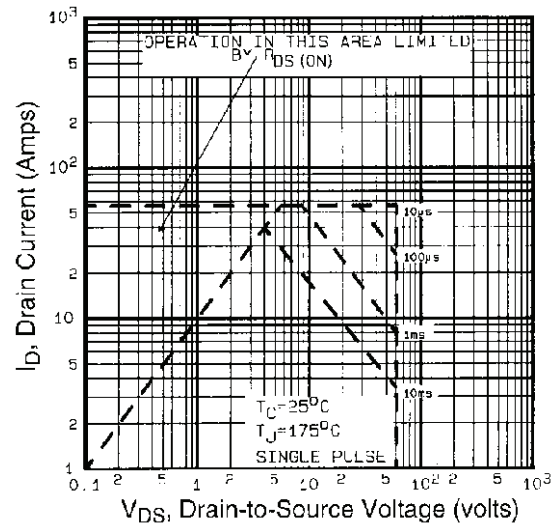


Fig. 8 - Maximum Safe Operating Area

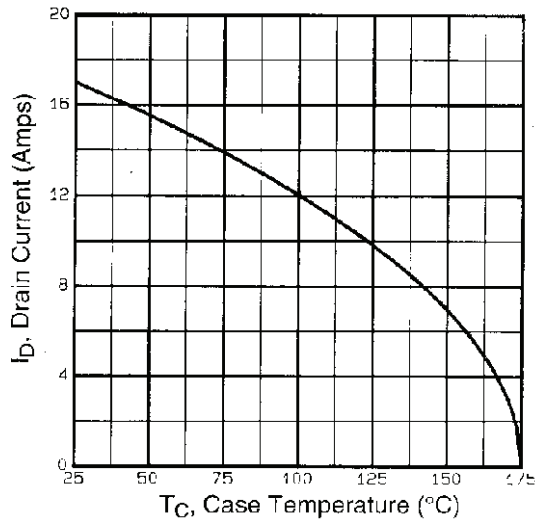


Fig. 9 - Maximum Drain Current vs. Case Temperature

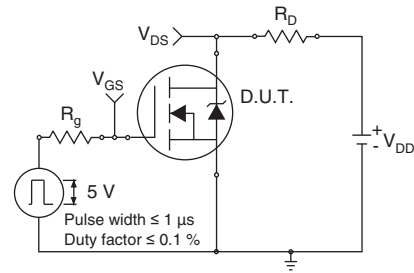


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

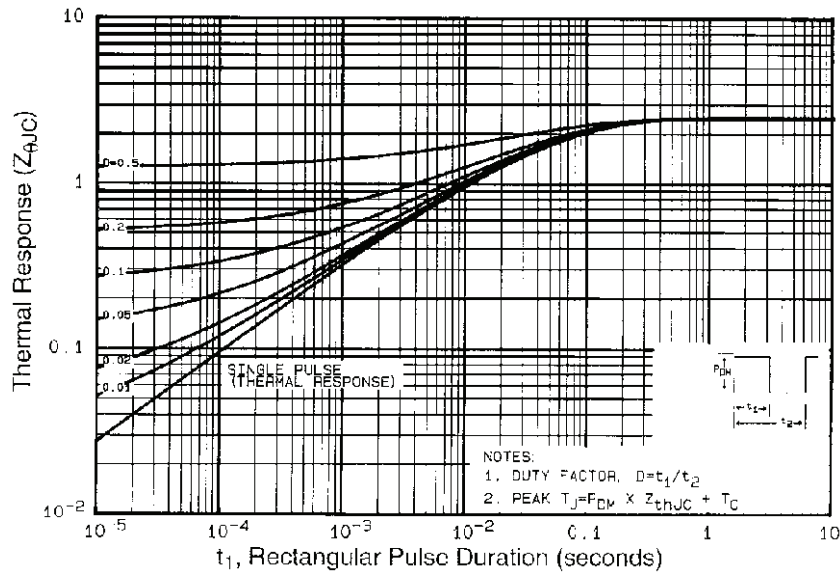


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

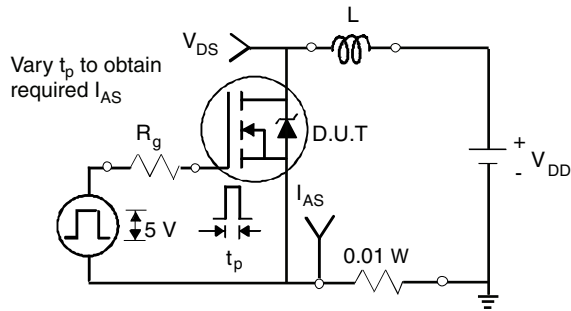


Fig. 12a - Unclamped Inductive Test Circuit

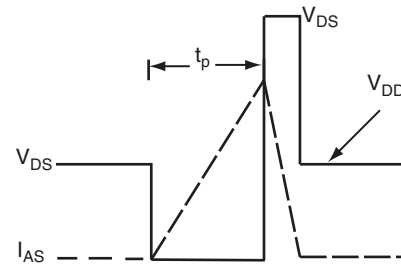


Fig. 12b - Unclamped Inductive Waveforms

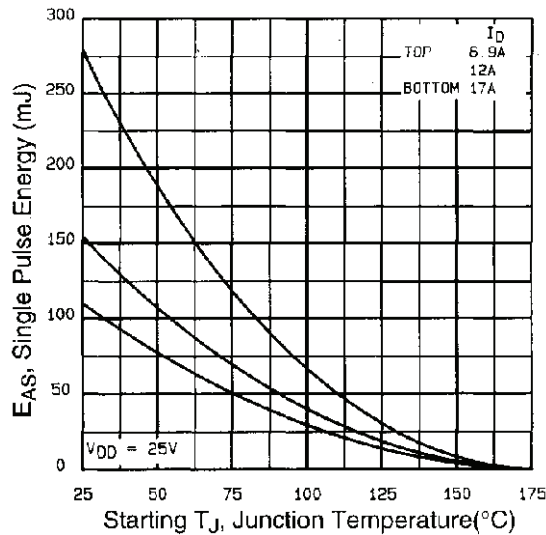


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

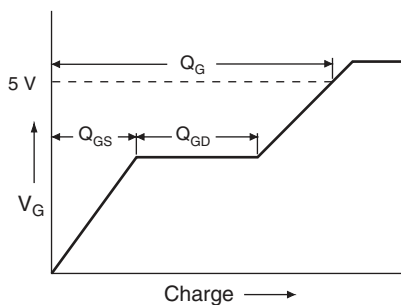


Fig. 13a - Basic Gate Charge Waveform

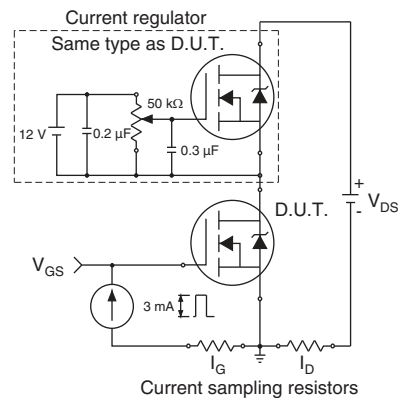
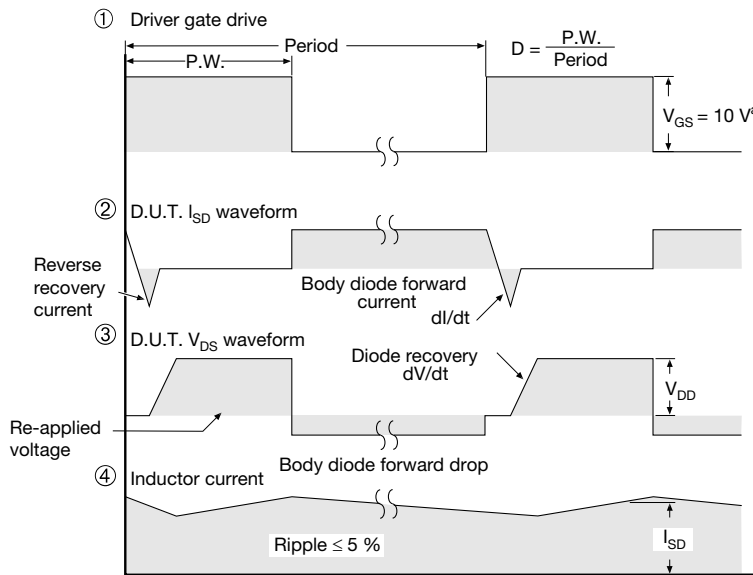
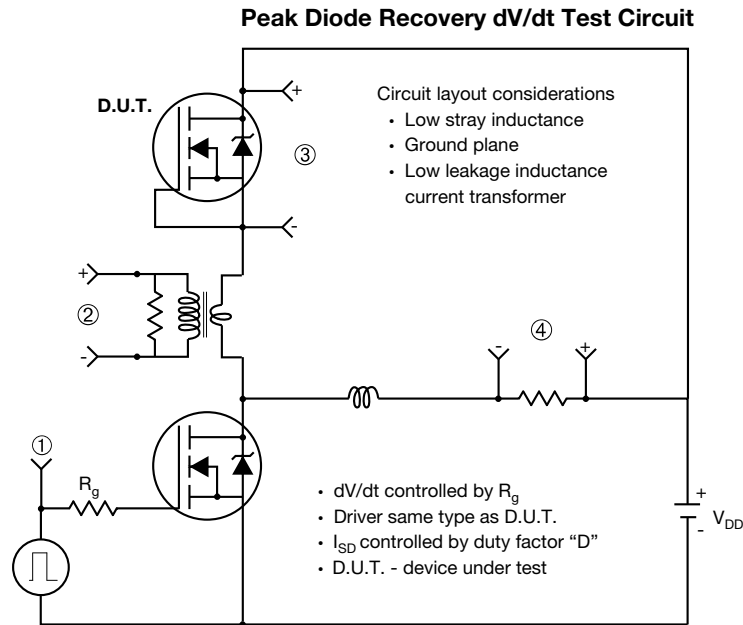


Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?90416.

TO-252AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
E	6.40	6.73	0.252	0.265
L	1.40	1.77	0.055	0.070
L1	2.743 REF		0.108 REF	
L2	0.508 BSC		0.020 BSC	
L3	0.89	1.27	0.035	0.050
L4	0.64	1.01	0.025	0.040
D	6.00	6.22	0.236	0.245
H	9.40	10.40	0.370	0.409
b	0.64	0.88	0.025	0.035
b2	0.77	1.14	0.030	0.045
b3	5.21	5.46	0.205	0.215
e	2.286 BSC		0.090 BSC	
A	2.20	2.38	0.087	0.094
A1	0.00	0.13	0.000	0.005
c	0.45	0.60	0.018	0.024
c2	0.45	0.58	0.018	0.023
D1	5.30	-	0.209	-
E1	4.40	-	0.173	-
θ	0'	10'	0'	10'

ECN: S-81965-Rev. A, 15-Sep-08
DWG: 5973

Notes

1. Package body sizes exclude mold flash, protrusion or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.
4. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of "b" dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.

TO-251AA (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

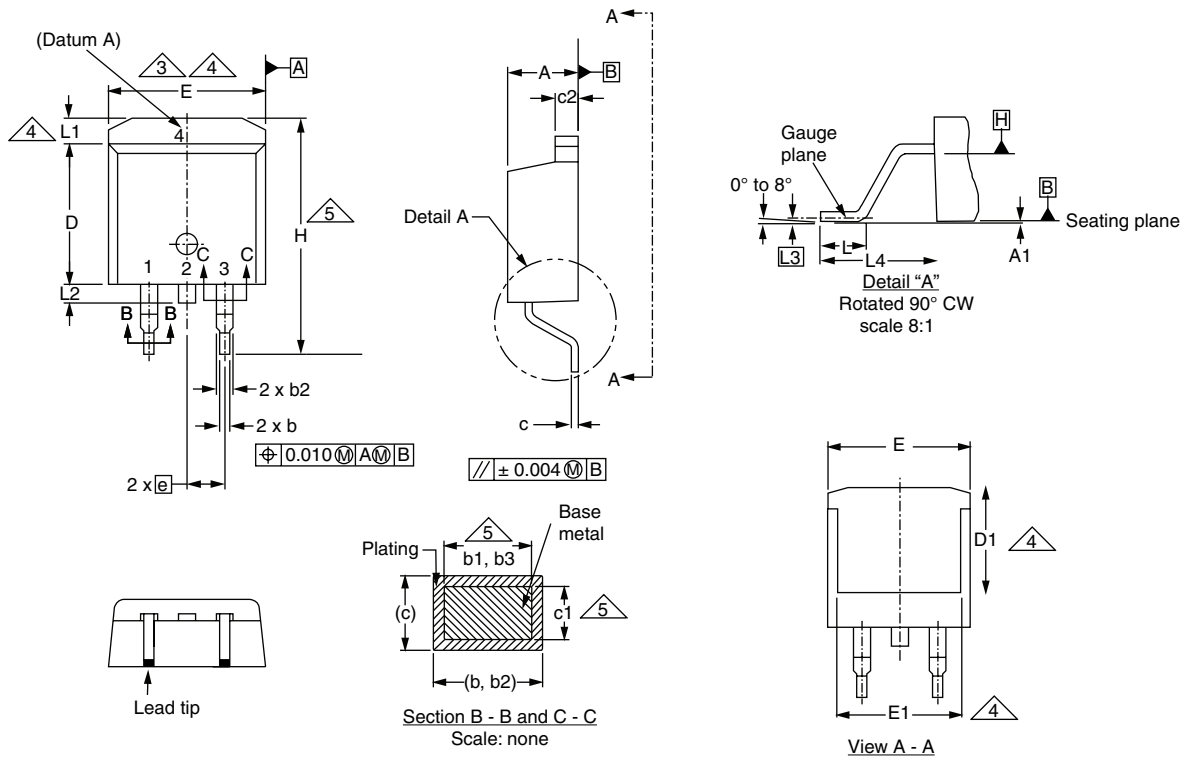
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
theta1	0'	15'	0'	15'
theta2	25'	35'	25'	35'

ECN: S-82111-Rev. A, 15-Sep-08
 DWG: 5968

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension are shown in inches and millimeters.
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body.
4. Thermal pad contour optional with dimensions b4, L2, E1 and D1.
5. Lead dimension uncontrolled in L3.
6. Dimension b1, b3 and c1 apply to base metal only.
7. Outline conforms to JEDEC outline TO-251AA.

TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

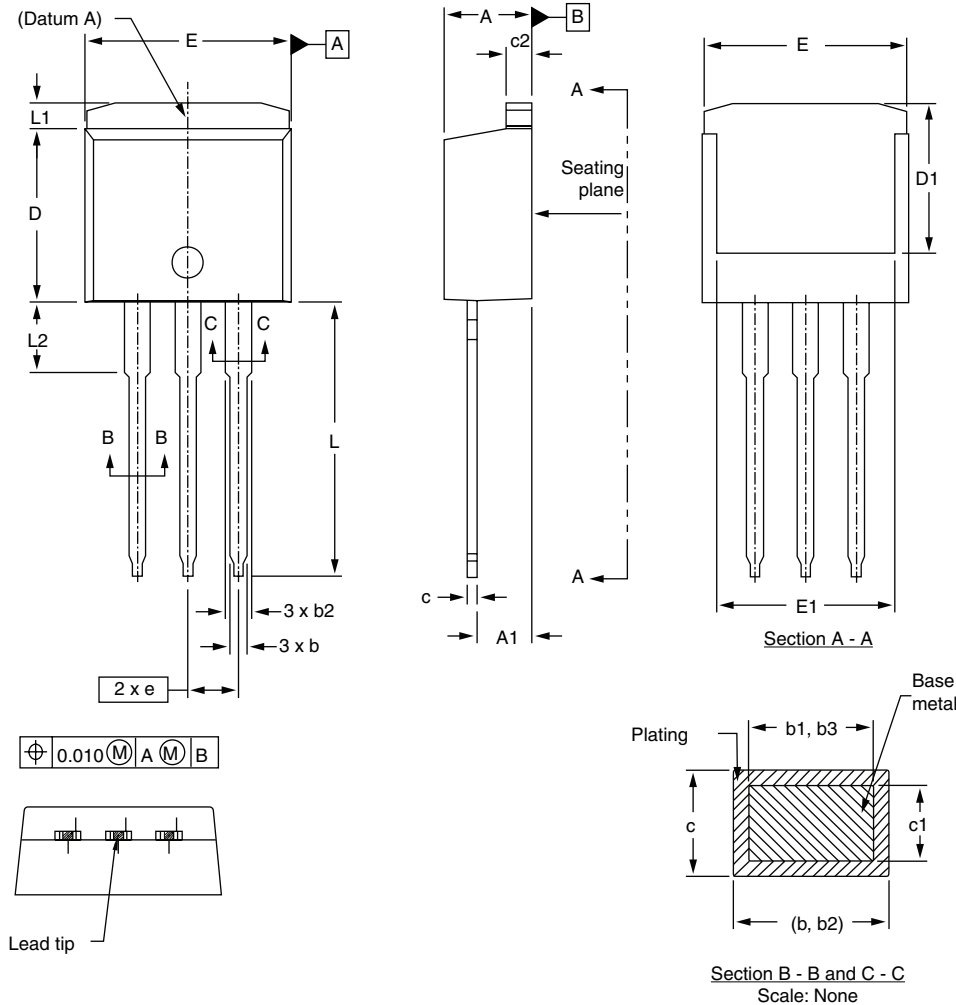
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

I²PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

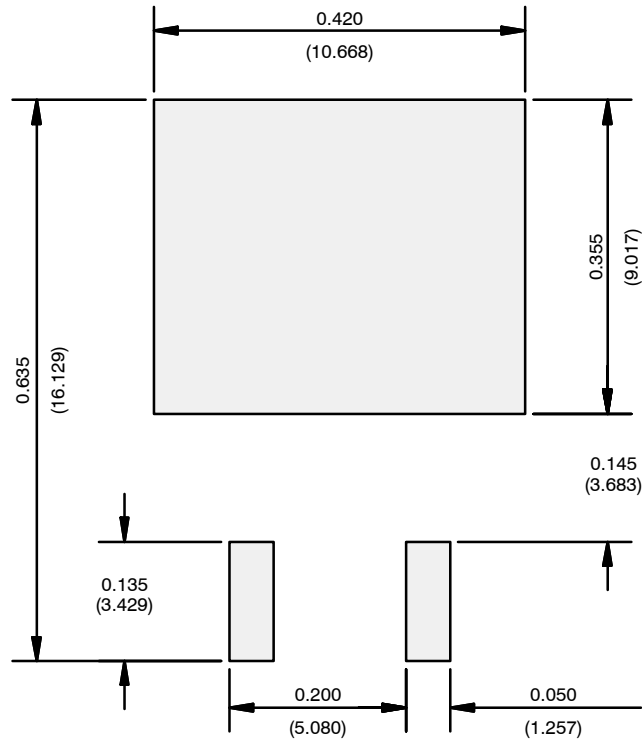
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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[NTE2903](#) [NTE2941](#) [NTE2945](#) [NTE2946](#) [NTE2960](#) [NTE2967](#) [NTE2969](#) [NTE2976](#) [NTE455](#) [NTE6400A](#) [NTE2910](#) [NTE2916](#) [NTE2956](#)
[NTE2911](#) [TK10A80W,S4X\(S](#) [SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)