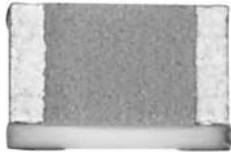


High Precision Wraparound - Wide Ohmic Value Range Thin Film Chip Resistors



For low noise and precision applications, superior stability, low temperature coefficient of resistance, and low voltage coefficient, Vishay Sfernice's proven precision thin film wraparound resistors exceed requirements of MIL-PRF-55342G characteristics $Y \pm 10 \text{ ppm}/^\circ\text{C}$ (- 55 °C; + 155 °C) down to $\pm 5 \text{ ppm}/^\circ\text{C}$ (- 55 °C; + 155 °C).

FEATURES

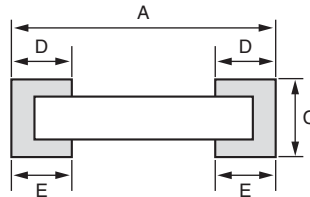
- Load life stability at $\pm 70 \text{ }^\circ\text{C}$ for 2000 h:
0.1 % under Pn/0.05 % under Pd
- Low temperature coefficient down to **5 ppm/°C**
(- 55 °C; + 155 °C)
- Very low noise < - 35 dB and voltage coefficient
< 0.01 ppm/V
- Wide resistance range: 10 Ω to 76 M Ω
depending on size
- Tolerances to **$\pm 0.01 \%$**
- In lot tracking $\leq 5 \text{ ppm}/^\circ\text{C}$
- Termination: Thin film technology
- Gold plated or pre-tinned terminations over nickel barrier
- Short circuits (jumpers) $r < 50 \text{ m}\Omega$, $I < 2 \text{ A}$, see PZR
datasheet (www.vishay.com/doc?53053)
- SMD wraparound terminations
- Withstand moisture resistance test of AEC-Q200
- Compliant to RoHS Directive 2002/95/EC



Notes

- * Pb containing terminations are not RoHS compliant, exemptions may apply
- ** Please see document "Vishay Material Category Policy":
www.vishay.com/doc?99902

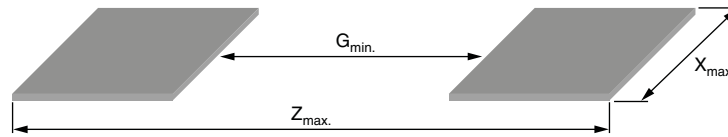
DIMENSIONS in millimeters (inches)



CASE SIZE	A		B		C	D/E	
	MAX. TOL. + 0.152 (+ 0.006)	MIN. TOL. - 0.152 (- 0.006)	MAX. TOL. + 0.127 (+ 0.005)	MIN. TOL. - 0.127 (- 0.005)		NOMINAL	TOLERANCE
	NOMINAL		NOMINAL				
0302	0.75 (0.029)		0.60 (0.024)		0.5 (0.02) $\pm 0.127 (0.005)$	0.15 (0.006)	0.08 (0.003)
0402	1.00 (0.039)		0.60 (0.024)			0.25 (0.010)	0.1 (0.004)
0505	1.27 (0.050)		1.27 (0.050)			0.38 (0.015)	0.13 (0.005)
0603	1.52 (0.060)		0.85 (0.033)				
0705/0805	1.91 (0.075)		1.27 (0.050)				
1005	2.54 (0.100)		1.27 (0.050)			0.40 (0.016)	
1206	3.06 (0.120)		1.60 (0.063)			0.48 (0.019)	
1505	3.81 (0.150)		1.32 (0.052)				
2010	5.08 (0.200)		2.54 (0.100)				

Note

- Case size 2512 under development. Please consult Vishay Sfernice.

SUGGESTED LAND PATTERN (to IPC-7351A)


CHIP SIZE	DIMENSIONS (in millimeter)		
	Z _{max.}	G _{min.}	X _{max.}
0302	1.30	0.14	0.73
0402	1.55	0.15	0.73
0505	1.82	0.10	1.40
0603	2.37	0.35	0.98
0705/0805	2.76	0.74	1.40
1005	3.39	1.37	1.40
1206	3.91	1.85	1.73
1505	4.66	2.44	1.45
2010	5.93	3.71	2.67

Note

- Case size 2512 under development. Please consult Vishay Sfernice.

ELECTRICAL SPECIFICATIONS

CASE SIZE	POWER RATING mW		LIMITING ELEMENT VOLTAGE V	RESISTANCE RANGE ⁽²⁾
	P _n ⁽¹⁾	P _d ⁽¹⁾		
0302	40	30	25	10 Ω to 750 kΩ
0402	63	40	50	10 Ω to 1.5 MΩ
0505	125	50	50	10 Ω to 4 MΩ
0603	125	100	75	10 Ω to 3.2 MΩ
0705/0805	200	125	150	10 Ω to 10 MΩ
1005	250	125	75	10 Ω to 8.1 MΩ
1206	330	250	200	10 Ω to 35 MΩ
1505	350	175	75	10 Ω to 15 MΩ
2010	1000	500	300	10 Ω to 76 MΩ

Notes

- Case size 2512 under development. Please consult Vishay Sfernice.
- ⁽¹⁾ P_n = Nominal power - P_d = Derated power intended to improve stability.
- ⁽²⁾ **For ohmic range versus tolerance and TCR see detailed table on next page.**



ELECTRICAL SPECIFICATIONS

Resistance range: 10 Ω to 76 MΩ
 Resistance tolerance: 0.01 % to 1 %
 Power dissipation: Pn: 40 mW to 1 W
 Pd: 40 mW to 500 mW
 Temperature coefficient: Down to 5 ppm - 55 °C; + 155 °C

CLIMATIC SPECIFICATIONS

Operating temp. range: - 55 °C to + 155 °C
 For temperature up to 230 °C, see PHT datasheet (www.vishay.com/doc?53050)

MECHANICAL SPECIFICATIONS

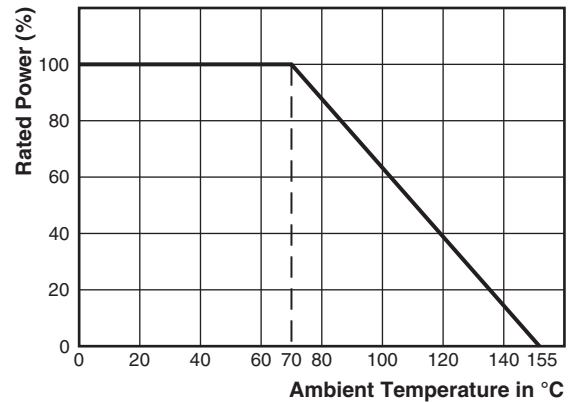
Substrate: Alumina
 Technology: Thin film
 Film: Nickel chromium with mineral passivation or CrSi
 Protection: Silicone
 Terminations: **B type:** SnPb over nickel barrier for solder reflow
N type: SnAg over nickel barrier
G type: gold over nickel barrier for other applications

TEMPERATURE COEFFICIENT

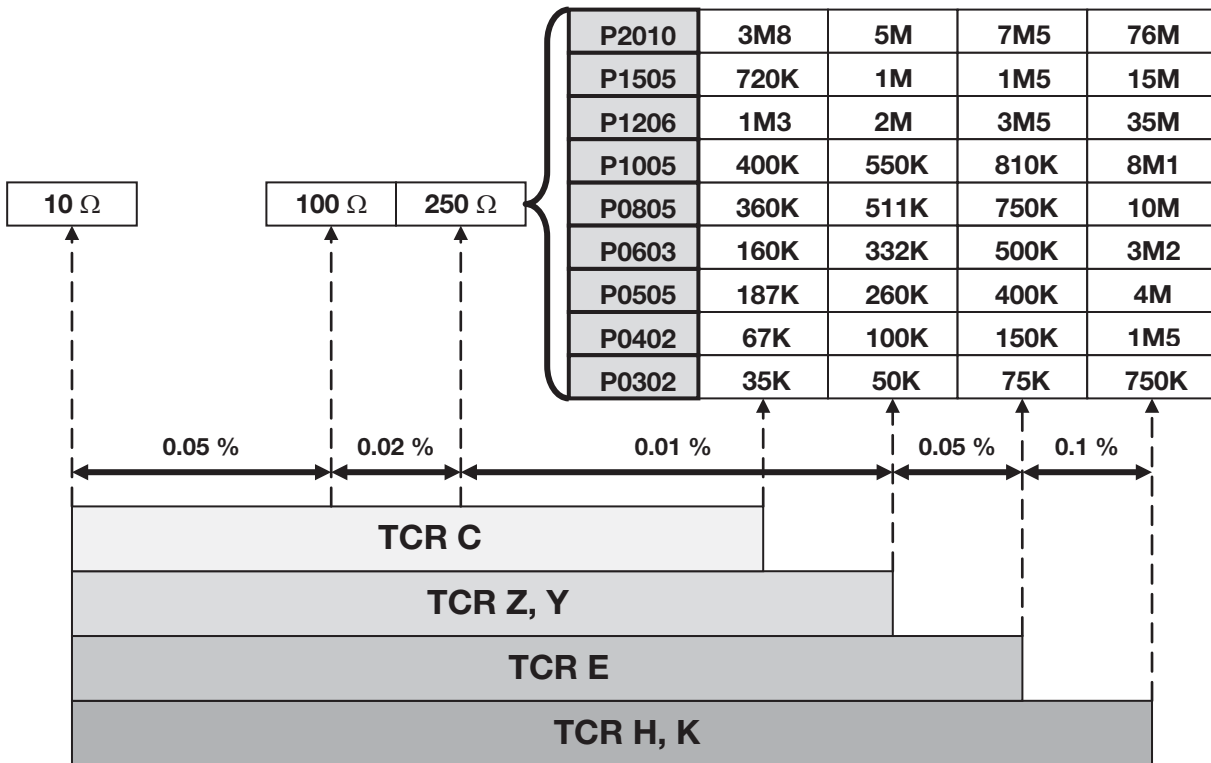
TCR	CODE	FILM
± 5 ppm/°C ⁽¹⁾	C (- 55 °C; + 155 °C)	NiCr
± 5 ppm/°C ⁽¹⁾	Z (0 °C; + 70 °C)	NiCr
± 10 ppm/°C ⁽¹⁾	Y	NiCr
± 25 ppm/°C	E	NiCr
± 50 ppm/°C	H	NiCr or CrSi
± 100 ppm/°C	K	NiCr or CrSi

Note
⁽¹⁾ R > 39 Ω on request for lower values.

POWER DERATING CURVE



BEST TOLERANCE AND TCR VS. OHMIC VALUE



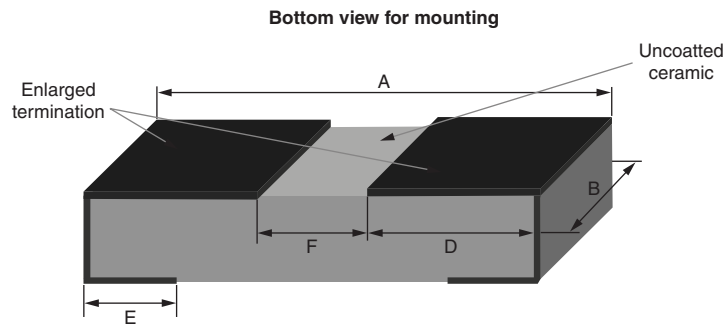
POPULAR OPTIONS

For any option it is recommended to consult Vishay Sfernice for availability first.

Option: Enlarged terminations:

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heatsink (see application note: 53048 Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film) www.vishay.com/doc?53048).

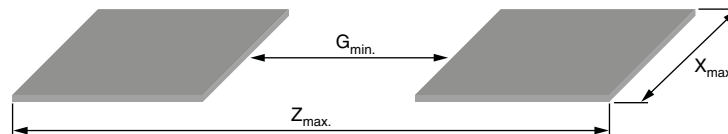
Option to order: 0063 (applies to size 1206/1505/2010).

DIMENSIONS (Option 0063) in millimeters


CASE SIZE	A	B	E	D	F		
	MAX. TOL. + 0.152 MIN. TOL. - 0.152	MAX. TOL. + 0.127 MIN. TOL. - 0.127	MAX. TOL. + 0.13 MIN. TOL. - 0.13	MAX. TOL. + 0.13 MIN. TOL. - 0.13	NOMINAL	MIN.	MAX.
	NOMINAL	NOMINAL	NOMINAL	NOMINAL	NOMINAL	MIN.	MAX.
1206	3.06	1.60	0.40	1.215	0.63	0.50	0.76
1505	3.81	1.32	0.48	1.59			
2010	5.08	2.54		2.25			

Note

- Case size 2512 under development. Please consult Vishay Sfernice.

SUGGESTED LAND PATTERN (Option 0063)


CHIP SIZE	DIMENSIONS (IN MILLIMETER)		
	Z _{max.}	G _{min.}	X _{max.}
1206	3.91	0.50	1.73
1505	4.66		1.45
2010	5.93		2.67

Note

- Case size 2512 under development. Please consult Vishay Sfernice.



Option: Marking

Option to order 0013:

Marking of ohmic value and tolerance:

Sizes: 0805 to 1005: 3 digits marking (according to EIA-96)

Sizes: 1206 to 2010: 4 digits marking (same codification than in the ordering procedure)

Tolerance indicated by a color dot.

Option to order 0014:

Marking of ohmic value:

Sizes: 0805 to 1005: 3 digits marking (according to EIA-96)

Sizes: 1206 to 2010: 4 digits marking (same codification than in the ordering procedure)

No standard marking available for smaller sizes.

A price adder will apply to the unit price of the parts for options 0013 and 0014.

Option: AEC-Q200

Moisture resistance

Option to Order 0058:

Specific production process to withstand 85 °C/85 % at Pn/10

PACKAGING

ESD packaging available: waffle-pack, and plastic tape and reel (low conductivity). Paper tape available upon request (ESD only) (for size 0603, 0805, and 1206).

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
		WAFFLE PACK 2" x 2"	TAPE AND REEL		
			MIN.	MAX.	
0302	100	100	100	5000	8 mm
0402					
0505					
0603					
0805 0705					
1005		221	4000	2000	8 mm
1206		140			
1505		60			
2010			100		

PACKAGING RULES

Waffle Pack

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.

To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code.

Tape and Reel

Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided.

When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code.

PERFORMANCE			
TESTS	CONDITIONS	MIL OR CECC REQUIREMENTS	TYPICAL PERFORMANCES
Thermal shock	MIL-PRF-55342G MIL-STD-202 F-Method 107 F	± 0.05 %	± 0.02 %
Short time overload	MIL-PRF-55342G PARA 3.10.4.7.5	± 0.05 %	± 0.01 %
Low temperature operation	MIL-PRF-55342G PARA 3.9 and 4.7.4	± 0.05 %	± 0.01 %
Resistance to solder heat	MIL-PRF-55342G PARA 3.12, 4.7.7, 4.7.1.2	± 0.05 %	± 0.03 %
Moisture resistance	MIL-PRF-55342G PARA 3.13 and 4.7.8 MIL-STD-202 F-Method 106 E	± 0.10 %	± 0.01 %
	CECC 56 days/40 °C/93 % RH	± 0.10 %	± 0.01 %
	AEC-Q200 ⁽²⁾ 85 °C/85 % RH/Pn/10 1000 h	± 0.5 % + 0.05 Ω	Max. < 0.3 % + 0.05 Ω
High temperature	MIL-PRF-55342G PARA 3.11 and 4.7.6	± 0.05 %	± 0.05 %
Load life	MIL-PRF-55342G 2000 h Pn at 70 °C MIL-STD-202 F-Method 108 A	± 0.5 %	± 0.10 % ⁽¹⁾

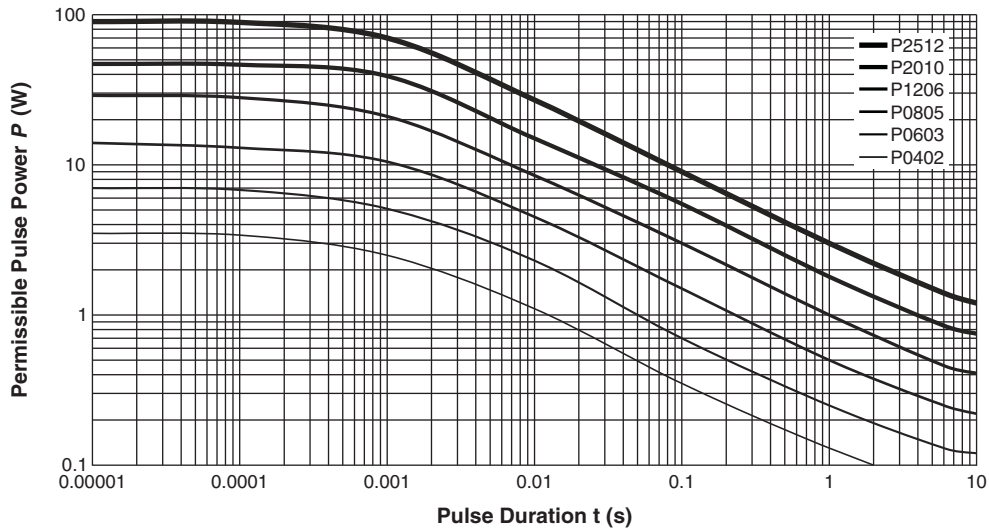
Notes

⁽¹⁾ 0.05 % under Pd

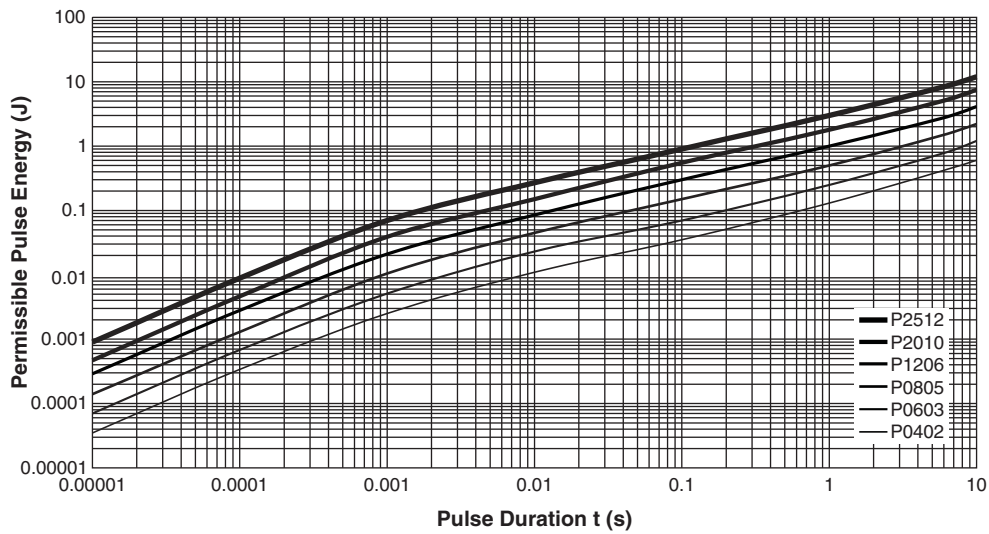
⁽²⁾ Option to order



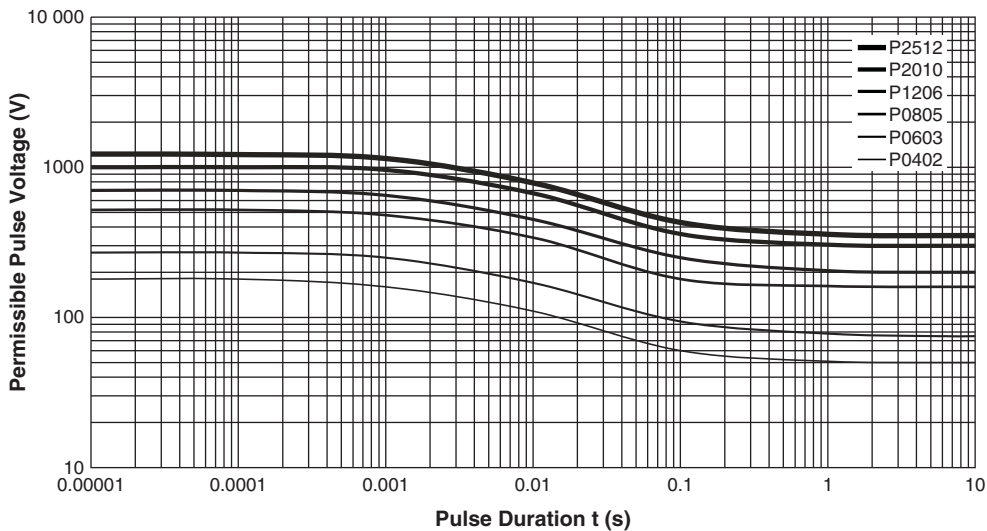
Maximum permissible pulse load P_i max. for single pulse



Energy for single pulse

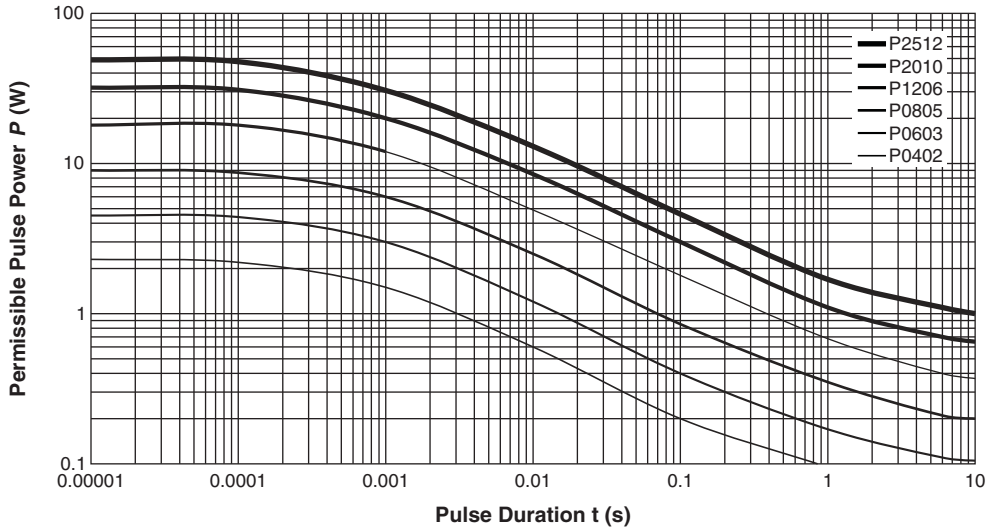


Maximum permissible pulse voltage U_i max.

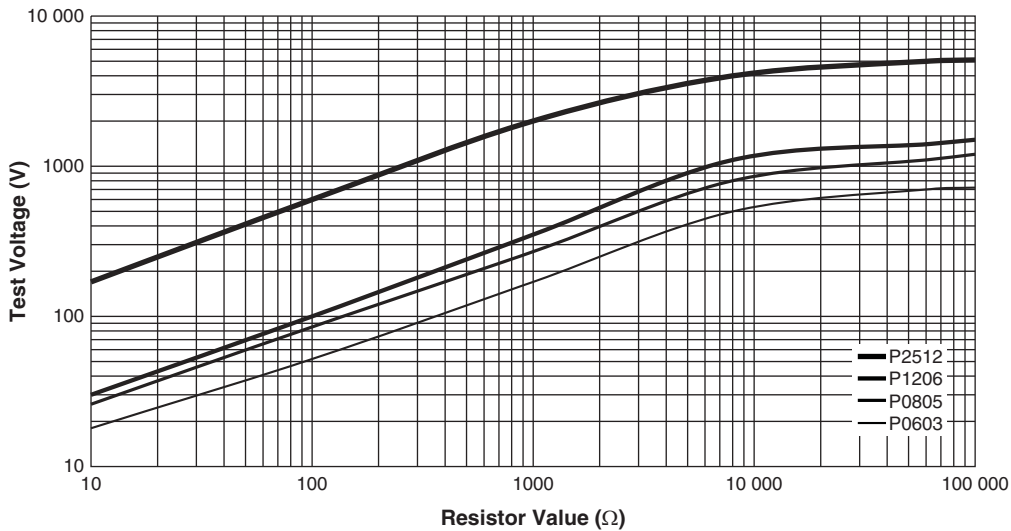




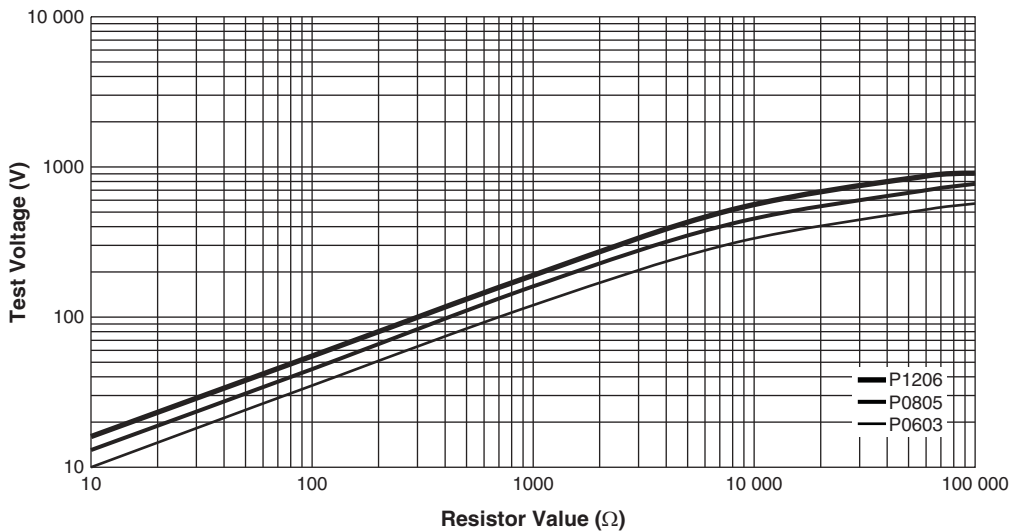
Maximum permissible pulse load P_i max.



1.2/50 μ s lightning surge



10/700 μ s lightning surge





GLOBAL PART NUMBER INFORMATION																
New Global Part Numbering: P0505Y1003BBT0999																
P	0	5	0	5	Y	1	0	0	3	B	B	T	0	9	9	9
GLOBAL MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION	PACKAGING	OPTION									
P	0302 0402 0505 0603 0705 0805 1005 1206 1505 2010	K = ± 100 ppm/°C H = ± 50 ppm/°C E = ± 25 ppm/°C Y = ± 10 ppm/°C Z = ± 5 ppm (0.70 °C) C = ± 5 ppm (- 55 °C; + 155 °C)	The first three digits are significant figures and the last digit specifies the number of zeros to follow, R designates decimal point 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ	L = ± 0.01 % P = ± 0.02 % W = ± 0.05 % B = ± 0.1 % C = ± 0.25 % D = ± 0.5 % F = ± 1 % G = ± 2 % J = ± 5 %	B: SnPb over nickel barrier N: SnAg over nickel barrier G: Gold over nickel barrier B: Lead bearing version N and G: Lead (Pb)-free/RoHS version	Blank = Waffle pack T = Tape ⁽¹⁾ PT = Paper tape ⁽²⁾	Leave blank if no option									
Historical Part Number example: P 0505 Y 1003 B B TR R0999 e2																
HISTORICAL MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION	PACKAGING	OPTION	RoHS								
P	0302 0402 0505 0603 0705 0805 1005 1206 1505 2010	K = ± 100 ppm/°C H = ± 50 ppm/°C E = ± 25 ppm/°C Y = ± 10 ppm/°C Z = ± 5 ppm (0.70 °C) C = ± 5 ppm (- 55 °C; + 155 °C)	The first three digits are significant figures and the last digit specifies the number of zeros to follow, R designates decimal point 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ	L = ± 0.01 % P = ± 0.02 % W = ± 0.05 % B = ± 0.1 % C = ± 0.25 % D = ± 0.5 % F = ± 1 % G = ± 2 % J = ± 5 %	B: SnPb over nickel barrier N: SnAg over nickel barrier G: Gold over nickel barrier B: Lead bearing version N and G: Lead (Pb)-free/RoHS version	Blank = Waffle pack TR = Tape ⁽¹⁾	Leave blank if no option	e2: Tin/silver e4: Gold Blank: SnPb								

Notes

- (1) For specific quantity of parts per packaging please consult Vishay Sfernice.
- (2) For paper tape please consult Vishay Sfernice (0603, 0805, and 1206 only).

QUICK PROTOTYPING

Vishay Sfernice can offer quick prototyping service in 3 weeks production time for most popular case sizes: 0603, 0805, 1206 (Best tolerance: 0.05 %, best TCR: 10 ppm/°C) - Premium will apply - Check availability

PTRIM

Chips ready to be trimmed available. Please consult Vishay Sfernice.

Notes

- For CECC qualified, see RV datasheet (www.vishay.com/doc?60022)
- For ESCC qualified, see PHR datasheet (www.vishay.com/doc?53037) or PFRR datasheet (www.vishay.com/doc?53046)
- For High Temperature (230 °C), see PHT datasheet (www.vishay.com/doc?53050)
- For Strap (0 Ω), see PZR datasheet (www.vishay.com/doc?53053)



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