

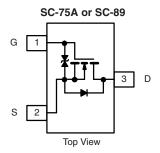
HALOGEN

FREE



# N-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (mA)		
	0.70 at V <sub>GS</sub> = 4.5 V	600		
20	0.85 at V <sub>GS</sub> = 2.5 V	500		
	1.25 at V <sub>GS</sub> = 1.8 V	350		



ORDERING INFORMATION					
Part Number	Package	Marking Code			
Si1012R-T1-GE3 (Lead (Pb)-free and Halogen-free)	SC-75A (SOT-416)	С			
Si1012X-T1-GE3 (Lead (Pb)-free and Halogen-free)	SC-89 (SOT-490)	Α			

#### **FEATURES**

TrenchFET® Power MOSFET: 1.8 V Rated

Gate-Source ESD Protected: 2000 V

High-Side Switching

Low On-Resistance: 0.7  $\Omega$ 

Low Threshold: 0.8 V (typ.)

Fast Switching Speed: 10 ns

Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

### **APPLICATIONS**

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- **Battery Operated Systems**
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

### **BENEFITS**

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- **High-Speed Circuits**
- Low Battery Voltage Operation

<b>ABSOLUTE MAXIMUM RATINGS</b> (	$\Gamma_A = 25  ^{\circ}\text{C}$ , unless	otherwise no	ted)		
Parameter	Symbol	5 s	Steady State	Unit	
Drain-Source Voltage	V <sub>DS</sub>	20		V	
Gate-Source Voltage		V <sub>GS</sub>	± 6		
0 11 D 1 O 1 (T 150 00)h	T <sub>A</sub> = 25 °C	I-	600	500	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>b</sup>	T <sub>A</sub> = 85 °C	I <sub>D</sub>	400	350	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	1000		mA
Continuous Source Current (Diode Conduction) <sup>b</sup>		I <sub>S</sub>	275	250	İ
M : D D: : :: ht 00.75	T <sub>A</sub> = 25 °C		175	150	mW
Maximum Power Dissipation <sup>b</sup> for SC-75	T <sub>A</sub> = 85 °C	1 , [	90	80	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	275	250	
Maximum Power Dissipation <sup>b</sup> for SC-89	T <sub>A</sub> = 85 °C		160	140	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000		V

- a. Pulse width limited by maximum junction temperature.
- b. Surface mounted on FR4 board.

# Si1012R, Si1012X

# Vishay Siliconix



<b>SPECIFICATIONS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.		Max.	Unit	
Static							
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.45		0.9	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 4.5 \text{ V}$		± 0.5	± 1	μΑ	
7 0	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V		0.3	100	nA	
Zero Gate Voltage Drain Current		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			5	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	700			mA	
	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 600 \text{ mA}$		0.41	0.70		
Drain-Source On-State Resistance <sup>a</sup>		$V_{GS} = 2.5 \text{ V}, I_D = 500 \text{ mA}$		0.53	0.85	Ω	
		$V_{GS} = 1.8 \text{ V}, I_D = 350 \text{ mA}$		0.70	1.25		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = 10 \text{ V}, I_{D} = 400 \text{ mA}$		1		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = 150 mA, V <sub>GS</sub> = 0 V		0.8	1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	$Q_g$			750			
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 250 \text{ mA}$		75		pC	
Gate-Drain Charge	$Q_{gd}$			225			
Turn-On Delay Time	t <sub>d(on)</sub>			5			
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 47 $\Omega$		5		ns	
Turn-Off Delay Time	t <sub>d(off)</sub>	$\text{I}_\text{D}\cong \text{200 mA},~\text{V}_\text{GEN}=\text{4.5 V},~\text{R}_\text{g}=\text{10}~\Omega$		25			
Fall Time	t <sub>f</sub>			11			

#### Notes:

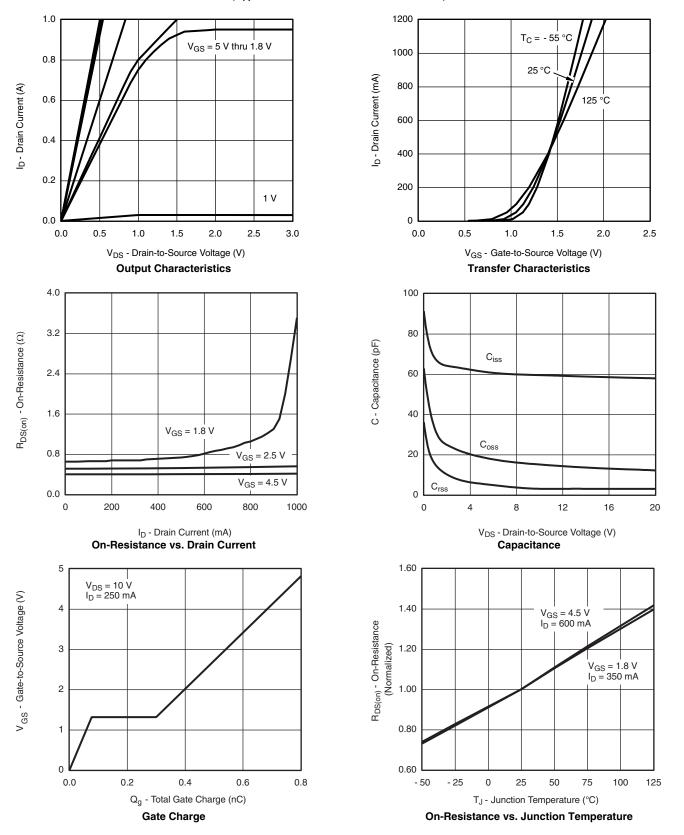
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

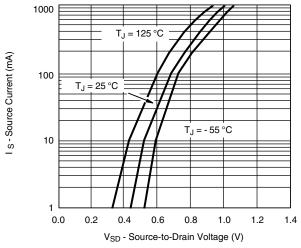


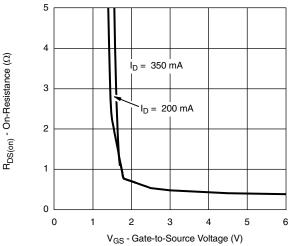
## TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



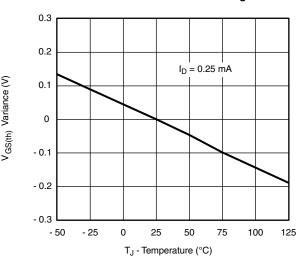
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## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

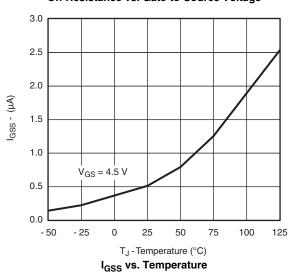




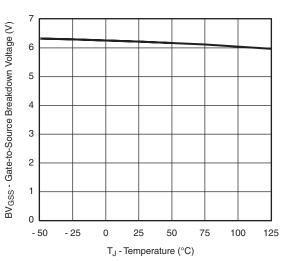
### Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



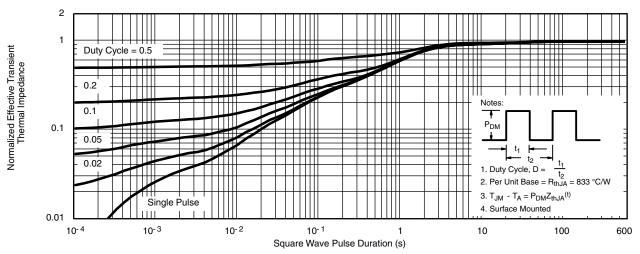
Threshold Voltage Variance vs. Temperature



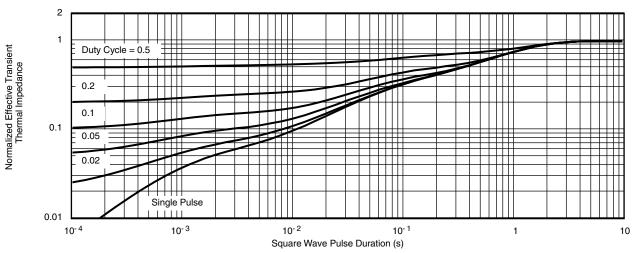
BV<sub>GSS</sub> vs. Temperature



# **TYPICAL CHARACTERISTICS** ( $T_A = 25$ °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (SC-75A)

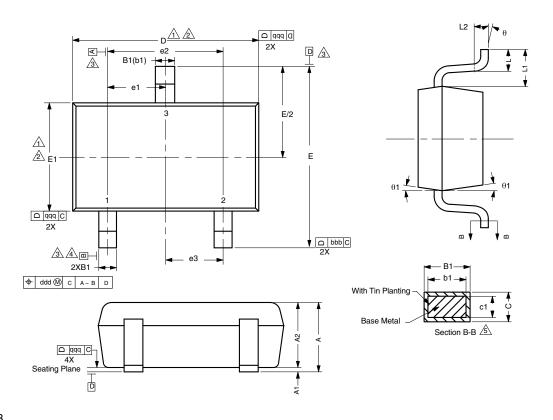


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg?71166">www.vishay.com/ppg?71166</a>.



## SC-75A: 3 Leads



DWG: 5868

#### Notes

Dimensions in millimeters will govern.

- Dimension D does not include mold flash, protrusions or gate burrs. Mold flash protrusions or gate burrs shall not exceed 0.10 mm per end. Dimension E1 does not include Interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.10 mm per side.
- Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
- ②Datums A, B and D to be determined 0.10 mm from the lead tip.

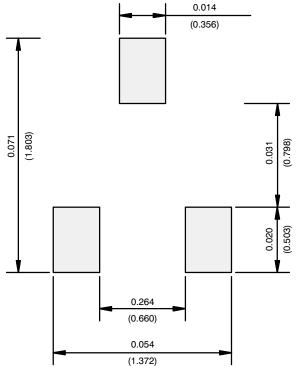
  4\text{Terminal positions are shown for reference only.}
- These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIMENSIONS	TOLERANCES
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.10

DIM.	N	NOTE		
Dilvi.	MIN.	NOM.	MAX.	NOTE
А	-	-	0.80	
A1	0.00	-	0.10	
A2	0.65	0.70	0.80	
B1	0.19	-	0.24	5
b1	0.17	-	0.21	
С	0.13	-	0.15	5
c1	0.10	-	0.12	5
D	1.48	1.575	1.68	1, 2
Е	1.50	1.60	1.70	
E1	0.66	0.76	0.86	1, 2
e1	0.50 BSC			
e2	1.00 BSC			
e3	0.50 BSC			
L	0.15	0.205	0.30	
L1	0.40 ref.			
L2	0.15 BSC			
q	0°	-	8°	
q1	4°	-	10°	



## **RECOMMENDED MINIMUM PADS FOR SC-75A: 3-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE



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Revision: 02-Oct-12 Document Number: 91000

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IPS70R2K0CEAKMA1 BUK954R8-60E DMN3404LQ-7 NTE6400 SQJ402EP-T1-GE3 2SK2614(TE16L1,Q) 2N7002KW-FAI

DMN1017UCP3-7 EFC2J004NUZTDG ECH8691-TL-W FCAB21350L1 P85W28HP2F-7071 DMN1053UCP4-7 NTE221 NTE2384

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