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Vishay Siliconix

# N-Channel 30 V (D-S) MOSFET

# SOT-23 (TO-236) D 3 2 S

Top View

Marking code: P4

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	30				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10 \text{ V}$	0.060				
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5 \text{ V}$	0.075				
Q <sub>g</sub> typ. (nC)	2.1				
I <sub>D</sub> (A) <sup>a</sup>	3.6				
Configuration	Single				

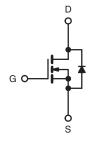
#### **FEATURES**

- TrenchFET® power MOSFET
- 100 % R<sub>g</sub> tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



#### **APPLICATIONS**

• DC/DC converter



N-Channel MOSFET

ORDERING INFORMATION				
Package	SOT-23			
Lead (Pb)-free and halogen-free	Si2304DDS-T1-GE3			

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	30	V	
Gate-source voltage		$V_{GS}$	± 20	V	
	T <sub>C</sub> = 25 °C		3.6 <sup>a</sup>	A	
Continuous dusin suggest /T 150 °C\	T <sub>C</sub> = 70 °C	Ι,	3.3		
Continuous drain current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	l <sub>D</sub>	3.3		
	T <sub>A</sub> = 70 °C		2.7		
Pulsed drain current		I <sub>DM</sub>	15		
Continuous source-drain diode current	T <sub>C</sub> = 25 °C	I <sub>S</sub>	1.4		
	T <sub>A</sub> = 25 °C		0.9 b, c		
Maximum power dissipation	T <sub>C</sub> = 25 °C	_	1.7	W	
	T <sub>C</sub> = 70 °C		1.1		
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	1.1 <sup>b, c</sup>		
	T <sub>A</sub> = 70 °C		0.7 b, c		
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering recommendations (peak temperature) d, e			260		

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient b, d	t ≤ 5 s	R <sub>thJA</sub>	90	115	°C/W		
Maximum junction-to-foot (drain)	Steady state	R <sub>thJF</sub>	60	75	- C/VV		

#### Notes

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 5 s
- d. Maximum under steady state conditions is 130  $^{\circ}\text{C/W}$



# Vishay Siliconix

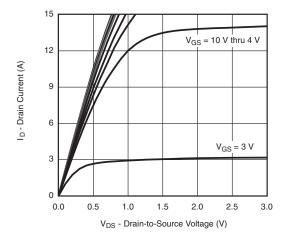
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			<u>'</u>				
Drain-source breakdown voltage	$V_{DS}$	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	30	-	-	V	
V <sub>DS</sub> temperature coefficient	$\Delta V_{DS}/T_{J}$	1 050 A	-	31	-		
V <sub>GS(th)</sub> temperature coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA	-	-5	-	mV/°C	
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.2	-	2.2	V	
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA	
7		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V	-	-	1		
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	10	μA	
On-state drain current a	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	10	-	-	Α	
<b>D</b>		$V_{GS} = 10 \text{ V}, I_D = 3.2 \text{ A}$	-	0.049	0.060	Ω	
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 2.8 \text{ A}$	-	0.061	0.075		
Forward transconductance a	9 <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_D = 4.8 \text{ A}$	-	11	-	S	
Dynamic <sup>b</sup>			1	1			
Input capacitance	C <sub>iss</sub>		-	235	-		
Output capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	45	-	pF	
Reverse transfer capacitance	C <sub>rss</sub>		-	17	-	1	
Total gate charge	Qg	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 3.4 \text{ A}$	-	4.5	6.7	nC	
			-	2.1	3.2		
Gate-source charge	Q <sub>qs</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 3.4 \text{ A}$	-	0.85	-		
Gate-drain charge	Q <sub>ad</sub>			0.65	-		
Gate resistance	R <sub>q</sub>	f = 1 MHz	0.8	4.4	8.8	Ω	
Turn-on delay time	t <sub>d(on)</sub>		-	12	20		
Rise time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_L = 5.6 \Omega,$	-	50	75	1	
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 2.7 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	12	20		
Fall time	t <sub>f</sub>		-	22	35		
Turn-on delay time	t <sub>d(on)</sub>		-	5	10	ns	
Rise time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_L = 5.6 \Omega,$	-	12	20		
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong 2.7 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	10	15	1	
Fall time	t <sub>f</sub>		-	5	10	1	
<b>Drain-Source Body Diode Characteristi</b>	cs		1	1			
Continuous source-drain diode current	Is	T <sub>C</sub> = 25 °C	-	-	1.4		
Pulse diode forward current	I <sub>SM</sub>		-	-	15	Α	
Body diode voltage	V <sub>SD</sub>	$I_S = 2.7 \text{ A}, V_{GS} = 0 \text{ V}$	-	0.8	1.2	V	
Body diode reverse recovery time	t <sub>rr</sub>		-	10	20	ns	
Body diode reverse recovery charge	Q <sub>rr</sub>	$I_F = 2.7 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	5	10	nC	
Reverse recovery fall time	t <sub>a</sub>	$T_J = 25  ^{\circ}C$	-	6	-		
Reverse recovery rise time	t <sub>b</sub>		_	4	-	ns	

#### Notes

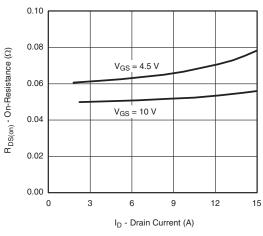
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

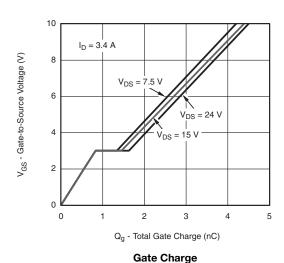


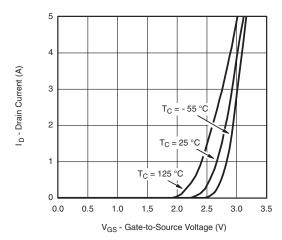


#### **Output Characteristics**

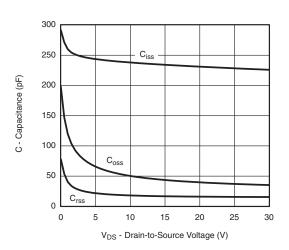


#### On-Resistance vs. Drain Current and Gate Voltage

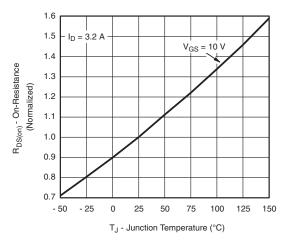




#### **Transfer Characteristics**

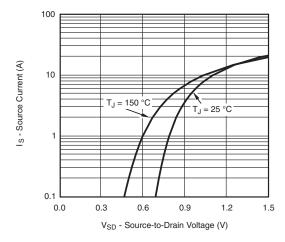


#### Capacitance

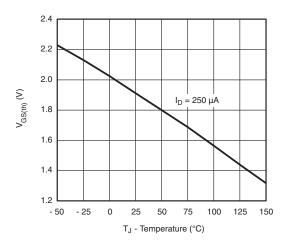


On-Resistance vs. Junction Temperature

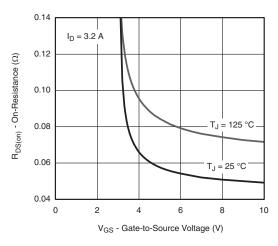




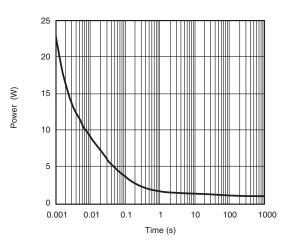
#### Source-Drain Diode Forward Voltage



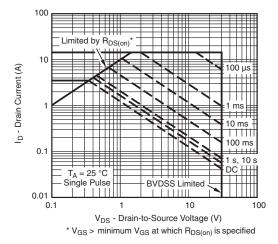
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage

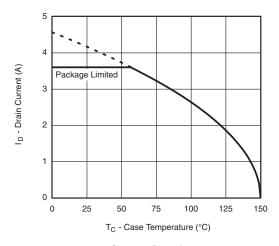


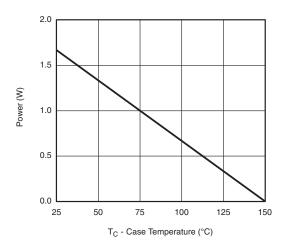
Single Pulse Power



Safe Operating Area, Junction-to-Ambient







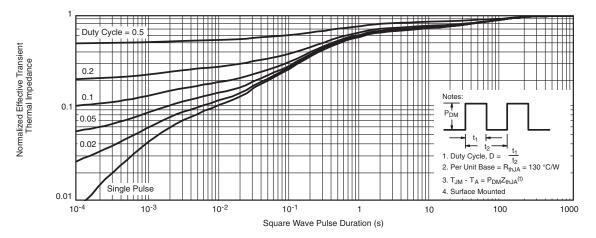
**Power Derating** 

#### Current Derating a

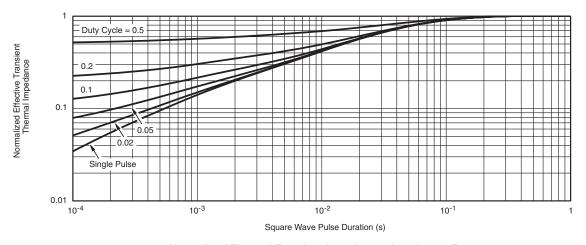
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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# SOT-23 (TO-236): 3-LEAD







Dim	MILLI	METERS	INCHES		
	Min	Max	Min	Max	
Α	0.89	1.12	0.035	0.044	
A <sub>1</sub>	0.01	0.10	0.0004	0.004	
A <sub>2</sub>	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E <sub>1</sub>	1.20	1.40	0.047	0.055	
е	0.95 BSC		0.0374 Ref		
e <sub>1</sub>	1.90 BSC		0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L <sub>1</sub>	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	
FCN: S-03946-Rev K 09-	lul-01	•			

ECN: S-03946-Rev. K, 09-Jul-01

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01



### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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