



# N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ)			
30	0.050 at V <sub>GS</sub> = 10 V	4.5	3.16 nC			
	0.080 at V <sub>GS</sub> = 4.5 V	3.4				

### **FEATURES**

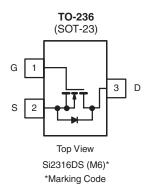
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- PWM Optimized
- 100 % R<sub>q</sub> tested
- Compliant to RoHS Directive 2002/95/EC



ROHS COMPLIANT HALOGEN FREE

### **APPLICATIONS**

- · Battery Switch
- DC/DC Converter



Ordering Information: Si2316BDS-T1-E3 (Lead (Pb)-free)

Si2316BDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Limit	Unit				
Drain-Source Voltage	V <sub>DS</sub>	30	V				
Gate-Source Voltage	V <sub>GS</sub>	± 20	¬				
	T <sub>C</sub> = 25 °C		4.5				
Continuous Drain Current (T = 150 °C)	T <sub>C</sub> = 70 °C	]	3.6	A			
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	3.9 <sup>b, c</sup>				
	T <sub>A</sub> = 70 °C		3.13 <sup>b, c</sup>				
Pulsed Drain Current	I <sub>DM</sub>	20	1				
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		1.39				
Continuous Source-Diairi Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	1.04 <sup>b, c</sup>				
	T <sub>C</sub> = 25 °C		1.66				
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	ь	1.06	W			
Maximum Power Dissipation	T <sub>A</sub> = 25 °C	$P_{D}$	1.25 <sup>b, c</sup>				
	T <sub>A</sub> = 70 °C		0.8 <sup>b, c</sup>	ĺ			
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stq</sub>	- 55 to 150	°C				

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>b, d</sup>	≤ 5 s	R <sub>thJA</sub>	80	100	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	60	75	C/ <b>VV</b>		

### Notes:

- a. Based on  $T_C$  = 25 °C.
- b. Surface mounted on 1" x 1" FR4 moard.
- c. t = 5 s.
- d. Maximum under Steady State conditions is 130 °C/W.

# **Si2316BDS**

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MOSFET SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				,			
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{DS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	30			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		23.92		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	-		5.2		IIIV/ C	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1		3	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	Inno	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			1	μΑ	
Zero date voltage Brain Guiterit	I <sub>DSS</sub>				10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
Drain-Source On-State Resistance <sup>a</sup>	D	$V_{GS} = 10 \text{ V}, I_D = 3.9 \text{ A}$		0.041	0.050		
Diain-Source On-State nesistance	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 3.3 \text{ A}$		0.064	0.080	Ω	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = 15V, I_D = 3.9 A$		6		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			350			
Output Capacitance	C <sub>oss</sub>	V 45VV 6V/ 44V		65		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		37			
Total Cata Charres	$Q_g$	$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 3.9 \text{ A}$		6.35	9.6	-	
Total Gate Charge				3.16	4.8		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 3.9 \text{ A}$		1.56			
Gate-Drain Charge	Q <sub>qd</sub>			1.1			
Gate Resistance	R <sub>q</sub>	f = 1 MHz		2.6	3.9	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			4.5	6.75	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_1 = 4.8 \Omega$		11	16.5		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 3.13 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 1 \Omega$		12	18		
Fall Time	t <sub>f</sub>			7	10.5		
Turn-On Delay Time	t <sub>d(on)</sub>			20	30	- ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 15 \text{ V}, R_{I} = 6.25 \Omega$		65	98		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D = 2.4 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		11	17		
Fall Time	t <sub>f</sub>	_		23	35	1	
Drain-Source Body Diode Characteristi					1		
Continuous Source-Drain Diode Current	Is	T <sub>C</sub> = 25 °C			1.39		
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>	<u> </u>			20	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 2.0 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	<u>-</u>		10	15	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			4	6	nC	
Reverse Recovery Fall Time	ta	$I_F = 2.0 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		6.6			
Reverse Recovery Rise Time	t <sub>b</sub>			3.5		ns	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

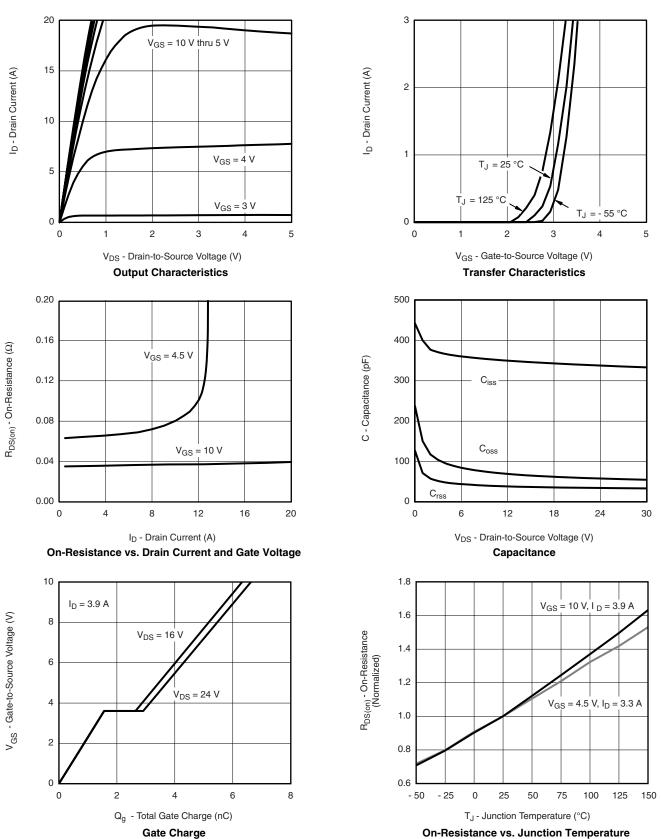
Notes: a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %. b. Guaranteed by design, not subject to production testing.







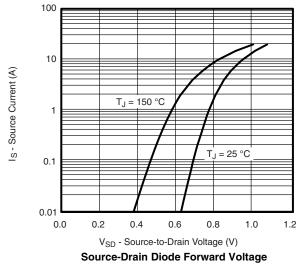
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

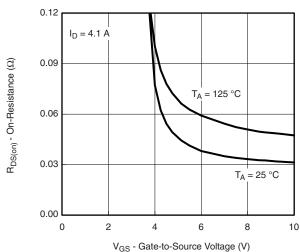


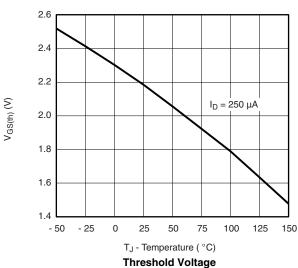
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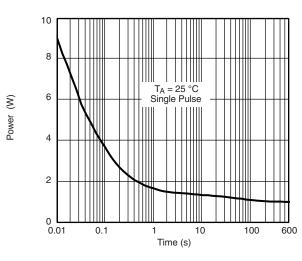
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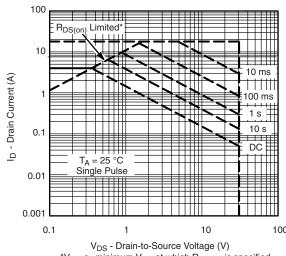




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power

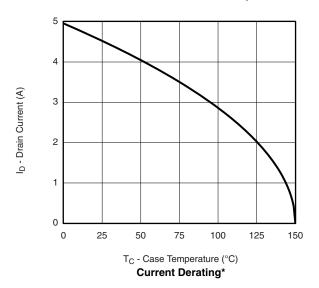


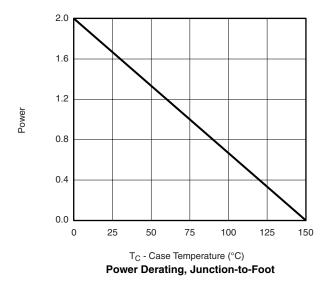
 $v_{DS}$  - Drain-to-Source voltage (V)  $v_{CS}$  > minimum  $v_{CS}$  at which  $v_{DS(on)}$  is specified

Safe Operating Area

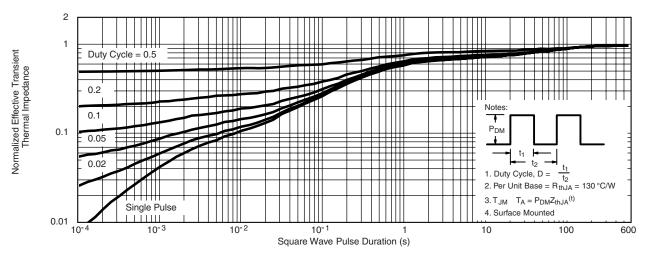


### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





\*The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg270445">www.vishay.com/ppg270445</a>.

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### SOT-23 (TO-236): 3-LEAD







Dim	MILLI	METERS	INCHES			
	Min	Max	Min	Max		
Α	0.89	1.12	0.035	0.044		
A <sub>1</sub>	0.01	0.10	0.0004	0.004		
A <sub>2</sub>	0.88	1.02	0.0346	0.040		
b	0.35	0.50	0.014	0.020		
С	0.085	0.18	0.003	0.007		
D	2.80	3.04	0.110	0.120		
E	2.10	2.64	0.083	0.104		
E <sub>1</sub>	1.20	1.40	0.047	0.055		
е	0.9	0.95 BSC		4 Ref		
e <sub>1</sub>	1.9	0 BSC	0.074			
L	0.40	0.60	0.016	0.024		
L <sub>1</sub>	0.64 Ref		0.025 Ref			
S	0.5	50 Ref	0.020 Ref			
q	3°	8°	3°	8°		
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### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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