



N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
40	0.045 at V _{GS} = 10 V	3.9		
	0.058 at V _{GS} = 4.5 V	3.5		

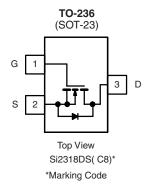
FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET



APPLICATIONS

- · Stepper Motors
- Load Switch



Ordering Information: Si2318DS-T1-E3 (Lead (Pb)-free)

Si2318DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted						
Parameter		Symbol	5 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	40		V	
Gate-Source Voltage		V _{GS}	± 20			
Continuous Dunin Comment /T 150 90\d.b	T _A = 25 °C	- I _D	3.9	3.0		
Continuous Drain Current (T _J = 150 °C) ^{a, b}	T _A = 70 °C		3.1	2.4		
Pulsed Drain Current ^b		I _{DM}	16		Α	
Continuous Source Current (Diode Conduction) ^{a, b}		I _S	0.8			
Danis Diadication A h	T _A = 25 °C	- P _D	1.25	0.75	W	
Power Dissipation ^{a, b}	T _A = 70 °C] 'D	0.8	0.48] **	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Manifestore boarding to Applicants	t ≤ 5 s	R _{thJA}	75	100	
Maximum Junction-to-Ambient ^a	Steady State	' 'thJA	120	166	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	40	50	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. Pulse width limited by maximum junction temperature

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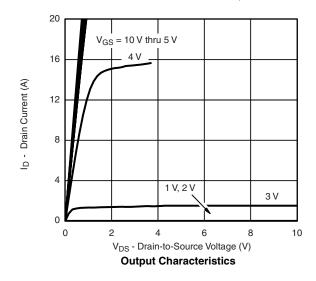


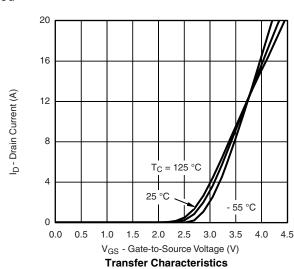
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
			Limits				
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	40			V	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$	1		3	•	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zava Cata Valtaga Drain Current	1	$V_{DS} = 32 \text{ V}, V_{GS} = 0 \text{ V}$			0.5		
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 32 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 4.5 \text{ V}, V_{GS} = 10 \text{ V}$	6			Α	
		$V_{GS} = 10 \text{ V}, I_D = 3.9 \text{ A}$		0.036	0.045	Ω	
Drain-Source On-Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 3.5 \text{ A}$		0.045	0.058		
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 3.9 \text{ A}$		11		S	
Diode Forward Voltage	V_{SD}	I _S = 1.25 A, V _{GS} = 0 V		0.8	1.2	V	
Dynamic ^b				•			
Total Gate Charge	Q_g			10	15		
Gate-Source Charge	Q_{gs}	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 3.9 \text{ A}$		1.6		nC	
Gate-Drain Charge	Q_{gd}			2.1			
Gate Resistance	R_g			1.8		Ω	
Input Capacitance	C _{iss}			540			
Output Capacitance	C _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		80		pF	
Reverse Transfer Capacitance	C _{rss}			45			
Switching				•			
Turn-On Delay Time	t _{d(on)}			5	10	_	
Rise Time	t _r	V_{DD} = 20 V, R_L = 20 Ω		12	20	200	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1.0 A, V_{GEN} = 10 V, R_G = 6 Ω		20	30	ns	
Fall Time	t _f			15	25		

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





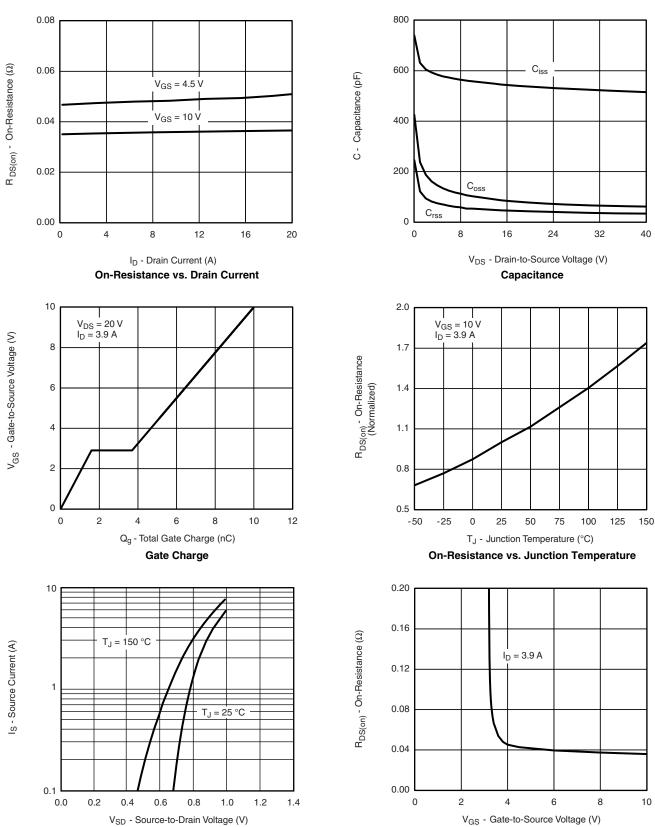
a. Pulse test; PW \leq 300 μ s, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.







TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



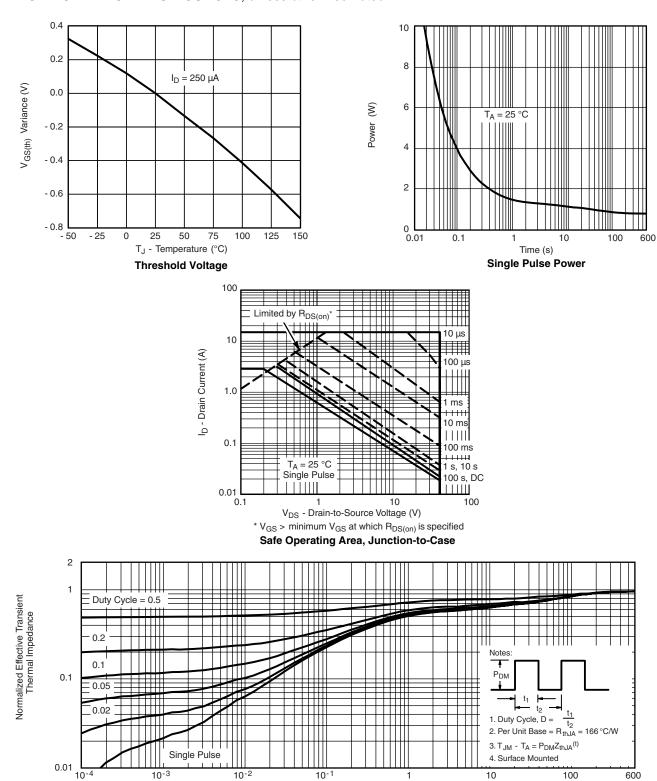
Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Square Wave Pulse Duration (s)
Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72322.

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SOT-23 (TO-236): 3-LEAD







Dim	MILLI	METERS	INCHES			
	Min	Max	Min	Max		
Α	0.89	1.12	0.035	0.044		
A ₁	0.01	0.10	0.0004	0.004		
A ₂	0.88	1.02	0.0346	0.040		
b	0.35	0.50	0.014	0.020		
С	0.085	0.18	0.003	0.007		
D	2.80	3.04	0.110	0.120		
E	2.10	2.64	0.083	0.104		
E ₁	1.20	1.40	0.047	0.055		
е	0.95 BSC		0.0374 Ref			
e ₁	1.90 BSC		0.074	0.0748 Ref		
L	0.40	0.60	0.016	0.024		
L ₁	0.64 Ref		0.025 Ref			
S	0.50 Ref		0.020 Ref			
q	3°	8°	3°	8°		
FCN: S-03946-Rev K 09-	lul-01	•				

ECN: S-03946-Rev. K, 09-Jul-01

DWG: 5479

Document Number: 71196 www.vishay.com 09-Jul-01



RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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