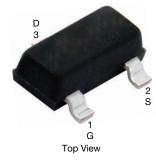


Vishay Siliconix

N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R_{DS(on)} (Ω) MAX.	I _D (A) ^d	Q _g (TYP.)			
	0.030 at V_{GS} = 4.5 V	5.9				
20	0.034 at V _{GS} = 2.5 V	5.5	7.7 nC			
	0.041 at V _{GS} = 1.8 V	5				

SOT-23 (TO-236)



FEATURES

- TrenchFET® power MOSFET
- 100 % R_g tested
- Material categorization: For definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Load switch
- Power management



See COMPLIANT HALOGEN FREE



N-Channel MOSFET

Marking Code: F5

Ordering Information:

Si2374DS-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, un PARAMETER		SYMBOL	LIMIT	UNIT
				UNIT
Drain-Source Voltage		V _{DS}	20	V
Gate-Source Voltage		V _{GS}	± 8	
	T _C = 25 °C		5.9	
Continuous Drain Current (T. 150 °C)	T _C = 70 °C	1, [4.7	
Continuous Drain Current ($T_J = 150 \ ^{\circ}C$)	T _A = 25 °C	I _D	4.5 ^{a, b}	
	T _A = 70 °C	1	3.6 ^{a, b}	А
Pulsed Drain Current (t = 100 µs)		I _{DM}	25	
	T _C = 25 °C		1.4	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	0.8 ^{a, b}	
	T _C = 25 °C		1.7	
Manimum David Diasia atian	T _C = 70 °C		1.1	
Maximum Power Dissipation	T _A = 25 °C	P _D	0.96 ^{a, b}	W
	T _A = 70 °C	1	0.62 ^{a, b}	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum Junction-to-Ambient ^{a, c}	t≤5 s	R _{thJA}	100	130	°C/W		
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	60	75	C/W		

Notes

a. Surface mounted on 1" x 1" FR4 board.

b. t = 5 s.

c. Maximum under steady state conditions is 175 $^{\circ}\text{C/W}.$

d. $T_C = 25 \ ^{\circ}C.$

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Si2374DS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static				•	•		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = 250 \mu A$	20	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	1 050	-	34	-	mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-5	-		
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	0.4	-	1	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 8 V$	-	-	± 100	nA	
Zara Cata Valtaga Drain Current		$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	μA	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$	-	-	10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	10	-	-	А	
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	-	0.025	0.030		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 2.5 V, I_D = 3 A$ - 0		0.028	0.034	Ω	
		V _{GS} = 1.8 V, I _D = 2 A	-	0.031	0.041		
Forward Transconductance ^a	g _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 4 \text{ A}$	-	29	-	S	
Dynamic ^b				•	•	•	
Input Capacitance	Ciss		-	735	-	pF	
Output Capacitance	Coss	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	110	-		
Reverse Transfer Capacitance	C _{rss}		-	40	-		
· · · · · ·	-	$V_{DS} = 10 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 4.5 \text{ A}$	-	13.4	20	20	
Total Gate Charge	Qg		-	7.7	12	nC	
Gate-Source Charge	Q _{gs}	V_{DS} = 10 V, V_{GS} = 4.5 V, I_{D} = 4.5 A	-	1	-		
Gate-Drain Charge	Q _{gd}		-	1	-		
Gate Resistance	Rg	f = 1 MHz	0.12	0.6	1.2	Ω	
Turn-On Delay Time	t _{d(on)}		-	4	8		
Rise Time	t _r	$V_{DD} = 10 \text{ V}, \text{ R}_{L} = 2.8 \Omega$	-	22	33	1	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 3.6$ A, V_{GEN} = 8 V, R_g = 1 Ω	-	16	24		
Fall Time	t _f		-	9	18		
Turn-On Delay Time	t _{d(on)}		-	10	20	ns	
Rise Time	t _r	$V_{DD} = 10 \text{ V}, \text{ R}_{L} = 2.8 \Omega$	-	23	35		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 3.6$ A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	16	24		
Fall Time	t _f		-	10	20		
Drain-Source Body Diode Characteristic	s				1		
Continuous Source-Drain Diode Current			-	-	1.4		
Pulse Diode Forward Current (t = 100 µs)	I _{SM}		-	-	25	A	
Body Diode Voltage	V _{SD}	I _S = 3.6 A, V _{GS} = 0 V	-	0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}		-	13	20	ns	
Body Diode Reverse Recovery Charge	Q _{rr}		-	6	12	nC	
Reverse Recovery Fall Time	ta	$I_F = 3.6 \text{ A}, \text{ dl/dt} = 100 \text{ A/}\mu\text{s}, \text{ T}_J = 25 ^\circ\text{C}$	-	9	-		
Reverse Recovery Rise Time	t _b		-	4	_	ns	

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

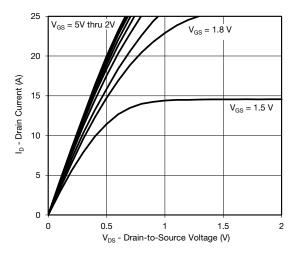
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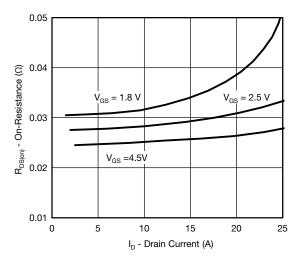


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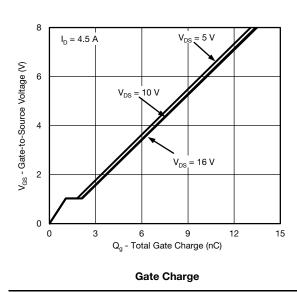
TYPICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise noted)

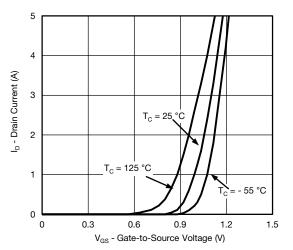


Output Characteristics

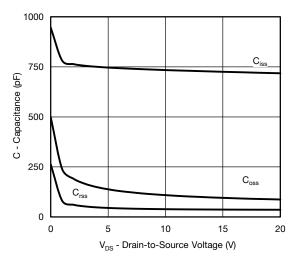


On-Resistance vs. Drain Current and Gate Voltage

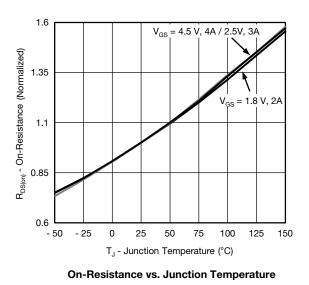




Transfer Characteristics







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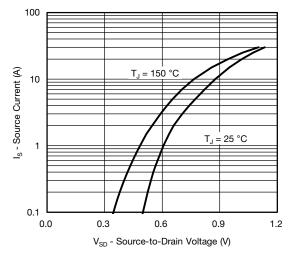
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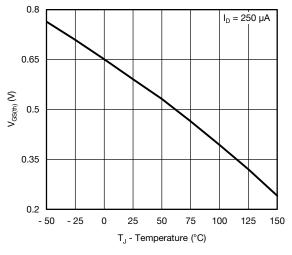


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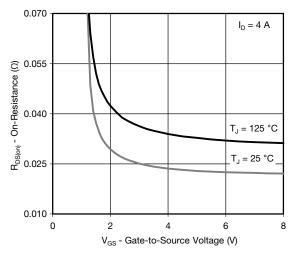
TYPICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise noted)



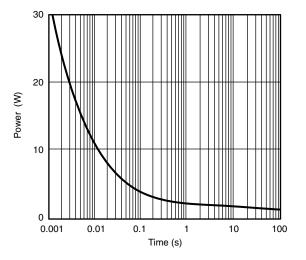
Source-Drain Diode Forward Voltage



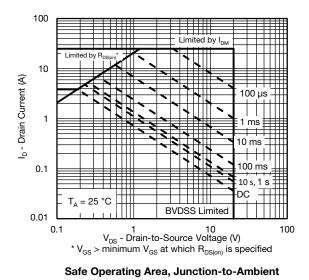




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)



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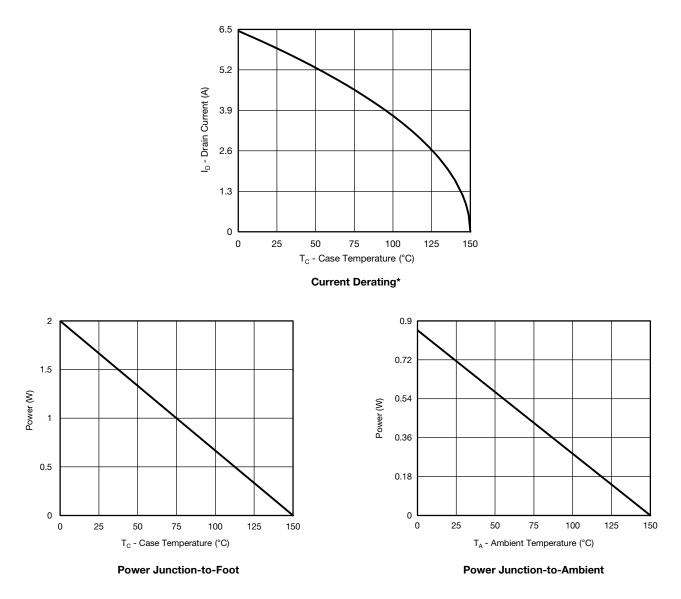
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TYPICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise noted)

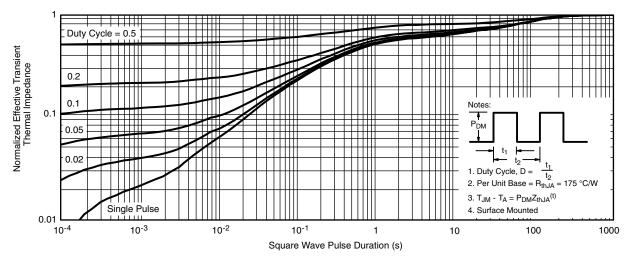


* The power dissipation P_D is based on $T_{J (max.)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

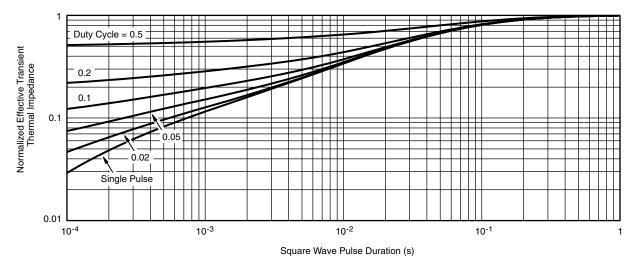


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TYPICAL CHARACTERISTICS (T_J = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62947.



Package Information

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SOT-23 (TO-236): 3-LEAD







Dim	MILLIN	METERS	INCHES		
	Min	Max	Min	Мах	
Α	0.89	1.12	0.035	0.044	
A ₁	0.01	0.10	0.0004	0.004	
A ₂	0.88	1.02	0.0346	0.040	
b	0.35	0.50	0.014	0.020	
С	0.085	0.18	0.003	0.007	
D	2.80	3.04	0.110	0.120	
E	2.10	2.64	0.083	0.104	
E ₁	1.20	1.40	0.047	0.055	
е	0.95 BSC		0.0374 Ref		
e ₁	1.90 BSC		0.0748 Ref		
L	0.40	0.60	0.016	0.024	
L ₁	0.64 Ref		0.025 Ref		
S	0.50 Ref		0.020 Ref		
q	3°	8°	3°	8°	



Application Note 826

Vishay Siliconix

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads Dimensions in Inches/(mm)

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