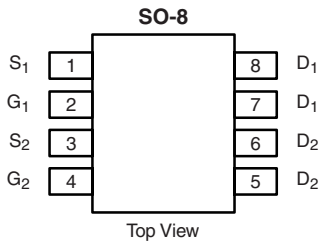


## Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a, e</sup>	Q <sub>g</sub> (Typ.)
Channel-1	30	0.020 at V <sub>GS</sub> = 10 V	8.0	7.3
		0.025 at V <sub>GS</sub> = 4.5 V	8.0	
Channel-2	30	0.020 at V <sub>GS</sub> = 10 V	8.0	7.3
		0.025 at V <sub>GS</sub> = 4.5 V	8.0	

SCHOTTKY PRODUCT SUMMARY		
V <sub>DS</sub> (V)	V <sub>SD</sub> (V) Diode Forward Voltage	I <sub>F</sub> (A) <sup>a</sup>
30	0.51 V at 1.0 A	2.0



Ordering Information: Si4834CDY-T1-E3 (Lead (Pb)-free)  
Si4834CDY-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

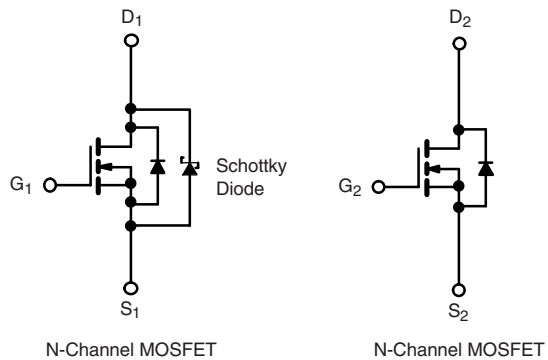
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Notebook Logic dc-to-dc
- Low Current dc-to-dc



ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Channel-1	Channel-2	Unit
Drain-Source Voltage	V <sub>DS</sub>	30	30	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	± 20	V
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>C</sub> = 25 °C	8.0 <sup>e</sup>	8.0 <sup>e</sup>	A
	T <sub>C</sub> = 70 °C	7.1	7.1	
	T <sub>A</sub> = 25 °C	7.5 <sup>b, c</sup>	7.5 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C	5.8 <sup>b, c</sup>	5.8 <sup>b, c</sup>	
Pulsed Drain Current (10 μs Pulse Width)	I <sub>DM</sub>	30	30	A
Source-Drain Current Diode Current	T <sub>C</sub> = 25 °C	2.6	2.6	A
	T <sub>A</sub> = 25 °C	1.8 <sup>b, c</sup>	1.8 <sup>b, c</sup>	
Pulsed Source-Drain Current	I <sub>SM</sub>	30	30	A
Single Pulse Avalanche Current	I <sub>AS</sub>	10	10	A
Single Pulse Avalanche Energy	E <sub>AS</sub>	5	5	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C	2.9	2.9	W
	T <sub>C</sub> = 70 °C	1.8	1.8	
	T <sub>A</sub> = 25 °C	2 <sup>b, c</sup>	2 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C	1.2 <sup>b, c</sup>	1.2 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ.	Max.	Typ.	Max.		
Maximum Junction-to-Ambient <sup>b, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	52	62.5	52	62.5	°C/W
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	35	43	35	43	°C/W

Notes:

- Based on T<sub>C</sub> = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- Maximum under Steady State conditions is 110 °C/W (Channel-1) and 110 °C/W (Channel-2).
- Package limited.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted								
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit		
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	Ch-1	30			V	
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	Ch-2	30				
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-2		32		mV/ $^\circ\text{C}$	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	Ch-2		-6			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	Ch-1	1		3	V	
		$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	Ch-2	1		3		
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1			100	nA	
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-2			100		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1		0.016	0.10	mA	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			0.001		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 100\text{ }^\circ\text{C}$	Ch-1		1.1	10		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 100\text{ }^\circ\text{C}$	Ch-2			0.025		
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20			A	
		$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	20				
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$	Ch-1		0.0156	0.020	$\Omega$	
		$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$	Ch-2		0.0156	0.020		
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-1		0.019	0.025		
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$	Ch-2		0.019	0.025		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 8\text{ A}$	Ch-1		29		S	
		$V_{DS} = 15\text{ V}, I_D = 8\text{ A}$	Ch-2		29			
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	$C_{iss}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		950		pF	
			Ch-2		950			
Output Capacitance	$C_{oss}$		Ch-1		185			
			Ch-2		155			
Reverse Transfer Capacitance	$C_{rss}$	Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		65			
			Ch-2		65			
Total Gate Charge	$Q_g$		$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 8\text{ A}$	Ch-1		16.5	25	nC
				Ch-2		16.5	25	
		$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$	Ch-1		7.3	11		
			Ch-2		7.3	11		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$	Ch-1		2.7			
	Ch-2			2.7				
Gate-Drain Charge	$Q_{gd}$	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$	Ch-1		2.1			
			Ch-2		2.1			
Gate Resistance	$R_g$		$f = 1\text{ MHz}$	Ch-1	0.2	1.2	2.4	$\Omega$
				Ch-2	0.2	1.2	2.4	

Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .



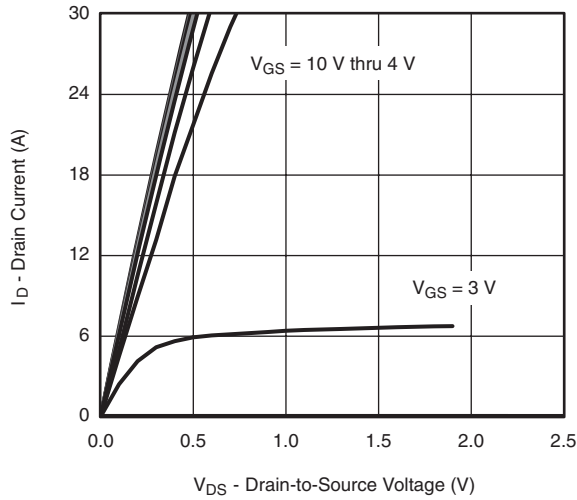
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ. <sup>a</sup>	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}, R_L = 3\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch-1		10	20	ns
Rise Time	$t_r$		Ch-2		9	18	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}, R_L = 3\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\ \Omega$	Ch-1		18	35	
Fall Time	$t_f$		Ch-2		18	35	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}, R_L = 3\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch-1		17	35	
Rise Time	$t_r$		Ch-2		17	35	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}, R_L = 3\ \Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\ \Omega$	Ch-1		12	24	
Fall Time	$t_f$		Ch-2		12	24	
			Ch-1		19	35	
			Ch-2		18	35	
			Ch-1		10	20	
			Ch-2		10	20	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			2.6	A
			Ch-2			2.6	
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$		Ch-1			30	A
			Ch-2			30	
Body Diode Voltage	$V_{SD}$	$I_S = 1\text{ A}$	Ch-1		0.46	0.51	V
		$I_S = 1\text{ A}$	Ch-2		0.74	1.1	
Body Diode Reverse Recovery Time	$t_{rr}$	Channel-1 $I_F = 5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		17	34	ns
			Ch-2		17	34	
Body Diode Reverse Recovery Charge	$Q_{rr}$	Channel-2 $I_F = 5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1		7	14	nC
			Ch-2		9	18	
Reverse Recovery Fall Time	$t_a$		Ch-1		9		ns
			Ch-2		10		
Reverse Recovery Rise Time	$t_b$		Ch-1		8		ns
			Ch-2		7		

Notes:

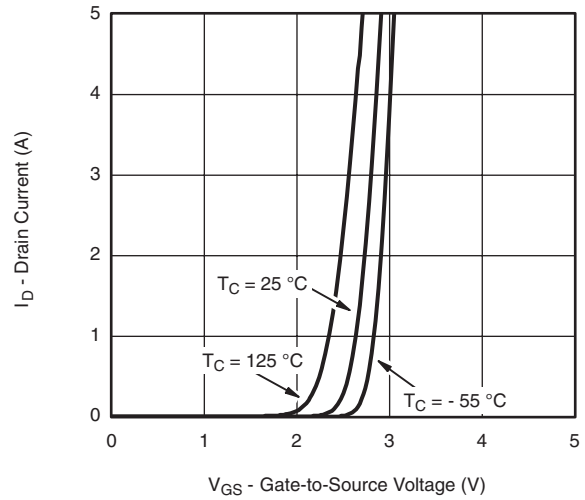
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

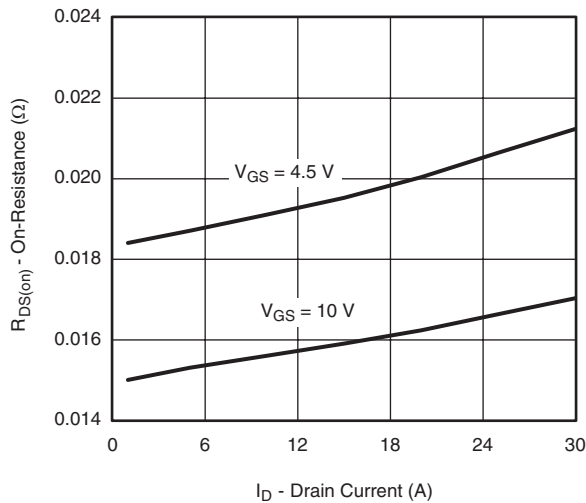
## CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



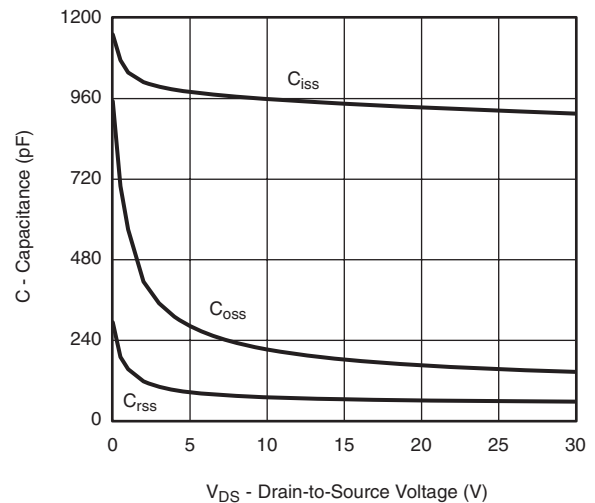
**Output Characteristics**



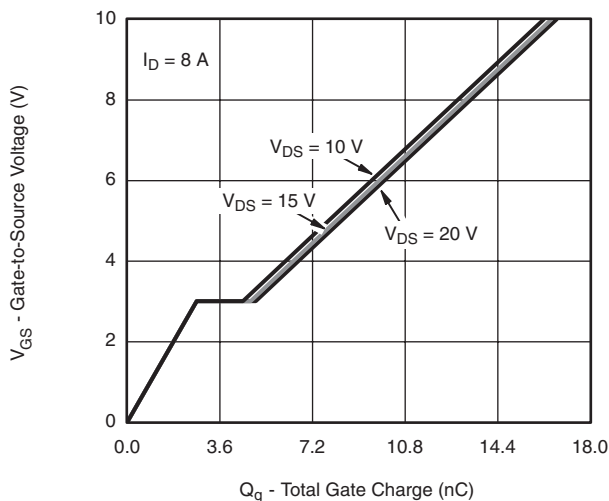
**Transfer Characteristics**



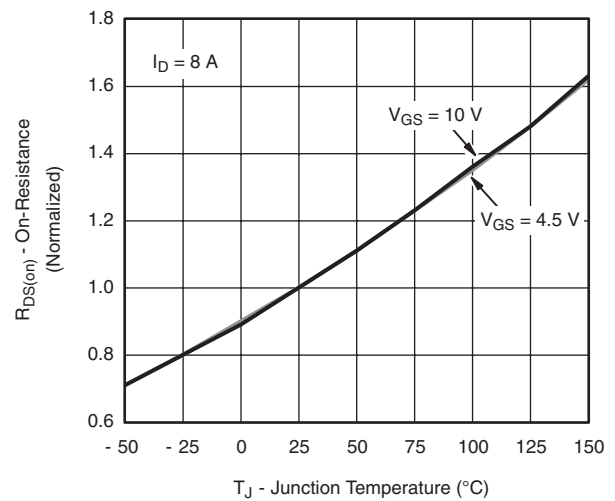
**On-Resistance vs. Drain Current**



**Capacitance**

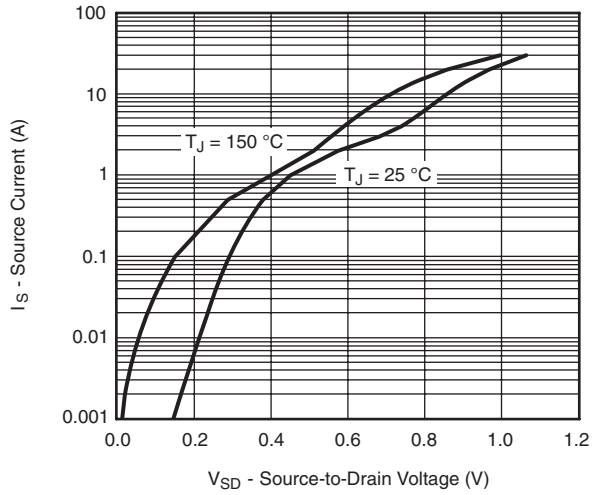


**Gate Charge**

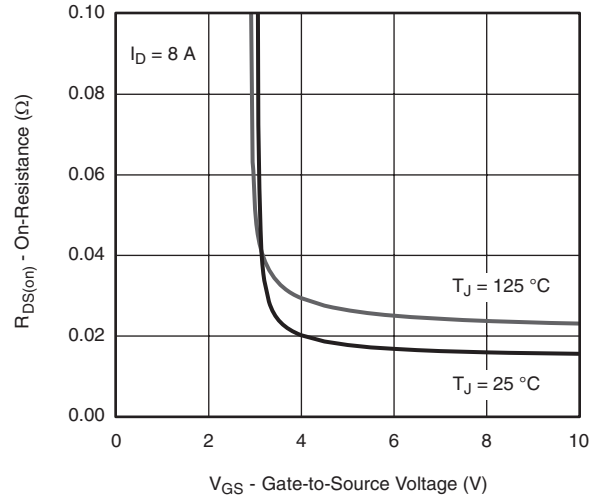


**On-Resistance vs. Junction Temperature**

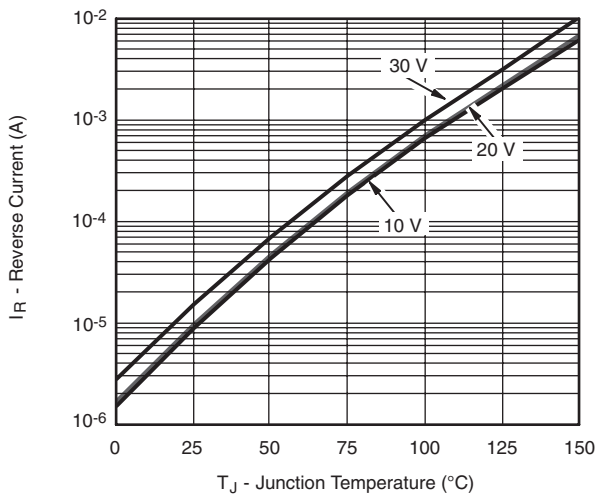
## CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



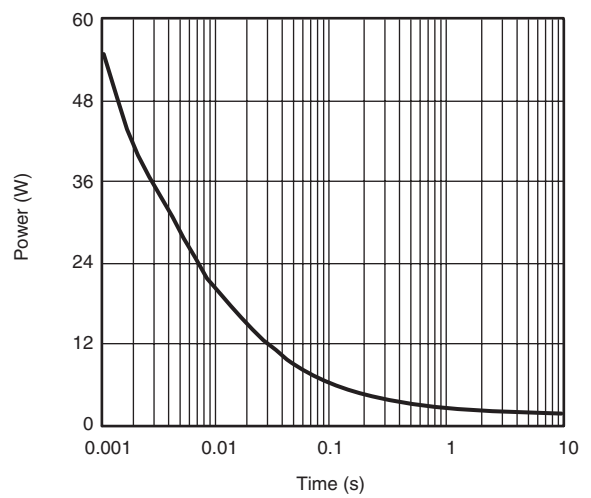
Source-Drain Diode Forward Voltage



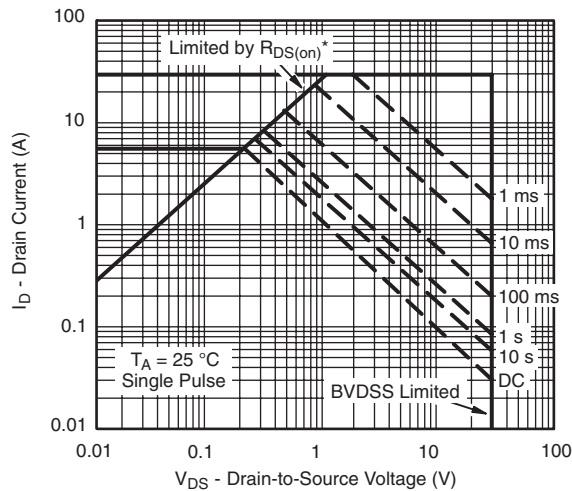
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)



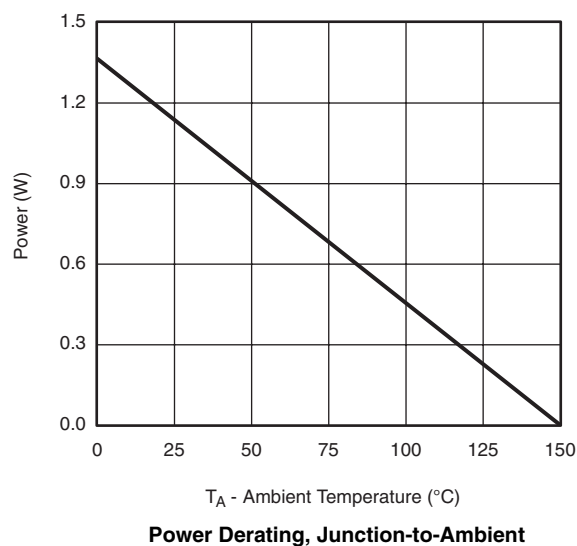
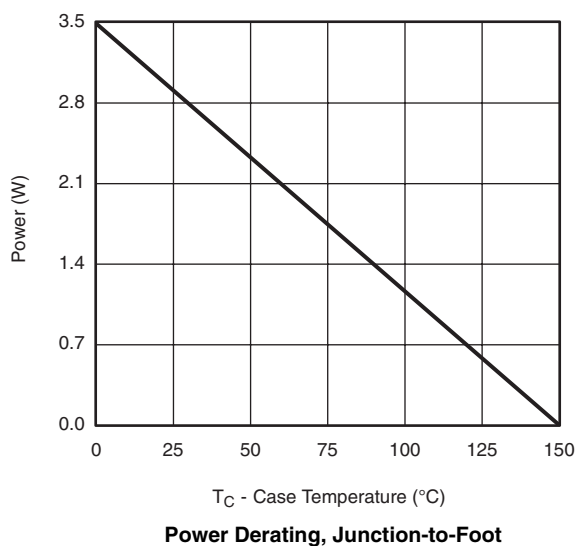
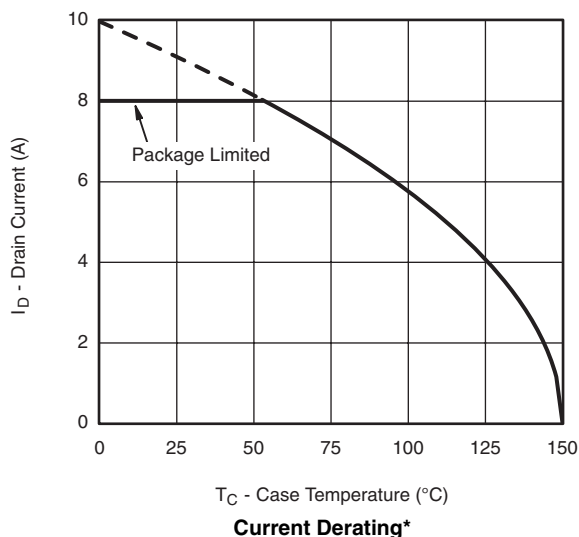
Single Pulse Power, Junction-to-Ambient



\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

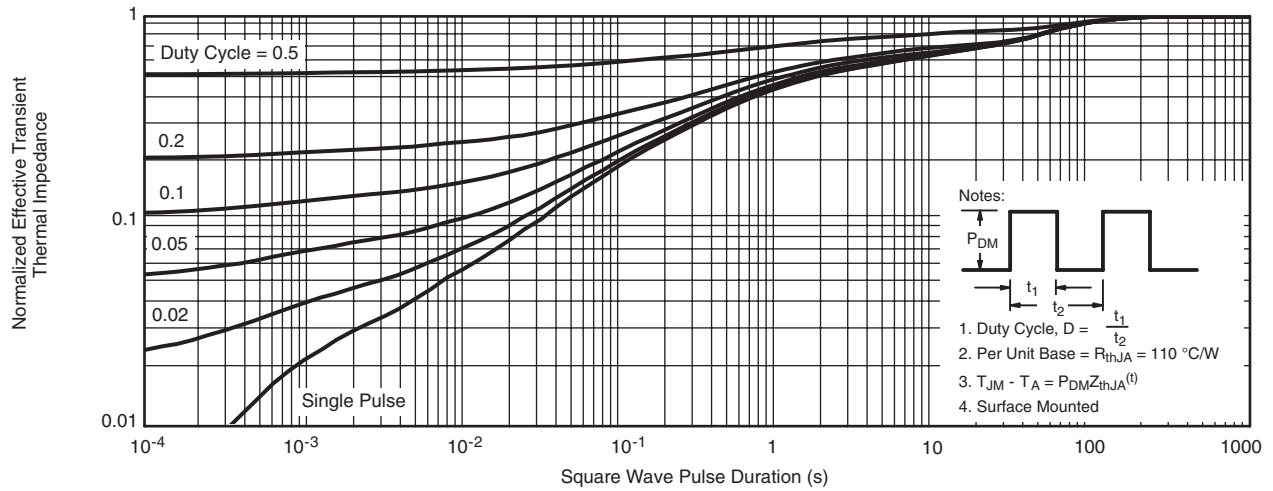
Safe Operating Area, Junction-to-Ambient

**CHANNEL-1 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

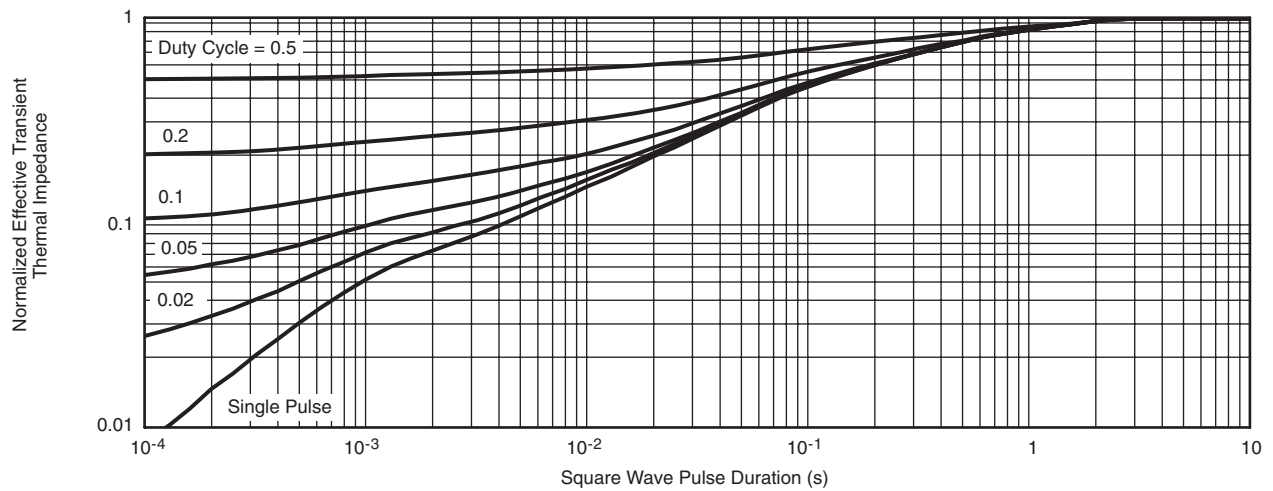


\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-1 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

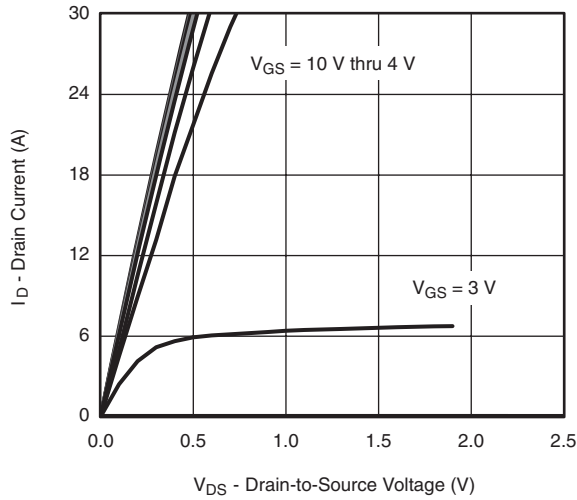


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

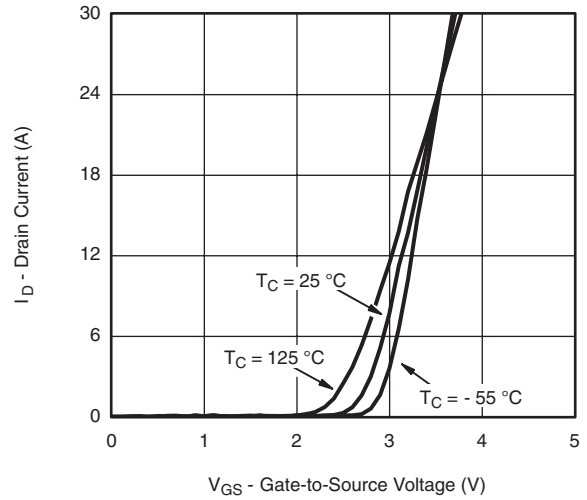


**Normalized Thermal Transient Impedance, Junction-to-Foot**

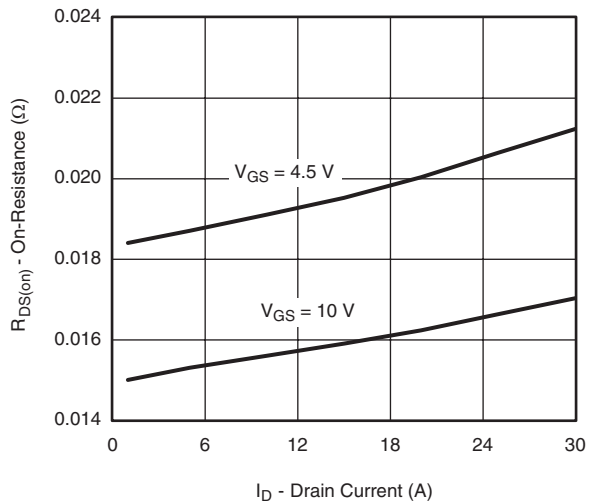
## CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



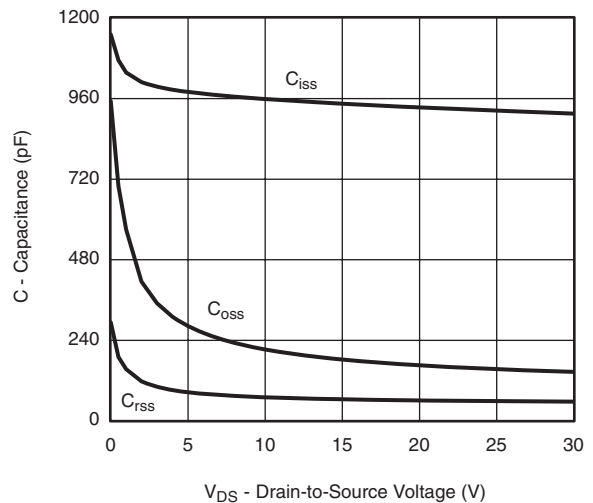
**Output Characteristics**



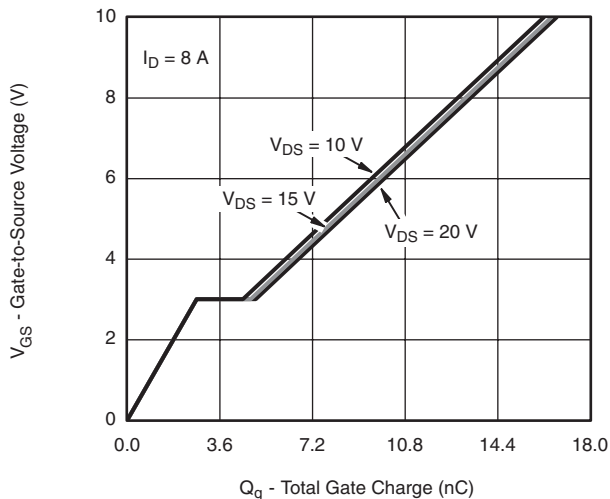
**Transfer Characteristics**



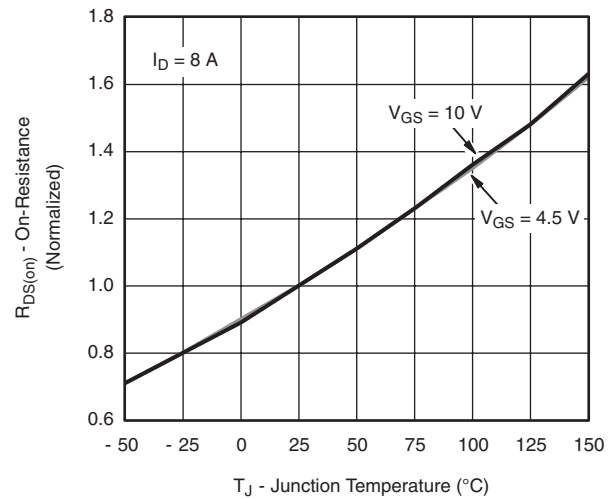
**On-Resistance vs. Drain Current**



**Capacitance**



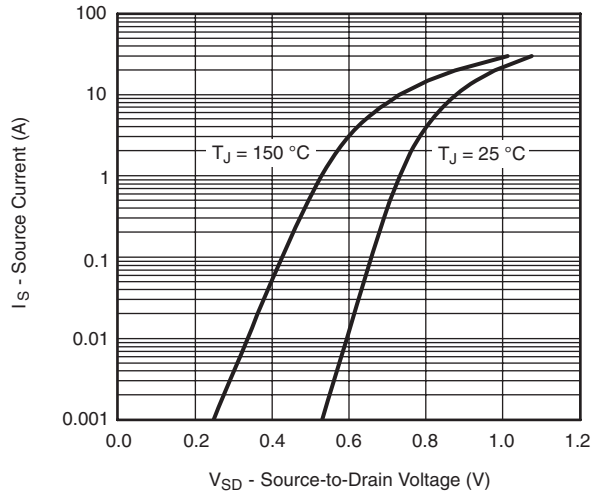
**Gate Charge**



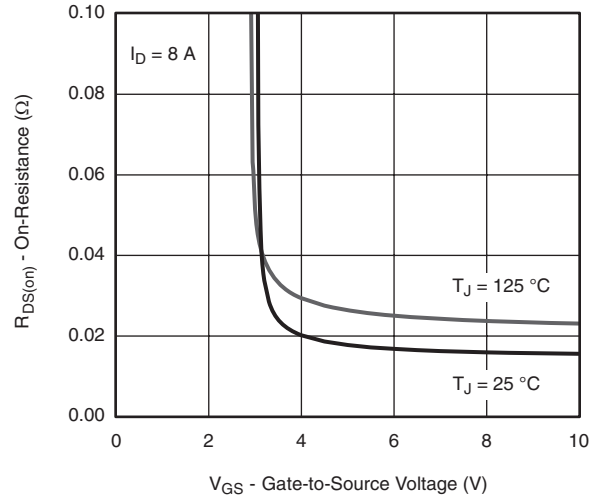
**On-Resistance vs. Junction Temperature**



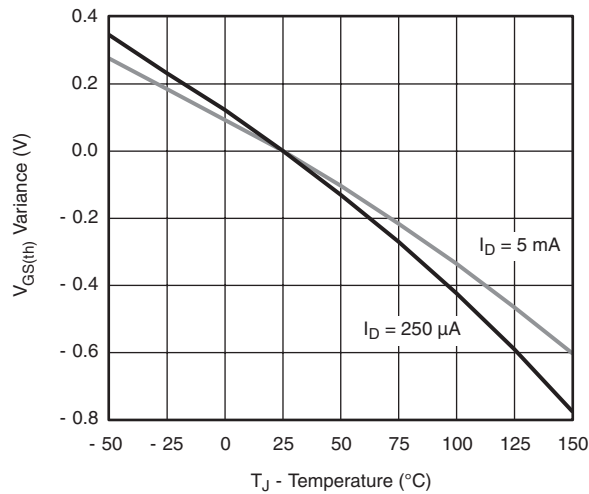
## CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



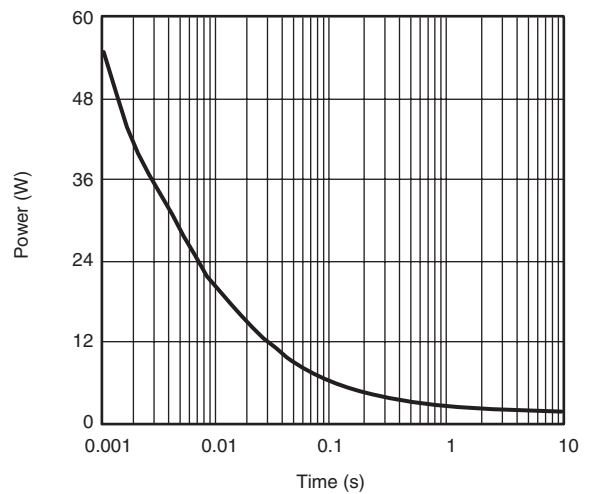
Source-Drain Diode Forward Voltage



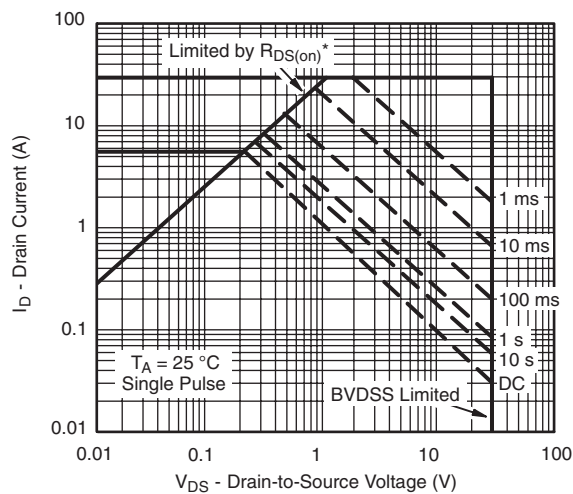
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



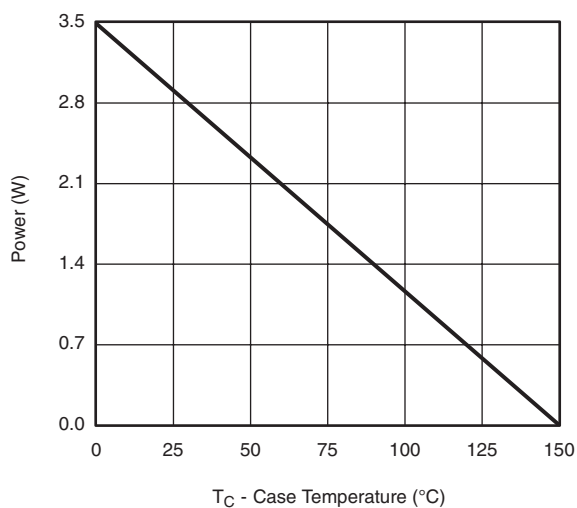
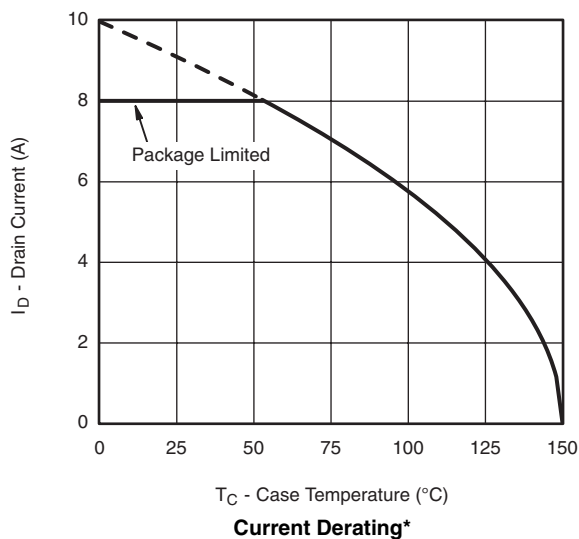
Single Pulse Power, Junction-to-Ambient



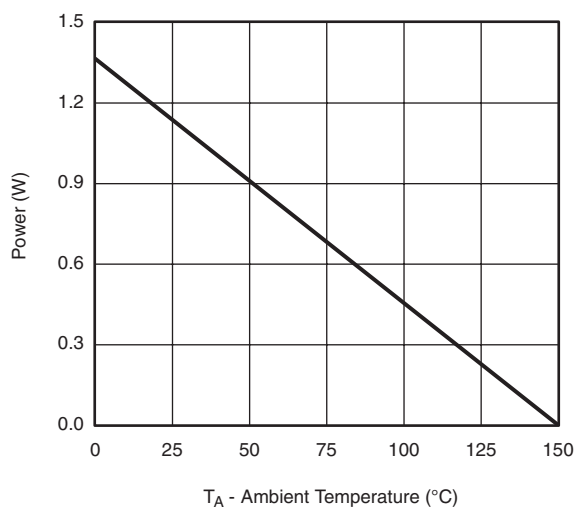
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

**CHANNEL-2 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



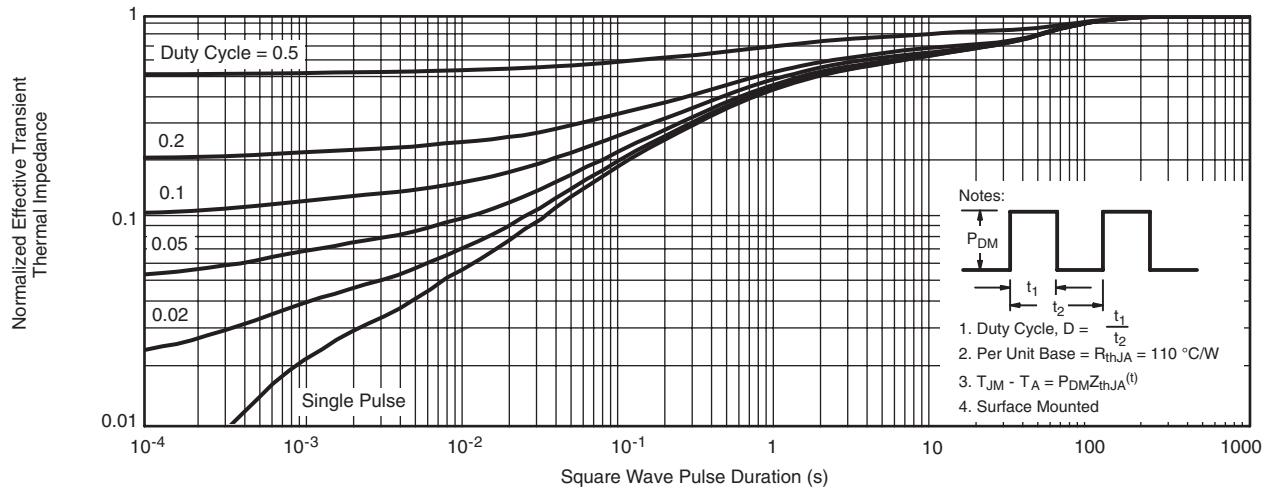
**Power Derating, Junction-to-Foot**



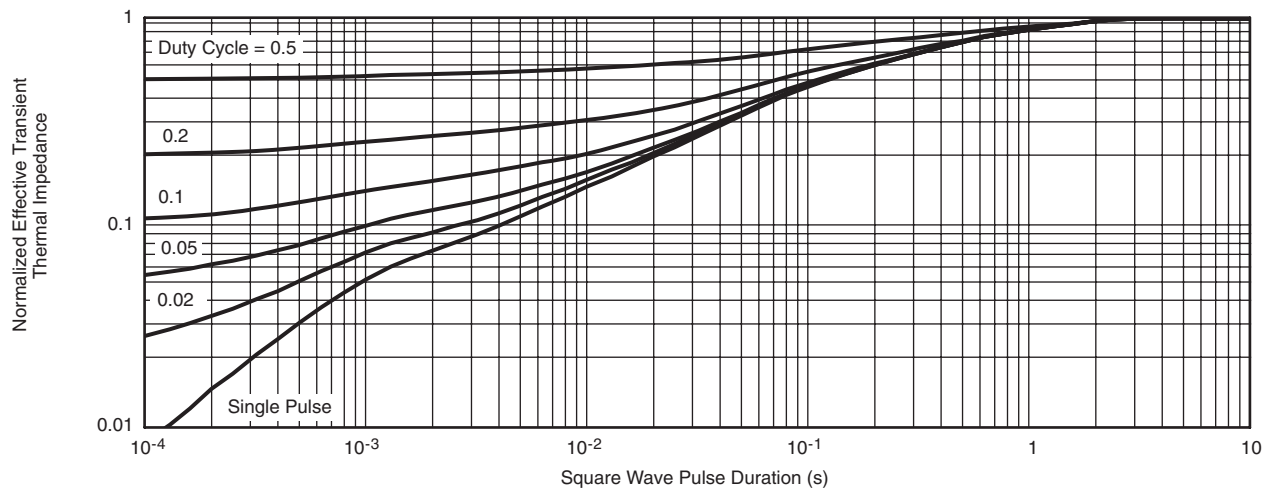
**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-2 TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Foot**

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## SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026

ECN: C-06527-Rev. I, 11-Sep-06  
DWG: 5498

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



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