Si4840BDY

RoHS

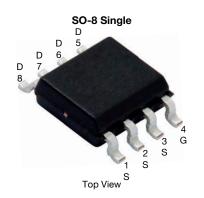
COMPLIANT

HALOGEN

FREE

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PRODUCT SUMMARY					
V _{DS} (V)	40				
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.009				
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.012				
Q _g typ. (nC)	15				
I _D (A)	19 ^d				
Configuration	Single				

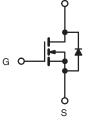
FEATURES

N-Channel 40 V (D-S) MOSFET

- TrenchFET[®] power MOSFET
- 100 % $\rm R_g$ and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Synchronous rectification
- POL, IBC
 - Secondary side



N-Channel MOSFET

ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free	Si4840BDY-T1-E3			
Lead (Pb)-free and halogen-free	Si4840BDY-T1-GE3			

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	40	V	
Gate-source voltage		V _{GS}	± 20		
	T _C = 25 °C		19		
Continuous drain surrent (T 150 °C)	T _C = 70 °C		15		
Continuous drain current (T _J = 150 °C)	T _A = 25 °C	I _D	12.4 ^{a, b}	•	
	T _A = 70 °C	1 1	9.9 ^{a, b}	— A	
Pulsed drain current		I _{DM}	50	1	
Avalanche current		I _{AS}	15		
Avalanche energy	L = 0.1 mH		11	mJ	
Continuous source-drain diode current	T _C = 25 °C		5	٨	
	T _A = 25 °C	I _S	2.1 ^{a, b}	— A	
Maximum power dissipation	T _C = 25 °C		6		
	T _C = 70 °C		3.8	14/	
	T _A = 25 °C	P _D	2.5 ^{a, b}	— W	
	T _A = 70 °C	1	1.6 ^{a, b}		
Operating junction and storage temperature range		T _J , T _{stq}	-55 to +150	°C	

THERMAL RESISTANCE RATINGS							
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT		
Maximum junction-to-ambient a, c	t ≤ 10 s	R _{thJA}	37	50	°C/W		
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	17	21	C/W		

Notes

a. Surface mounted on 1" x 1" FR4 board

b. t = 10 s

c. Maximum under steady state conditions is 85 °C/W

d. Based on $T_C = 25 \ ^{\circ}C$

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static				•			
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 V, I_{D} = 250 \mu A$	40	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_J$	L 050 A	-	40	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	l _D = 250 μA	-	-6	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1	-	3	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 100	nA	
7		$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μΑ	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C	-	-	5		
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 V, V_{GS} = 10 V$	50	-	-	Α	
		V _{GS} = 10 V, I _D = 12.4 A	-	0.0074	0.0090	- Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 10.8 A	-	0.0095	0.0120		
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 12.4 A	-	56	-	S	
Dynamic ^b		-			1		
Input capacitance	C _{iss}		-	2000	-	pF	
Output capacitance	C _{oss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz	-	260	-		
Reverse transfer capacitance	C _{rss}		-	150	-		
Total gate charge	Qg	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 12.4 A	-	33	50	s nC	
			-	15	23		
Gate-source charge	Q _{as}	V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 12.4 A	-	6.7	-		
Gate-drain charge	Q _{gd}		-	5.1	-		
Gate resistance	Rg	f = 1 MHz	-	1.4	2.1	Ω	
Turn-on delay time	t _{d(on)}		-	25	40		
Rise time	tr	$V_{DD} = 20 \text{ V}, \text{ R}_{\text{L}} = 2 \Omega$	-	12	20	1	
Turn-off delay time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{\text{GEN}} = 4.5 \text{ V}, R_g = 1 \Omega$	-	25	40		
Fall time	tf		-	10	15		
Turn-on delay time	t _{d(on)}		-	10	15	ns	
Rise time	t _r	$V_{DD} = 20 \text{ V}, \text{ R}_{\text{I}} = 2 \Omega$	-	15	25	-	
Turn-off delay time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	30	45		
Fall time	t _f		-	10	15		
Drain-Source Body Diode Characterist	cs				1		
Continuous source-drain diode current	IS	T _C = 25 °C	-	-	30		
Pulse diode forward current	I _{SM}		-	-	50	A	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	-	0.8	1.2	V	
Body diode reverse recovery time	t _{rr}		-	30	60	ns	
Body diode reverse recovery charge	Q _{rr}		-	26	52	nC	
Reverse recovery fall time	ta	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	17.5	-		
Reverse recovery rise time	t _b	1	-	12.5	_	ns	

Notes

a. Pulse test: pulse width $\leq 300~\mu\text{s},~\text{duty}~\text{cycle} \leq 2~\%$

b. Guaranteed by design, not subject to production testing

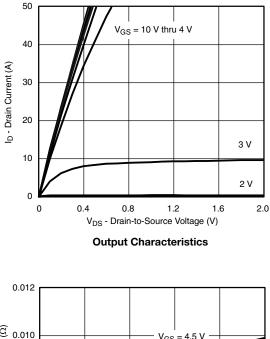
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

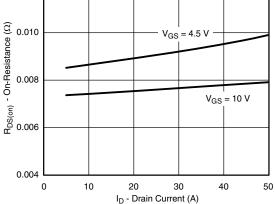
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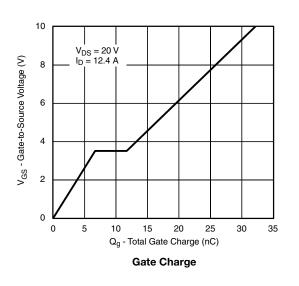
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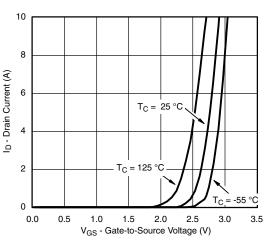
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



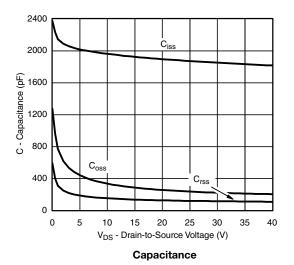


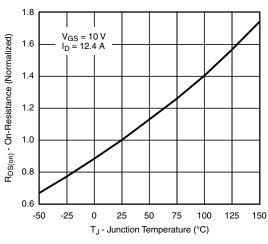
On-Resistance vs. Drain Current and Gate Voltage





Transfer Characteristics





On-Resistance vs. Junction Temperature

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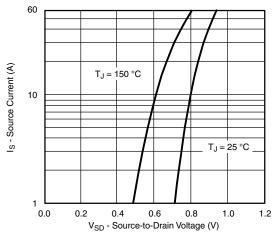
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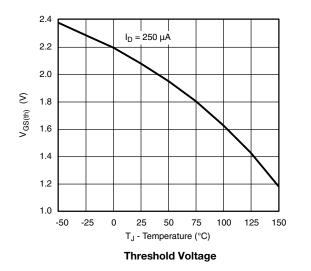
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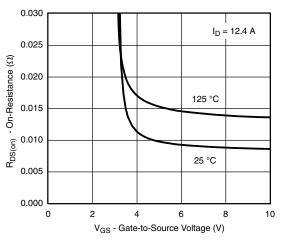
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

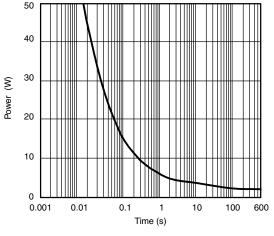


Source-Drain Diode Forward Voltage

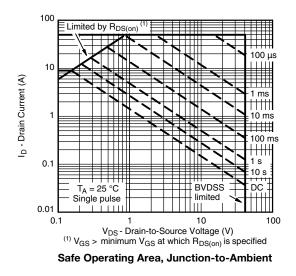




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)

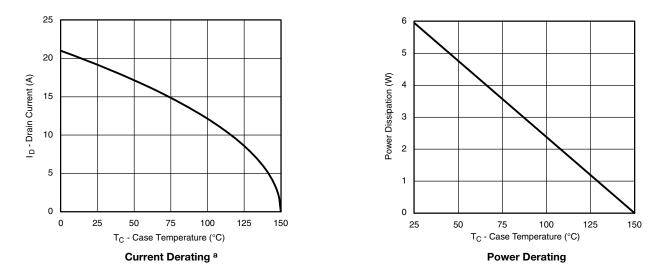


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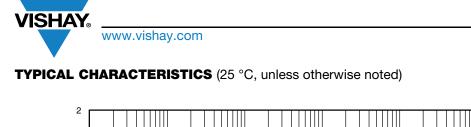
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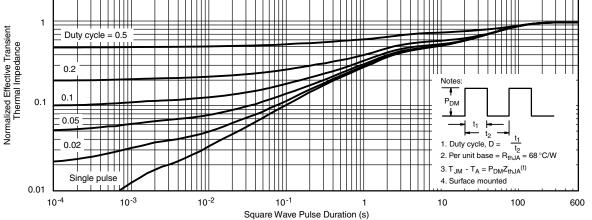
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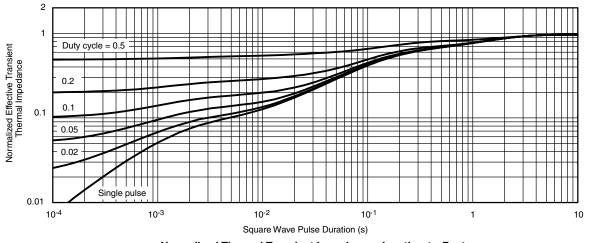
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?69795.

Si4840BDY

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Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

Application Note 826

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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