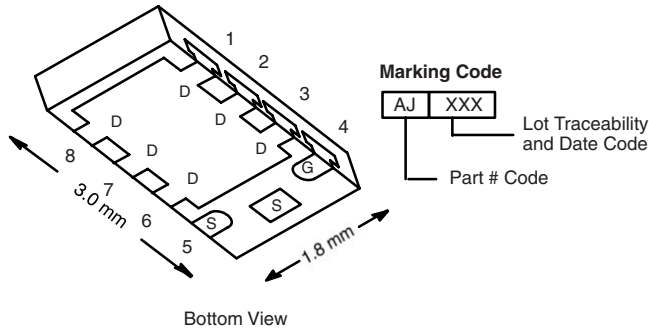


## N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
40	0.018 at V <sub>GS</sub> = 10 V	12	10 nC
	0.021 at V <sub>GS</sub> = 4.5 V	12	

PowerPAK ChipFET Single



### FEATURES

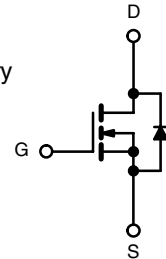
- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET
- New Thermally Enhanced PowerPAK<sup>®</sup> ChipFET<sup>®</sup> Package
  - Small Footprint Area
  - Low On-Resistance
  - Thin 0.8 mm Profile
- 100 % UIS Tested



**RoHS**  
COMPLIANT

### APPLICATIONS

- Load Switch, PA Switch, and Battery Switch for Portable Applications
- DC-DC Synchronous Rectification



Ordering Information: Si5410DU-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	40	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	12 <sup>a</sup>
		T <sub>C</sub> = 70 °C	12 <sup>a</sup>
		T <sub>A</sub> = 25 °C	9.8 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	7.9 <sup>b, c</sup>
Pulsed Drain Current	I <sub>DM</sub>	30	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	2.6 <sup>b, c</sup>
Single Pulse Avalanche Current	I <sub>AS</sub>	19	mJ
Single Pulse Avalanche Energy	E <sub>AS</sub>	18	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	31
		T <sub>C</sub> = 70 °C	20
		T <sub>A</sub> = 25 °C	3.1 <sup>b, c</sup>
		T <sub>A</sub> = 70 °C	2 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	34	40	°C/W	
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	3	4		

Notes:

- Package limited.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 s.
- See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under Steady State conditions is 90 °C/W.



SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		45		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.2		3	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.6\text{ A}$		0.015	0.018	$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 6.1\text{ A}$		0.017	0.021	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 6.6\text{ A}$		30		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		1350		pF
Output Capacitance	$C_{oss}$			150		
Reverse Transfer Capacitance	$C_{rss}$			70		
Total Gate Charge	$Q_g$	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 9.8\text{ A}$		21	32	nC
		$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 9.8\text{ A}$		10	15	
Gate-Source Charge	$Q_{gs}$			4.5		
Gate-Drain Charge	$Q_{gd}$		3.1			
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		3.5		$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2.5\text{ }\Omega$ $I_D \cong 7.9\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		25	40	ns
Rise Time	$t_r$			15	25	
Turn-Off Delay Time	$t_{d(off)}$			25	40	
Fall Time	$t_f$			12	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2.5\text{ }\Omega$ $I_D \cong 7.9\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		10	15	
Rise Time	$t_r$			15	25	
Turn-Off Delay Time	$t_{d(off)}$			22	35	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			12	A
Pulse Diode Forward Current	$I_{SM}$				30	
Body Diode Voltage	$V_{SD}$	$I_S = 7.9\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 7.9\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		25	40	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			22	35	nC
Reverse Recovery Fall Time	$t_a$			15		ns
Reverse Recovery Rise Time	$t_b$			10		

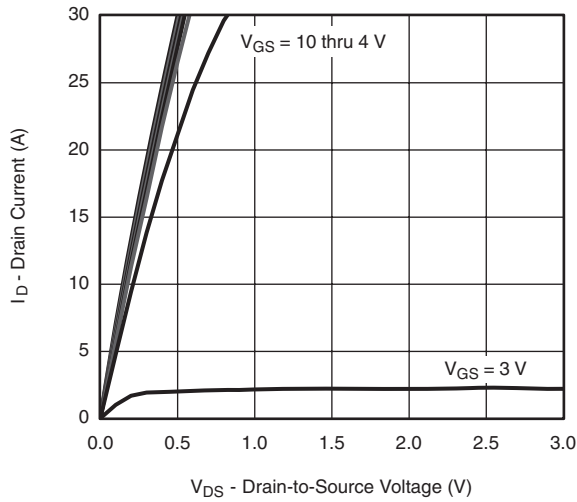
## Notes:

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

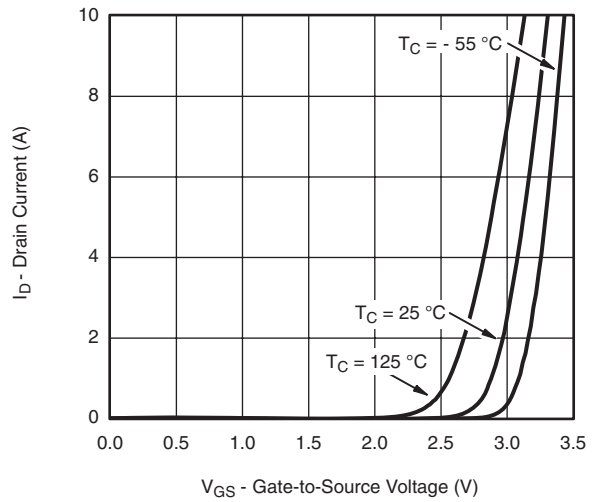
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



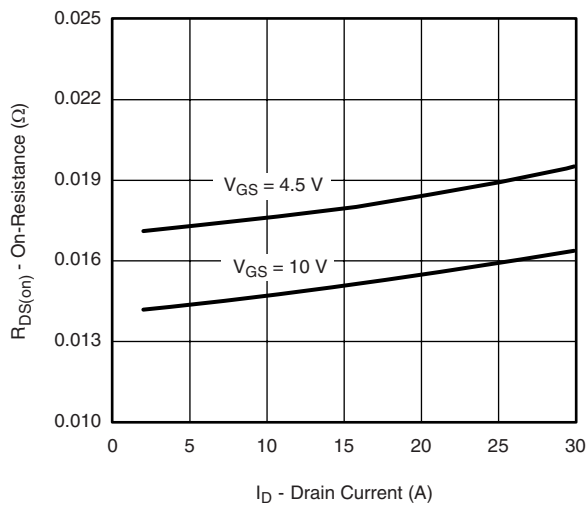
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



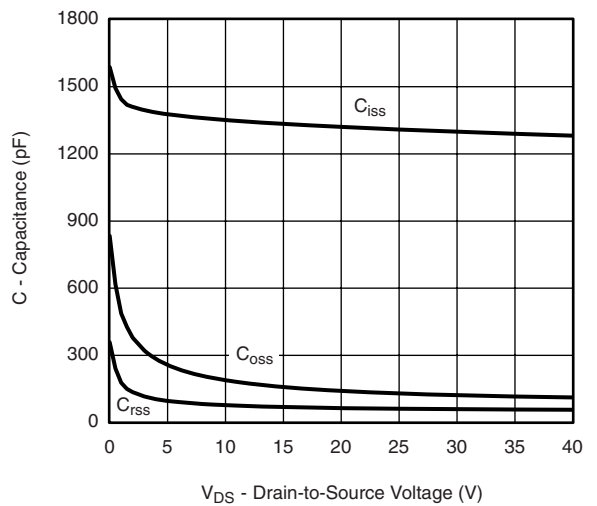
**Output Characteristics**



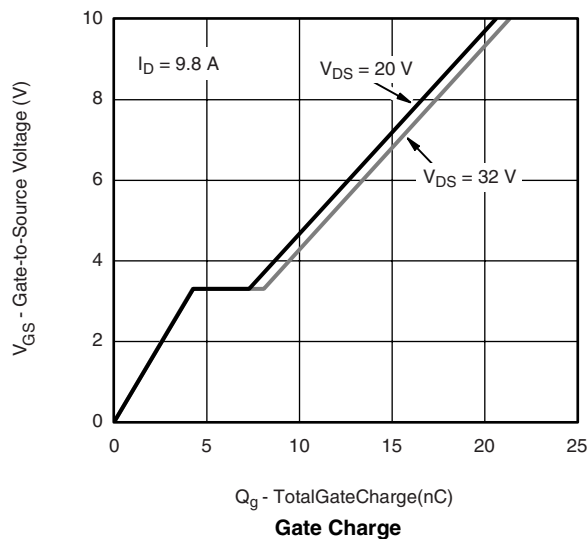
**Transfer Characteristics**



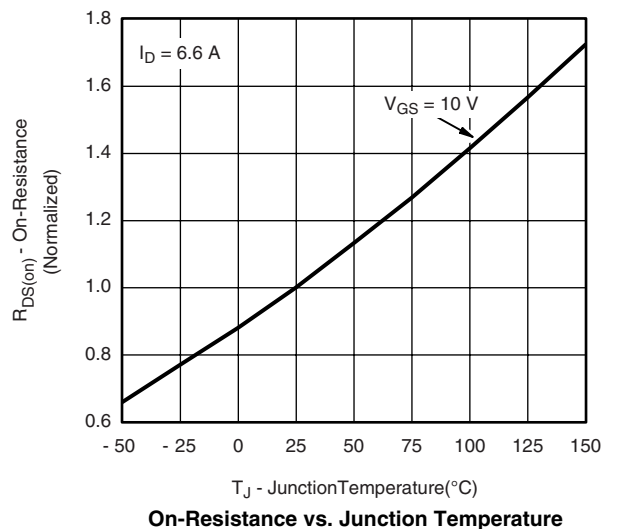
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



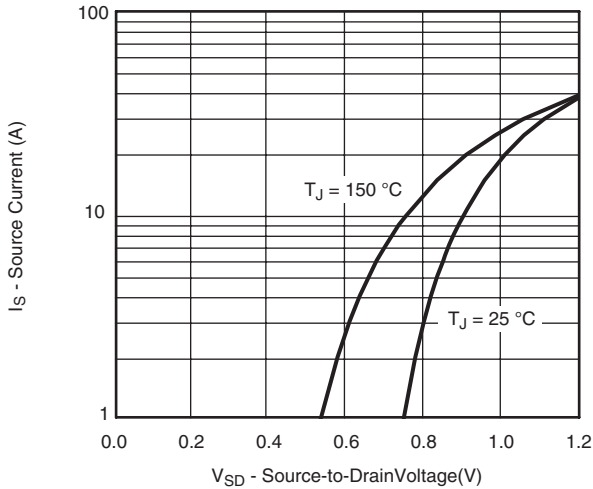
**Gate Charge**



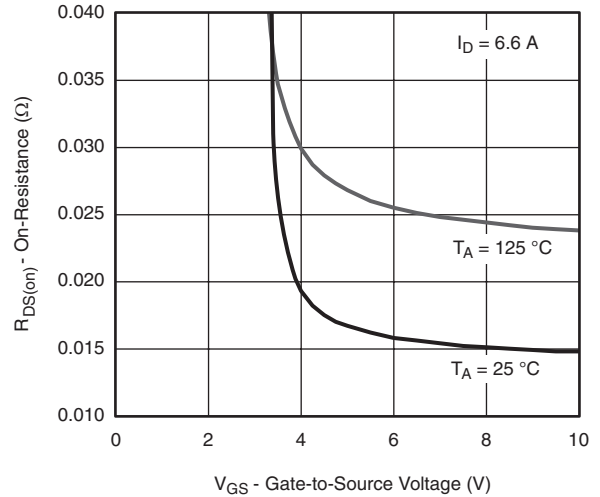
**On-Resistance vs. Junction Temperature**



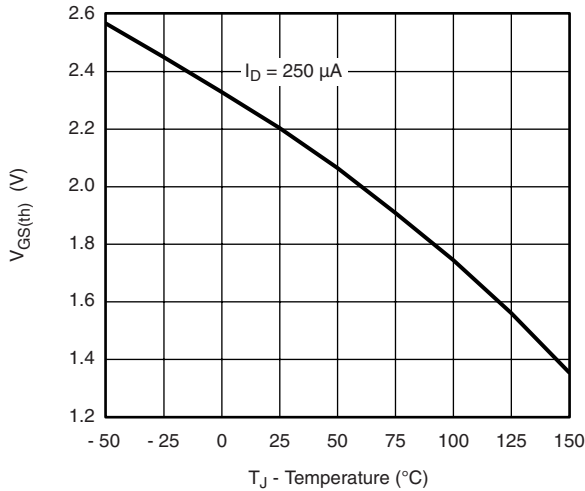
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



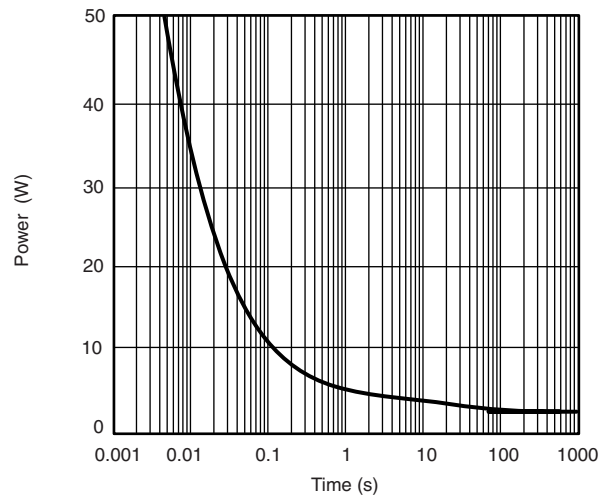
Source-Drain Diode Forward Voltage



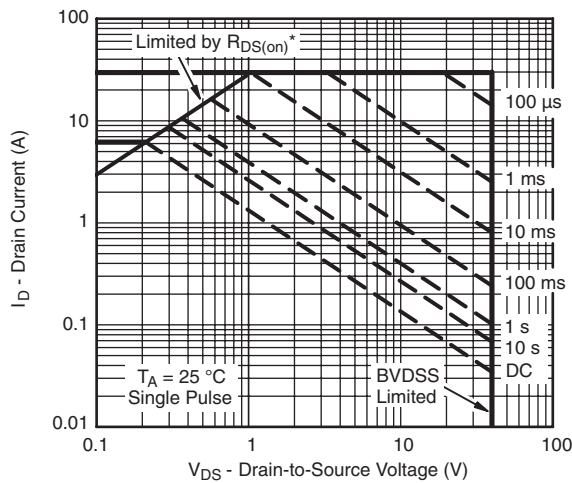
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient

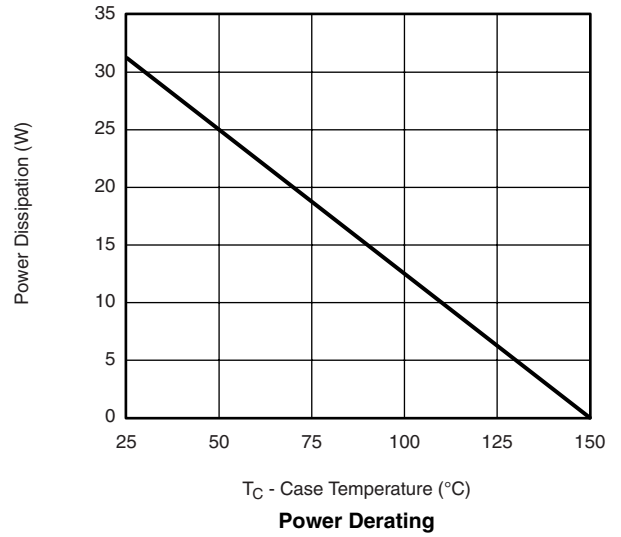
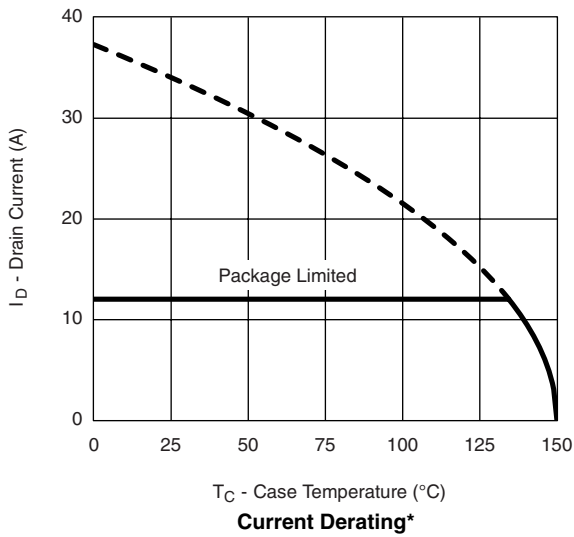


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient



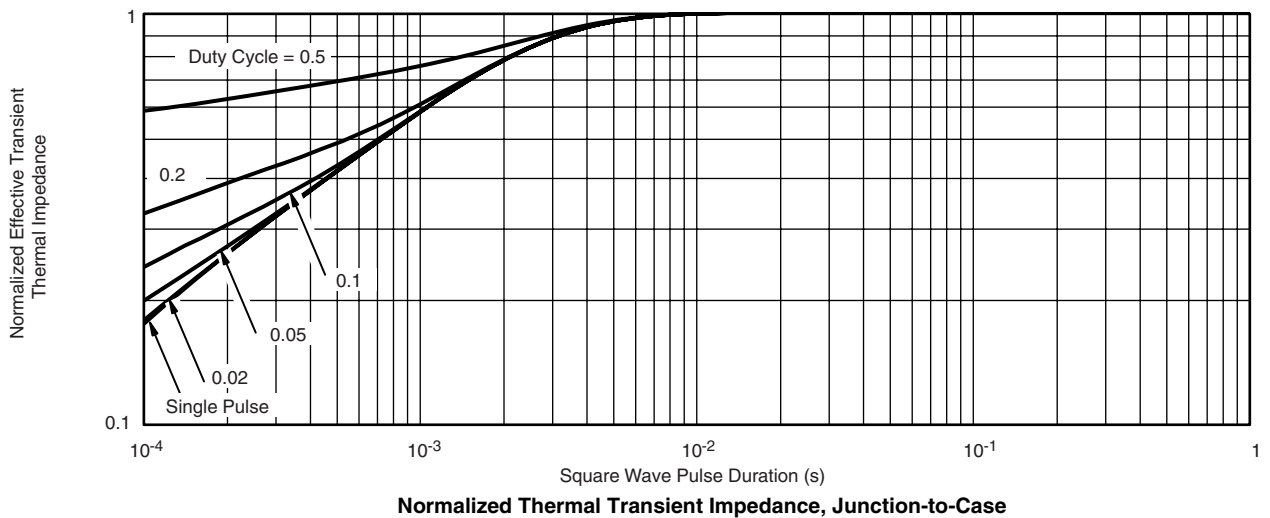
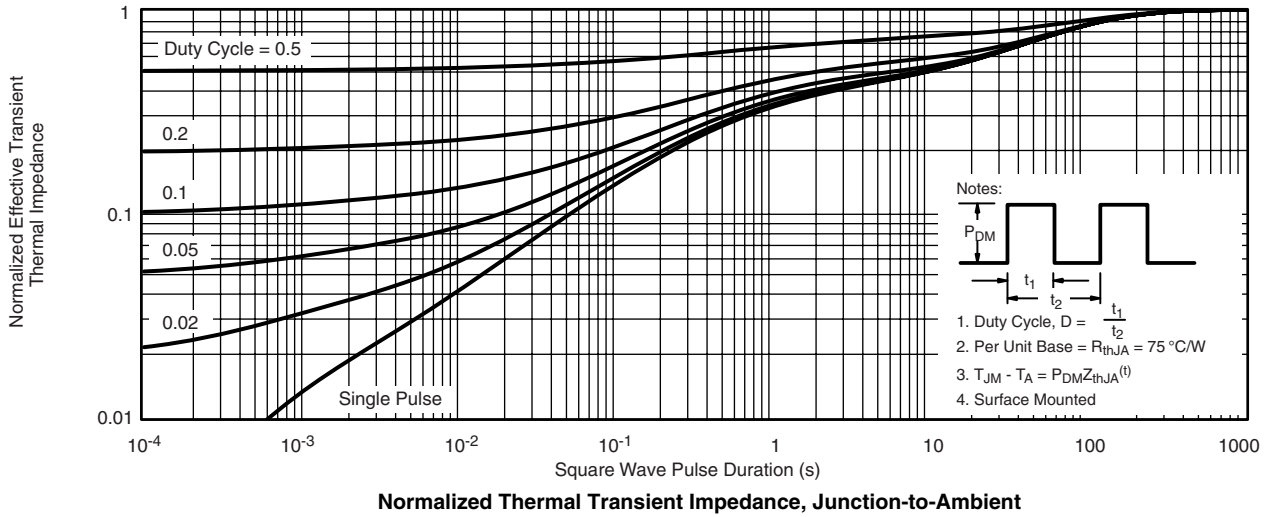
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69827>.

### PowerPAK<sup>®</sup> ChipFET<sup>®</sup> Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.85	0.028	0.030	0.033
A1	0	-	0.05	0	-	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
C	0.15	0.20	0.25	0.006	0.008	0.010
D	2.92	3.00	3.08	0.115	0.118	0.121
D1	1.75	1.87	2.00	0.069	0.074	0.079
D2	1.07	1.20	1.32	0.042	0.047	0.052
D3	0.20	0.25	0.30	0.008	0.010	0.012
E	1.82	1.90	1.98	0.072	0.075	0.078
E1	1.38	1.50	1.63	0.054	0.059	0.064
E2	0.92	1.05	1.17	0.036	0.041	0.046
E3	0.45	0.50	0.55	0.018	0.020	0.022
e	0.65 BSC			0.026 BSC		
H	0.15	0.20	0.25	0.006	0.008	0.010
K	0.25	-	-	0.010	-	-
K1	0.30	-	-	0.012	-	-
K2	0.20	-	-	0.008	-	-
K3	0.20	-	-	0.008	-	-
L	0.30	0.35	0.40	0.012	0.014	0.016
C14-0630-Rev. E, 21-Jul-14						
DWG: 5940						

**Note**

- Millimeters will govern

## RECOMMENDED MINIMUM PADS FOR PowerPAK® ChipFET® Single



Recommended Minimum Pads  
Dimensions in mm/(Inches)

[Return to Index](#)





## **Disclaimer**

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [MOSFET](#) category:*

*Click to view products by [Vishay](#) manufacturer:*

Other Similar products are found below :

[614233C](#) [648584F](#) [IRFD120](#) [JANTX2N5237](#) [2N7000](#) [FCA20N60\\_F109](#) [FDZ595PZ](#) [2SK2545\(Q,T\)](#) [405094E](#) [423220D](#)  
[TPCC8103,L1Q\(CM](#) [MIC4420CM-TR](#) [VN1206L](#) [614234A](#) [715780A](#) [NTNS3166NZT5G](#) [SSM6J414TU,LF\(T](#) [751625C](#)  
[IPS70R2K0CEAKMA1](#) [BUK954R8-60E](#) [DMN3404LQ-7](#) [NTE6400](#) [SQJ402EP-T1-GE3](#) [2SK2614\(TE16L1,Q\)](#) [2N7002KW-FAI](#)  
[DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [ECH8691-TL-W](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#) [NTE221](#) [NTE2384](#)  
[NTE2903](#) [NTE2941](#) [NTE2945](#) [NTE2946](#) [NTE2960](#) [NTE2967](#) [NTE2969](#) [NTE2976](#) [NTE455](#) [NTE6400A](#) [NTE2910](#) [NTE2916](#) [NTE2956](#)  
[NTE2911](#) [US6M2GTR](#) [TK10A80W,S4X\(S](#) [SSM6P69NU,LF](#)