



# P-Channel 20-V (D-S) MOSFET

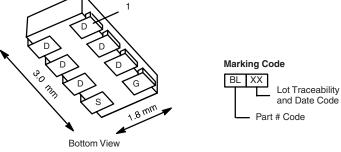
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
	0.037 at V <sub>GS</sub> = - 4.5 V	- 6.7			
- 20	0.050 at V <sub>GS</sub> = - 2.5 V	- 5.9	15		
	0.070 at V <sub>GS</sub> = - 1.8 V	- 5.0			

### **FEATURES**

- Halogen-free According to IEC 61249-2-21 **Available**
- TrenchFET<sup>®</sup> Power MOSFET







Ordering Information: Si5433BDC-T1-E3 (Lead (Pb)-free)

Si5433BDC-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	A = 25 °C, unle	ss otherwise r	noted		
Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 20		V
Gate-Source Voltage		V <sub>GS</sub>	± 8		
Continuous Drain Current (T <sub>1</sub> = 150 °C) <sup>a</sup>	T <sub>A</sub> = 25 °C	- I <sub>D</sub>	- 6.7	- 4.8	
Continuous Drain Current (1, = 150°C)	T <sub>A</sub> = 85 °C		- 4.8	- 3.5	^
Pulsed Drain Current		I <sub>DM</sub>	- 20		Α
Continuous Source Current <sup>a</sup>		I <sub>S</sub>	- 2.1	- 1.1	
M	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2.5	1.3	W
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 85 °C		1.3	0.7	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) <sup>b, c</sup>			260		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	t ≤ 5 s	R <sub>thJA</sub>	45	50	°C/W	
	Steady State		85	95		
Maximum Junction-to-Foot (Drain)	Steady State	R <sub>thJF</sub>	17	20	]	

### Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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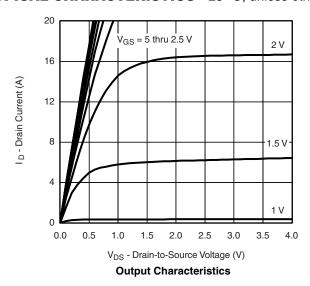
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	•		•	•			
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.45		- 1.0	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V			- 1		
		V <sub>DS</sub> = - 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 85 °C			- 5 μA		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	- 20			Α	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = - 4.5 V, I <sub>D</sub> = - 4.8 A		0.030	0.037	Ω	
		$V_{GS} = -2.5 \text{ V}, I_D = -4.2 \text{ A}$		0.041	0.050		
		V <sub>GS</sub> = - 1.8 V, I <sub>D</sub> = - 1 A		0.056	0.070		
Forward Transconductance <sup>a</sup> 9 <sub>fs</sub>		V <sub>DS</sub> = - 10 V, I <sub>D</sub> = - 4.8 A		18		S	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	I <sub>S</sub> = - 1.1 A, V <sub>GS</sub> = 0 V		- 0.8	- 1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	$Q_g$			15	22		
Gate-Source Charge	Q <sub>gs</sub> Q <sub>gd</sub>	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -4.8 \text{ A}$		2.4		nC	
Gate-Drain Charge				3.6			
Gate Resistance	$R_g$			10		Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			12	25		
Rise Time	t <sub>r</sub>	$V_{DD}$ = - 10 V, $R_L$ = 10 $\Omega$		25	40		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong$ - 1 A, $V_{GEN}$ = - 4.5 V, $R_g$ = 6 $\Omega$		80	120	ns	
Fall Time	t <sub>f</sub>			55	85		
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = - 1.1 A, dl/dt = 100 A/μs		30	60		

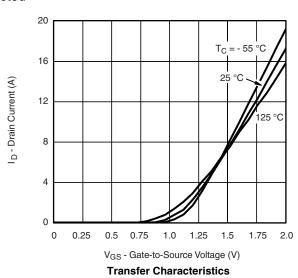
#### Notes:

- a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



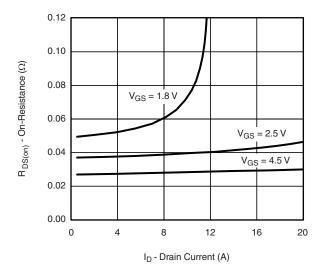




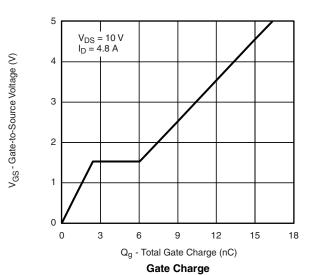


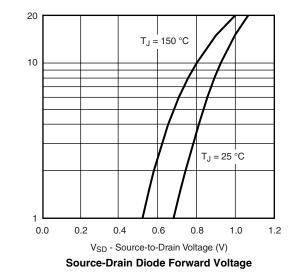


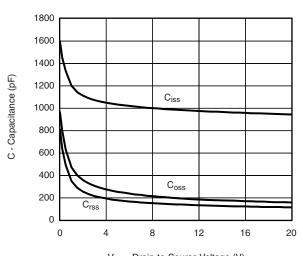
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



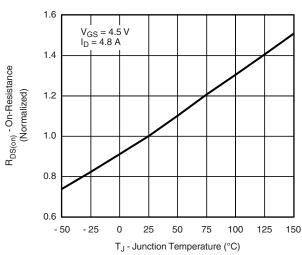
**On-Resistance vs. Drain Current** 



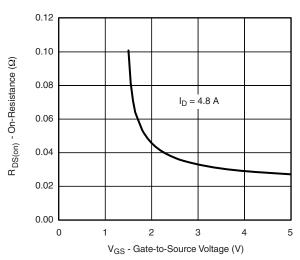




V<sub>DS</sub> - Drain-to-Source Voltage (V) **Capacitance** 



On-Resistance vs. Junction Temperature



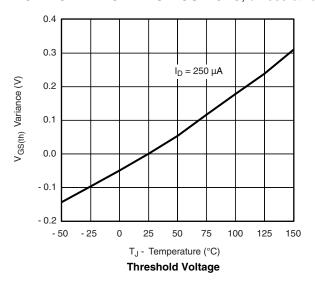
On-Resistance vs. Gate-to-Source Voltage

Source Current (A)

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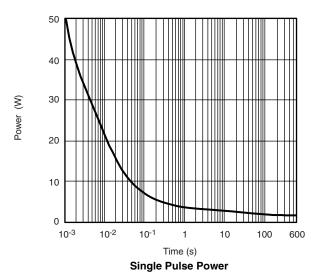
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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



100

0.01 **L** 



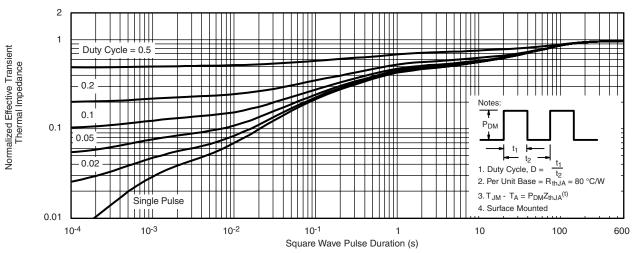
 $\label{eq:VDS} V_{DS}\mbox{-} \mbox{Drain-to-Source Voltage (V)} $$^*V_{GS} > \mbox{minimum } V_{GS} \mbox{ at which } R_{DS(on)} \mbox{ is specified}$ 

**BVDSS** Limited

10

100

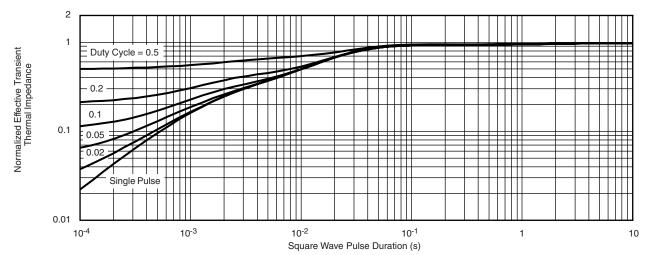
### Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="https://www.vishay.com/ppg273208">www.vishay.com/ppg273208</a>.

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