

N-Channel 20-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
20	0.0062 at V _{GS} = 4.5 V	19.5	17.5 nC
	0.0098 at V _{GS} = 2.5 V	15.5	

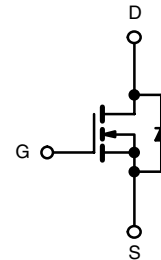
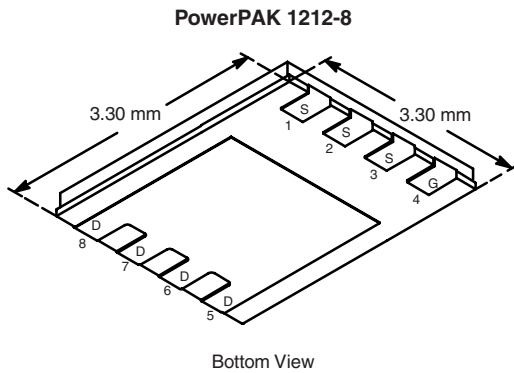
FEATURES

- Halogen-free Option Available
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- PWM Optimized
- 100 % R_g Tested



APPLICATIONS

- Synchronous Rectification



Ordering Information: Si7106DN-T1-E3 (Lead (Pb)-free)
Si7106DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted					
Parameter	Symbol	10 s	Steady State	Unit	
Drain-Source Voltage	V _{DS}	20		V	
Gate-Source Voltage	V _{GS}	± 12			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	19.5	12.5	A
		T _A = 70 °C	15.6	10.0	
Pulsed Drain Current	I _{DM}	60			
Continuous Source Current (Diode Conduction) ^a	I _S	3.2	1.3		
Single Avalanche Current	L = 0.1 mH	I _{AS}	30		mJ
Single Avalanche Energy		E _{AS}	45		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.8	1.5	W
		T _A = 70 °C	2.0	0.8	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	24	33	°C/W
	Steady State		65	81	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.9	2.4	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.



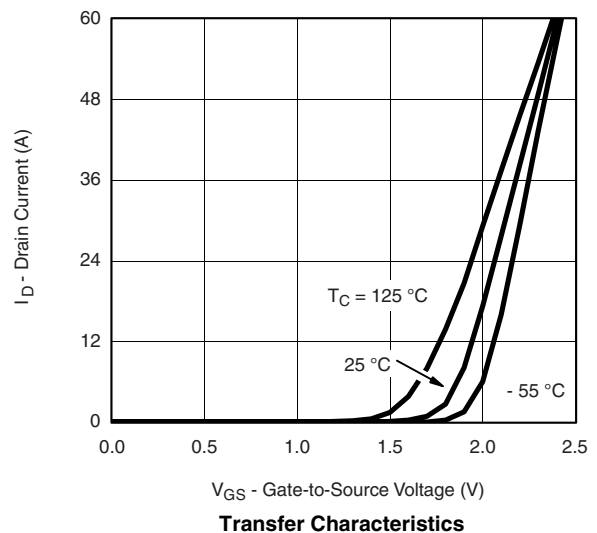
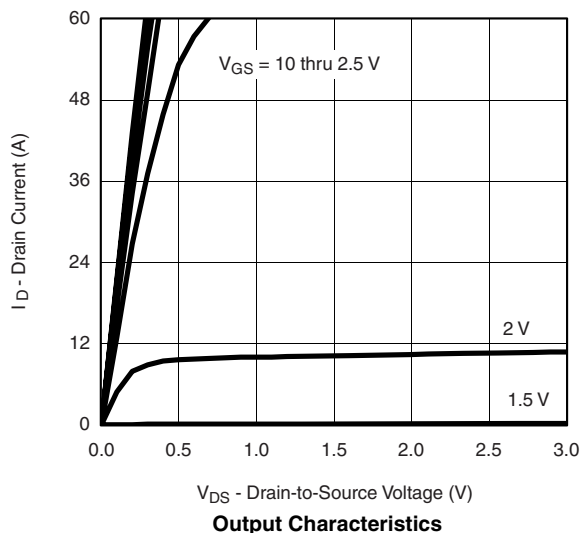
MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	40			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 4.5\text{ V}, I_D = 19.5\text{ A}$		0.0051	0.0062	Ω
		$V_{GS} = 2.5\text{ V}, I_D = 15.5\text{ A}$		0.0081	0.0098	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 19.5\text{ A}$		105		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.2\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 19.5\text{ A}$		17.5	27	nC
Gate-Source Charge	Q_{gs}		6.6			
Gate-Drain Charge	Q_{gd}		2.8			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.7	1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D = 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$		25	40	ns
Rise Time	t_r		15	25		
Turn-Off Delay Time	$t_{d(off)}$		50	75		
Fall Time	t_f		12	20		
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		30	60	

Notes:

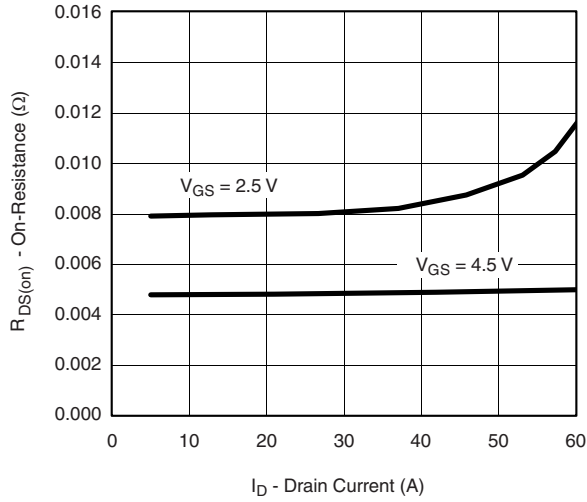
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

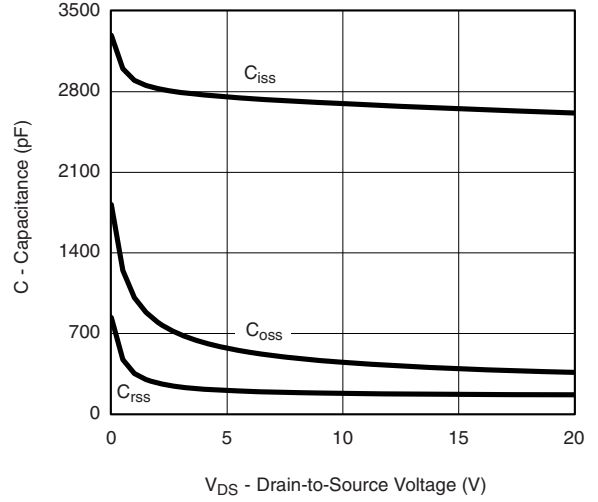
TYPICAL CHARACTERISTICS $25\text{ }^\circ\text{C}$, unless otherwise noted



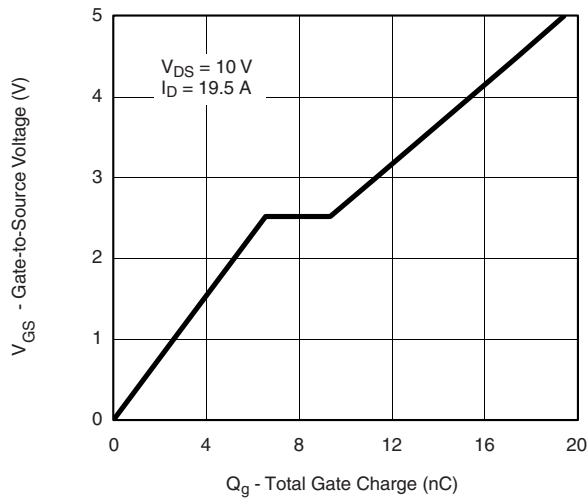
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



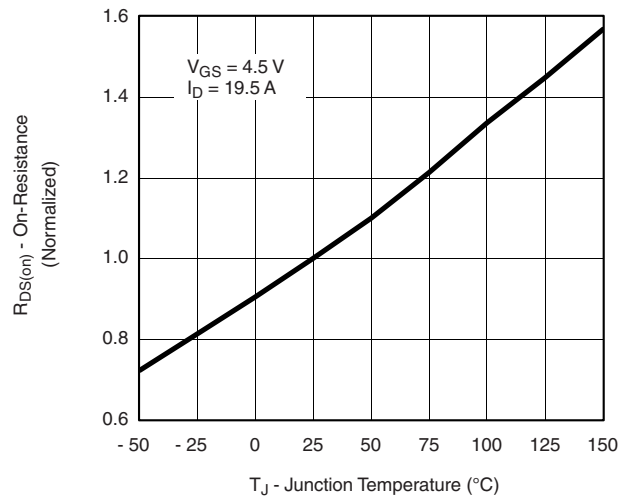
On-Resistance vs. Drain Current



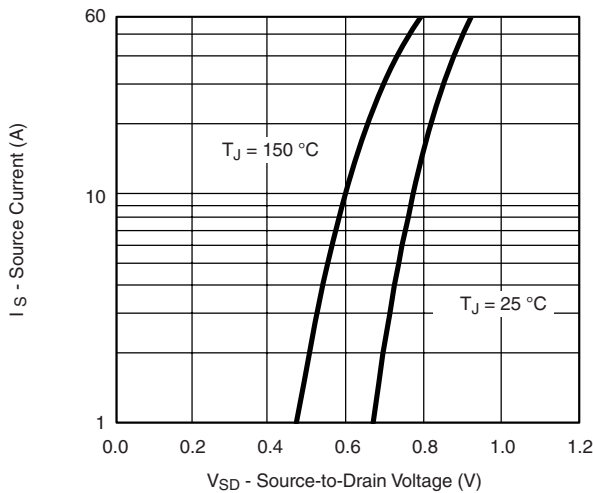
Capacitance



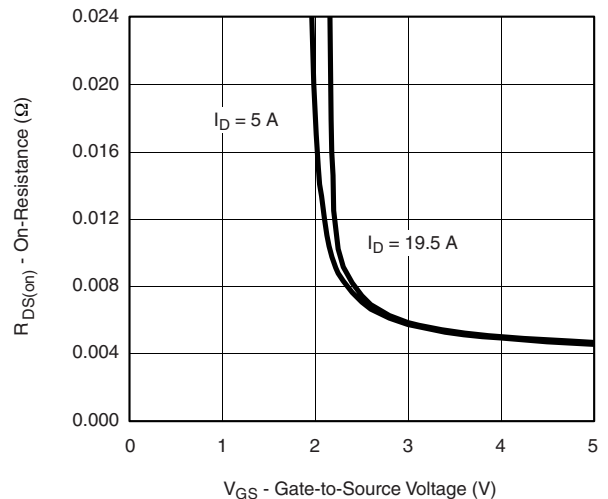
Gate Charge



On-Resistance vs. Junction Temperature

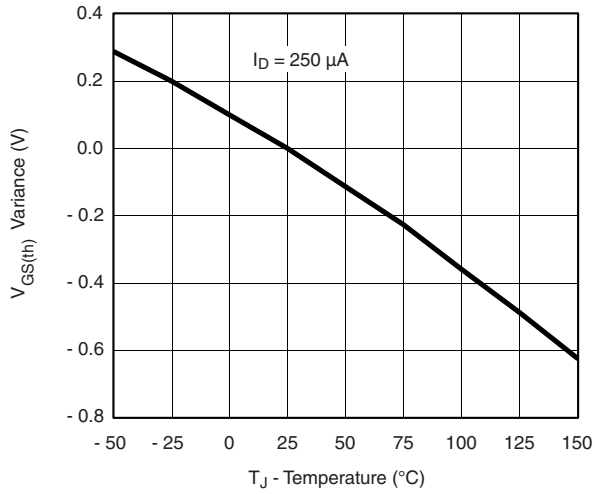


Source-Drain Diode Forward Voltage

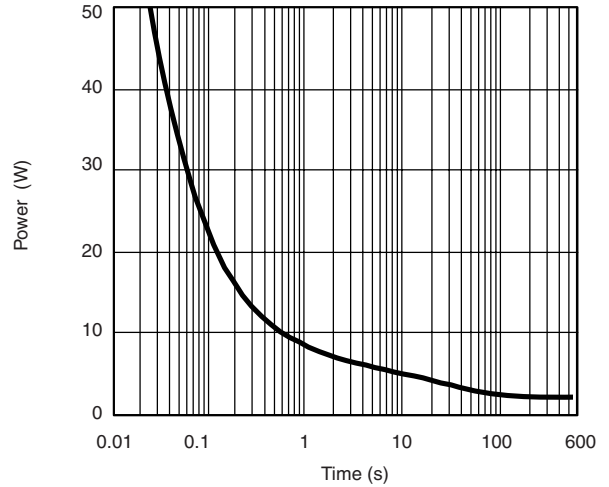


On-Resistance vs. Gate-to-Source Voltage

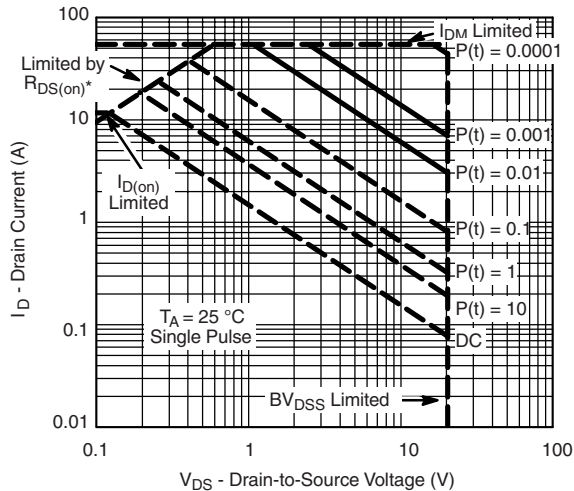
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Threshold Voltage

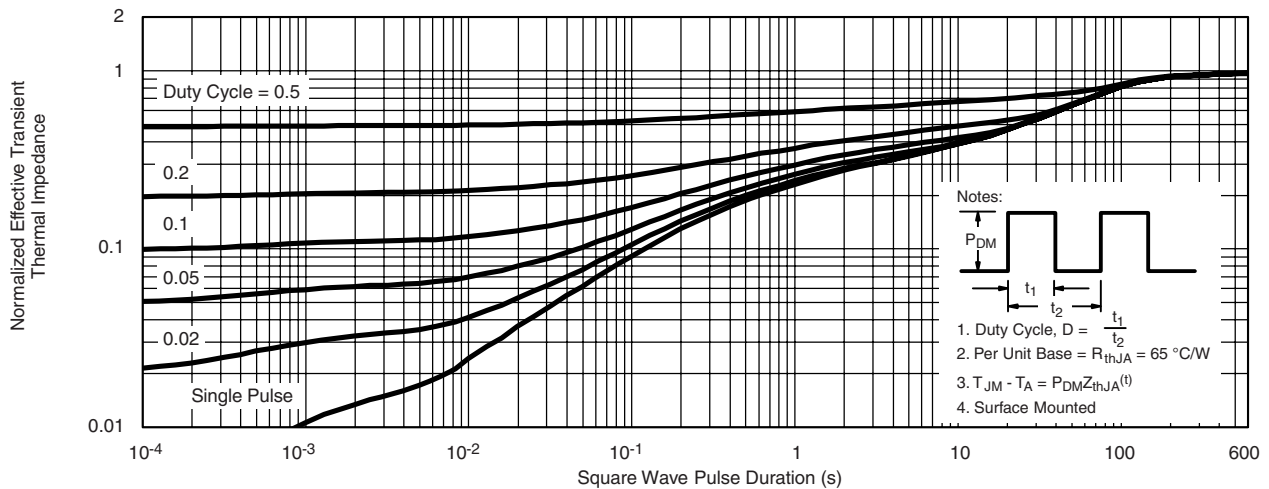


Single Pulse Power, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

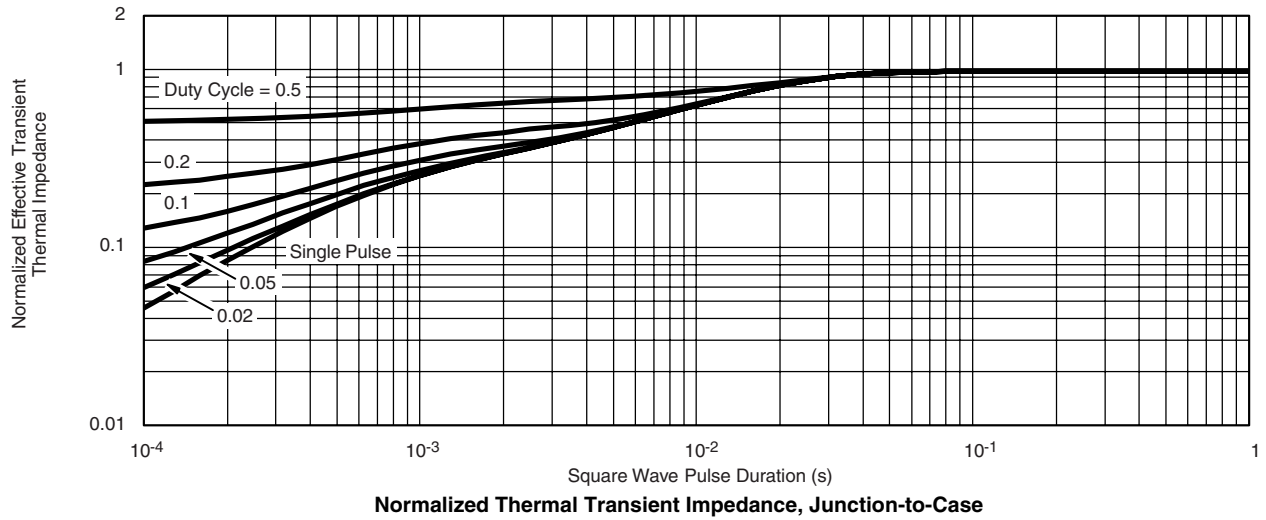
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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