

Complementary 30-V (D-S) MOSFET

PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
P-Channel	- 30	0.051 at V _{GS} = - 10 V	- 6.4
		0.075 at V _{GS} = - 6 V	- 5.3
N-Channel	30	0.035 at V _{GS} = 10 V	7.7
		0.050 at V _{GS} = 4.5 V	6.5

FEATURES

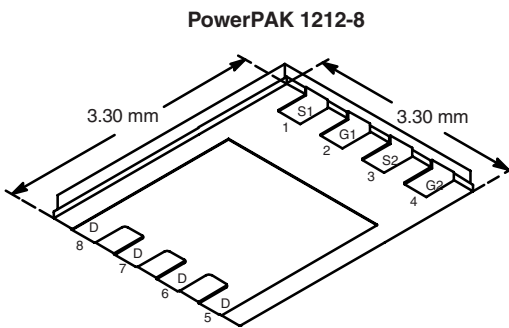
- Halogen-free Option Available
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance
- PowerPAK[®] Package with Low 1.07 mm Profile



RoHS
COMPLIANT

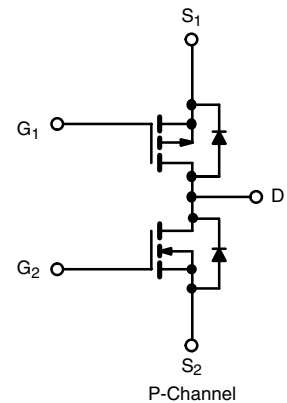
APPLICATIONS

- Backlight Inverter
- DC/DC Converter
- 4 Cell Battery



Bottom View

Ordering Information: Si7501DN-T1-E3 (Lead (Pb)-free)
Si7501DN-T1-GE3 (Lead (Pb)-free and Halogen-free)



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted							
Parameter	Symbol	P-Channel		N-Channel		Unit	
		10 s	Steady State	10 s	Steady State		
Drain-Source Voltage	V _{DS}	- 30		30		V	
Gate-Source Voltage	V _{GS}	± 25		± 20			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	- 6.4	- 4.5	7.7	5.4	A
		T _A = 70 °C	- 5.1	- 3.6	4.7	4.3	
Pulsed Drain Current	I _{DM}	- 25		25		W	
Continuous Source Current (Diode Conduction) ^a	I _S	- 2.6	- 1.3	2.6	1.3		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	3.1	1.6	3.1	1.6	W
		T _A = 70 °C	3	1.0	2	1.0	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C	
Soldering Recommendations (Peak Temperature) ^{b, c}		260					

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	32	40	°C/W
	Steady State		65	81	
Maximum Junction-to-Foot (Case)	Steady State	R _{thJC}	5	6.3	

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

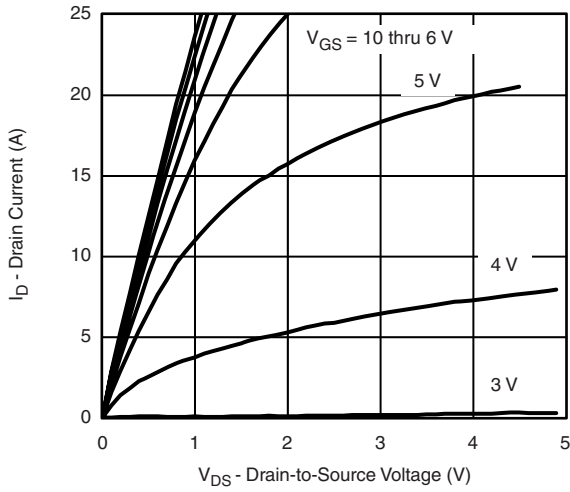
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-1.0		-3	V
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1.0		3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$	P-Ch			± 200	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-5	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-25			A
		$V_{DS} \leq 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	25			
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -6.4\text{ A}$	P-Ch		0.041	0.051	Ω
		$V_{GS} = 10\text{ V}, I_D = 7.7\text{ A}$	N-Ch		0.028	0.035	
		$V_{GS} = -6\text{ V}, I_D = -5.3\text{ A}$	P-Ch		0.055	0.075	
		$V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$	N-Ch		0.040	0.050	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -6.4\text{ A}$	P-Ch		13		S
		$V_{DS} = 15\text{ V}, I_D = 7.7\text{ A}$	N-Ch		15		
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.7\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		-0.80	-1.2	V
		$I_S = 1.7\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.80	1.2	
Dynamic^b							
Total Gate Charge	Q_g	P-Channel $V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -6.4\text{ A}$	P-Ch		12.5	19	nC
Gate-Source Charge	Q_{gs}		N-Ch		9	14	
Gate-Drain Charge	Q_{gd}	N-Channel $V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 7.7\text{ A}$	P-Ch		2.5		
			N-Ch		2		
Gate Resistance	R_g		P-Ch		9		Ω
			N-Ch		3		
Turn-On Delay Time	$t_{d(on)}$	P-Channel $V_{DD} = -15\text{ V}, R_L = 5\text{ }\Omega$ $I_D \cong -3\text{ A}, V_{GEN} = -10\text{ V}, R_G = 1\text{ }\Omega$	P-Ch		10	15	ns
Rise Time	t_r		N-Ch		10	15	
		P-Ch		20	30		
Turn-Off Delay Time	$t_{d(off)}$	N-Channel $V_{DD} = 15\text{ V}, R_L = 5\text{ }\Omega$ $I_D \cong 3\text{ A}, V_{GEN} = 10\text{ V}, R_G = 1\text{ }\Omega$	N-Ch		15	25	
			P-Ch		25	40	
Fall Time	t_f		N-Ch		20	30	
			P-Ch		30	45	
Source-Drain Reverse Recovery Time	t_{rr}		P-Ch		25	50	
			N-Ch		20	40	

Notes:

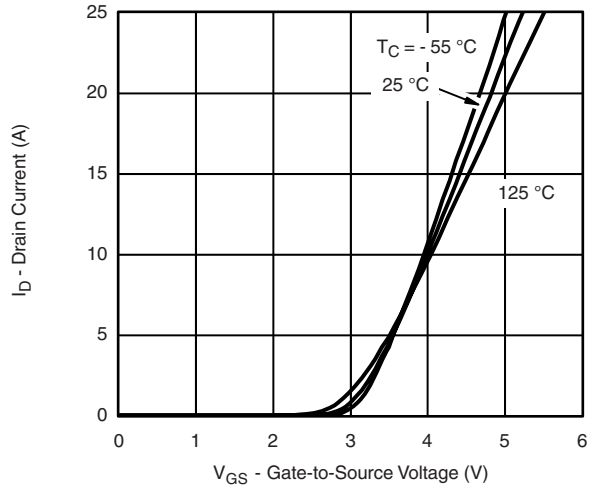
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

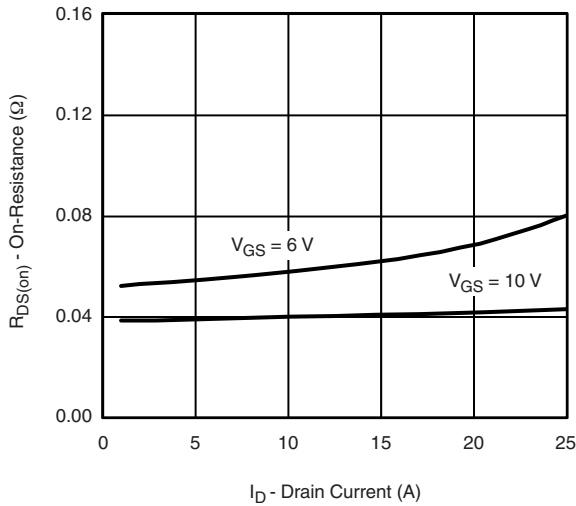
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



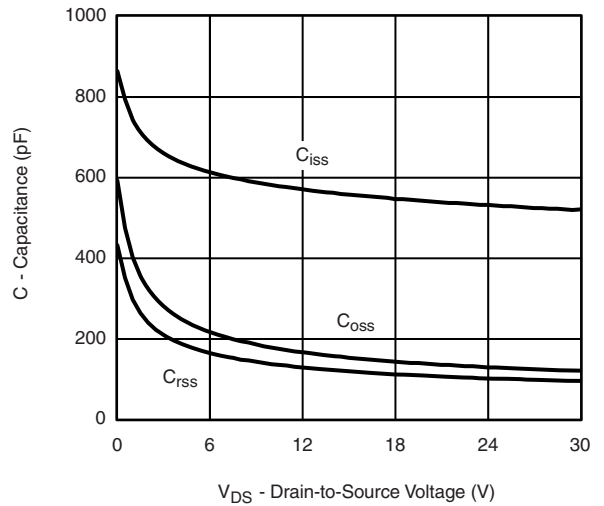
Output Characteristics



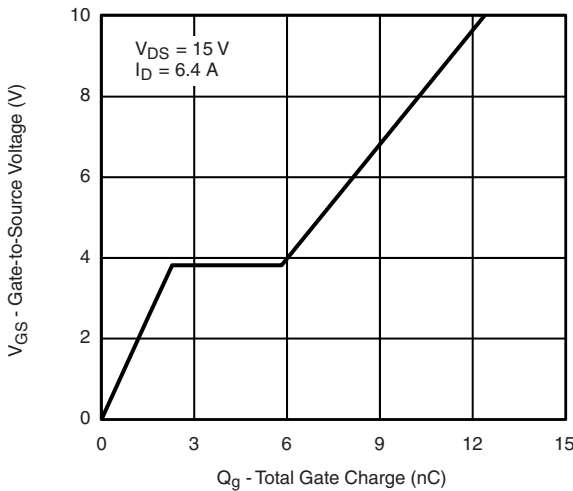
Transfer Characteristics



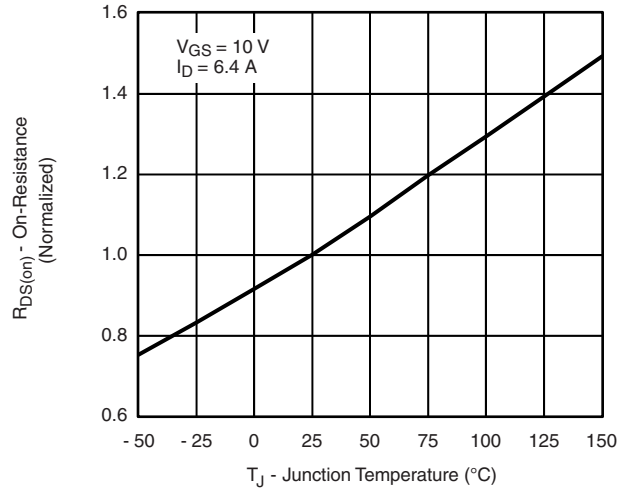
On-Resistance vs. Drain Current



Capacitance

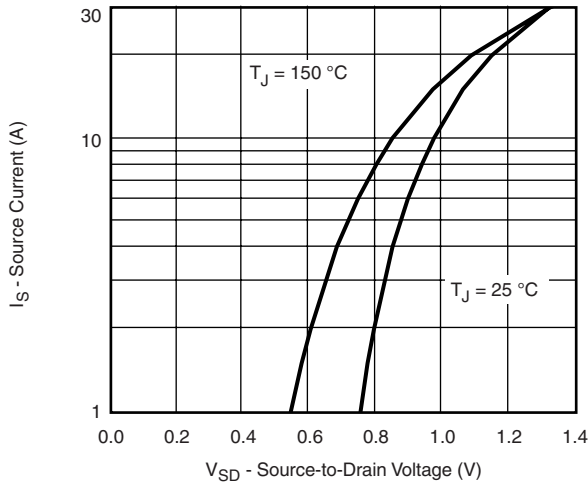


Gate Charge

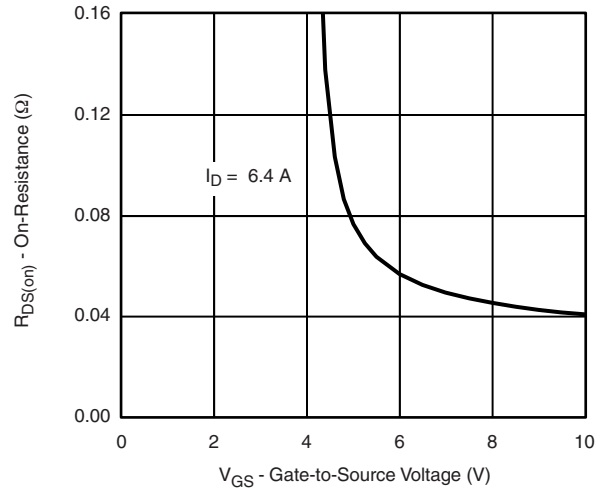


On-Resistance vs. Junction Temperature

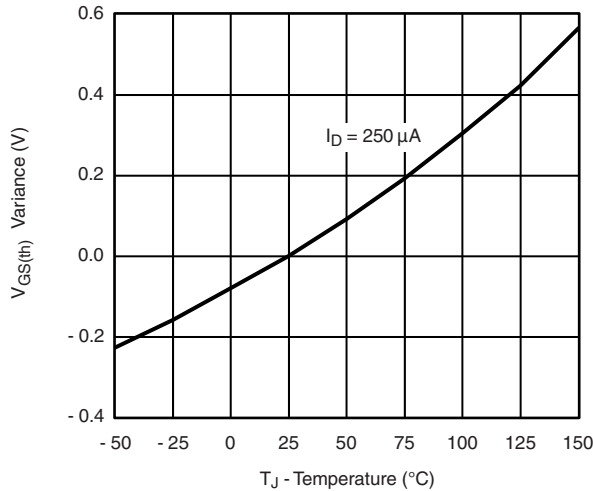
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



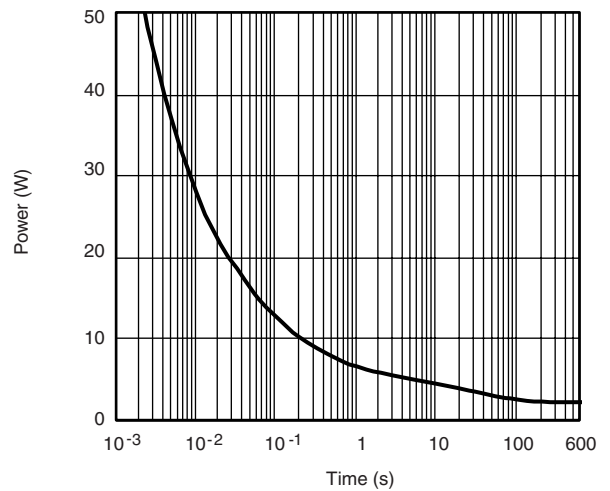
Source-Drain Diode Forward Voltage



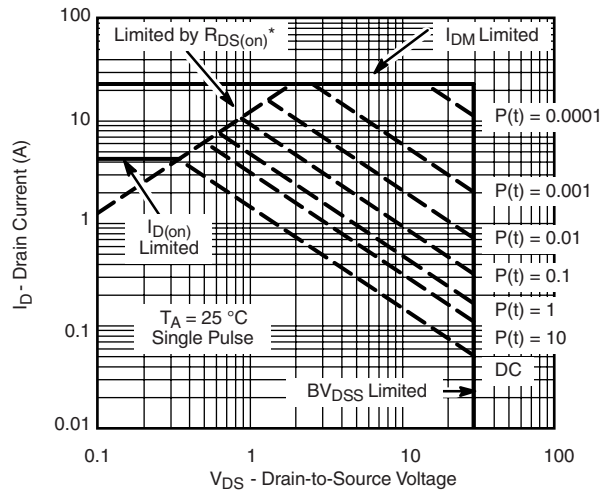
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



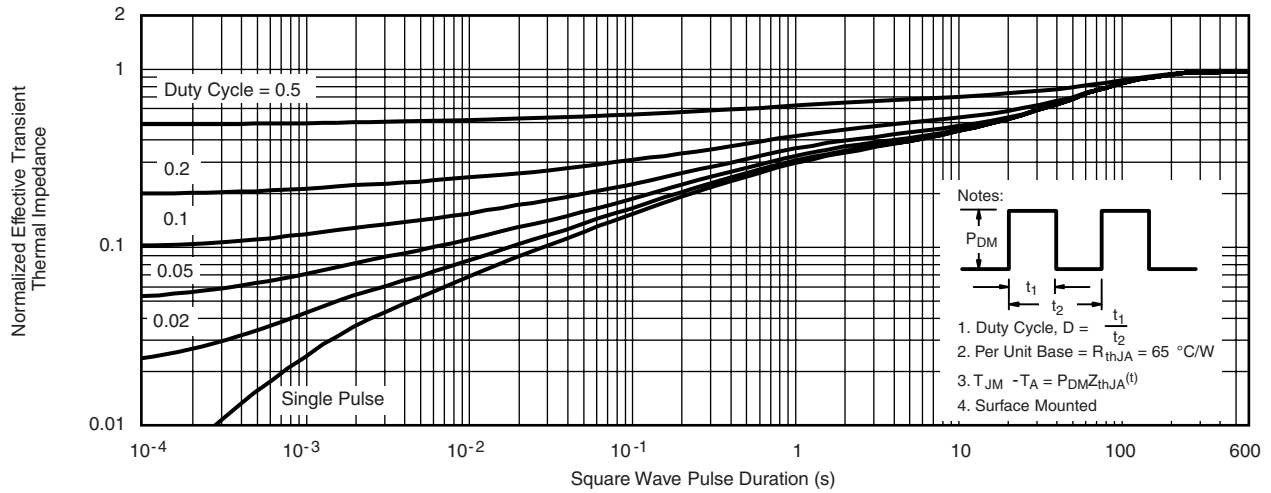
Single Pulse Power



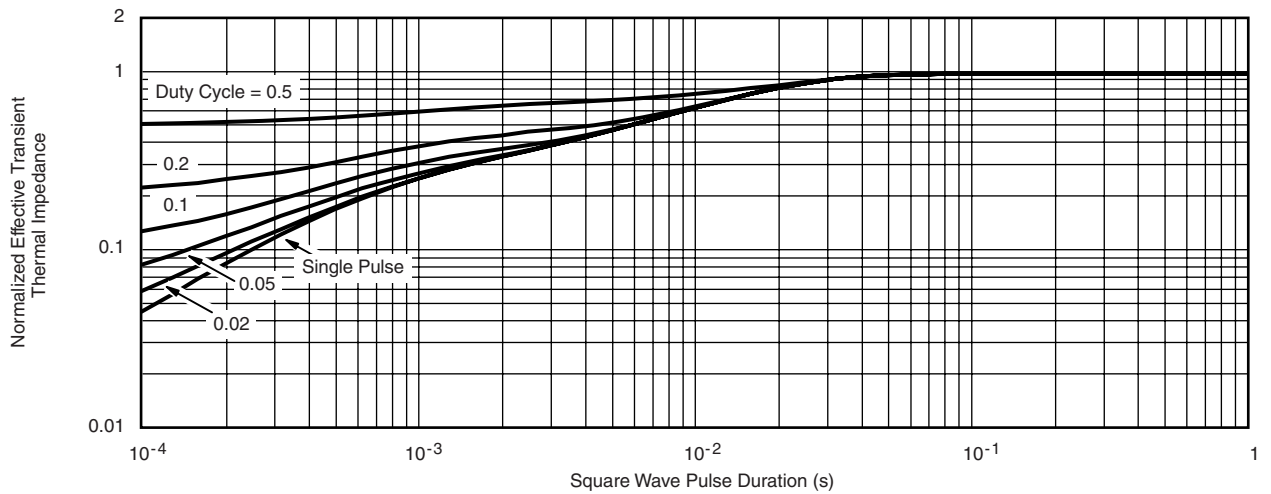
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

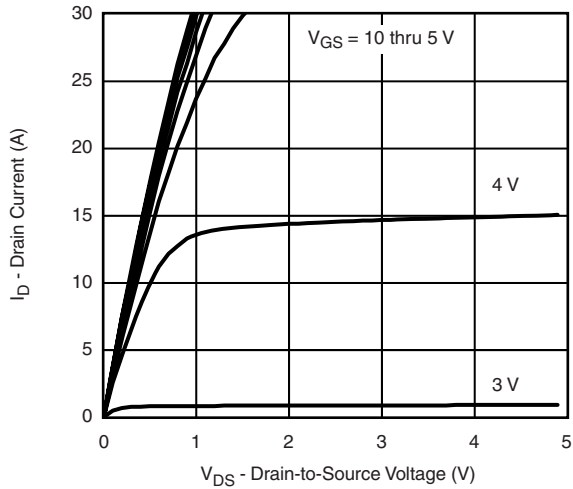


Normalized Thermal Transient Impedance, Junction-to-Ambient

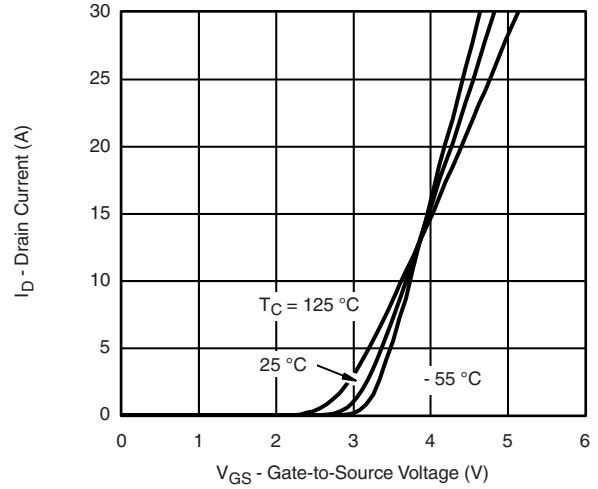


Normalized Thermal Transient Impedance, Junction-to-Case

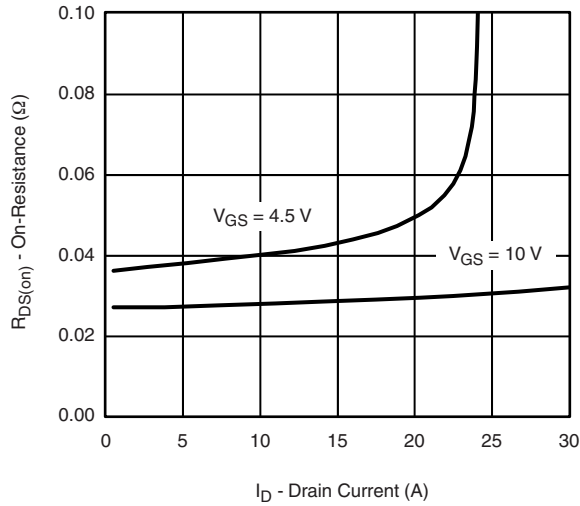
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



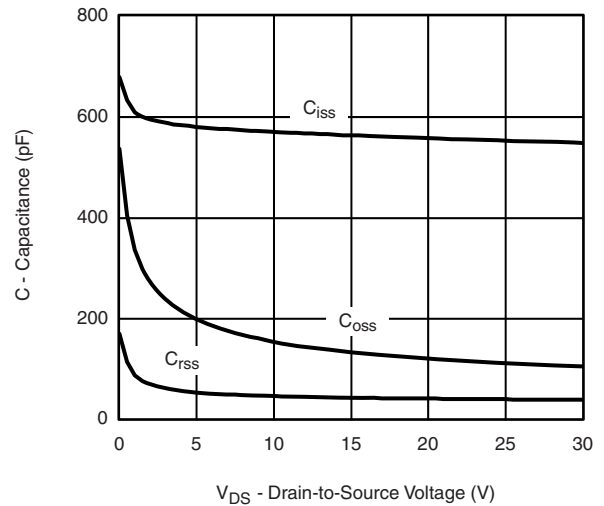
Output Characteristics



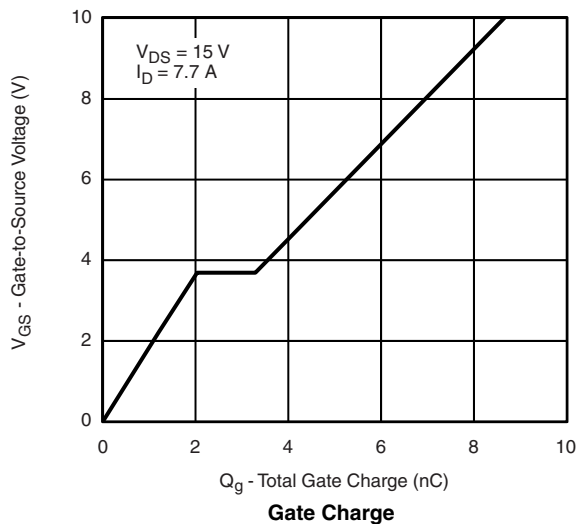
Transfer Characteristics



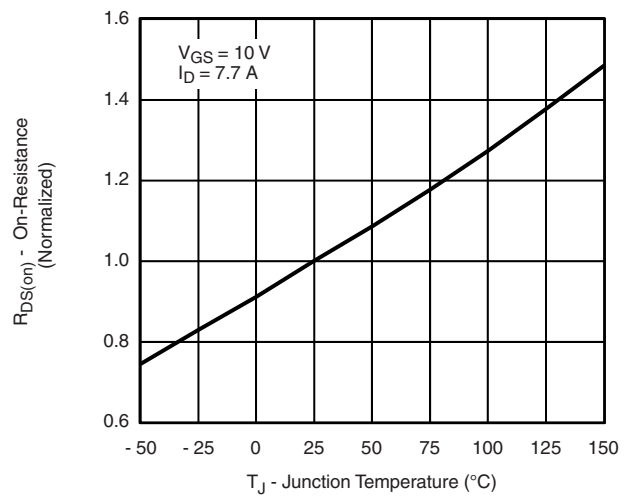
On-Resistance vs. Drain Current



Capacitance

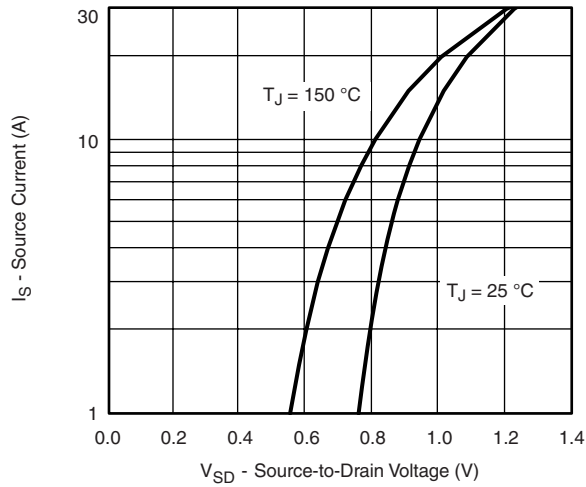


Gate Charge

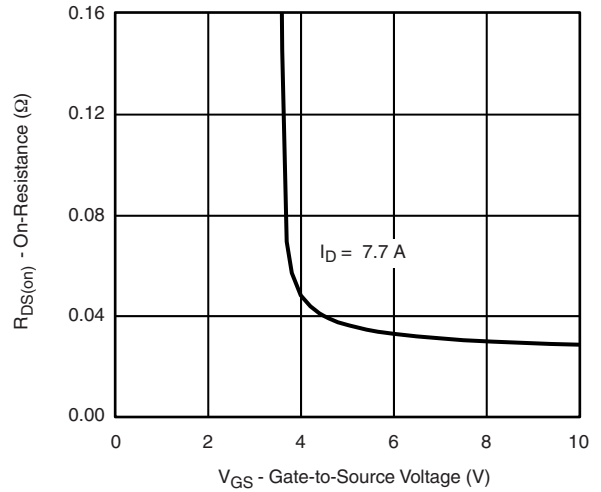


On-Resistance vs. Junction Temperature

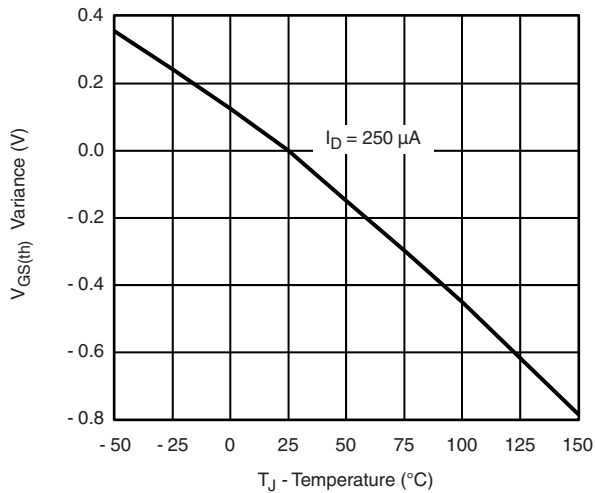
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



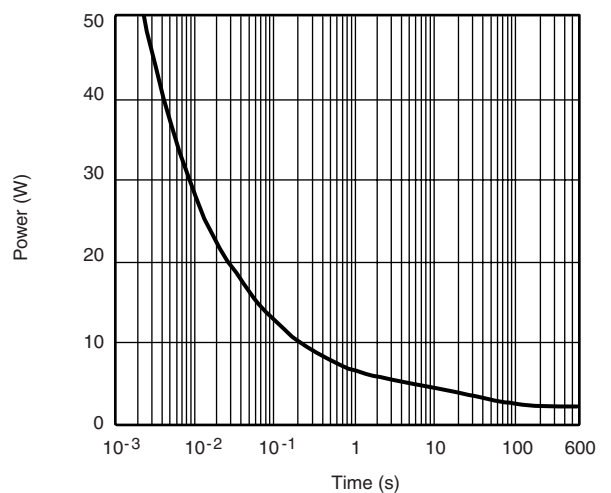
Source-Drain Diode Forward Voltage



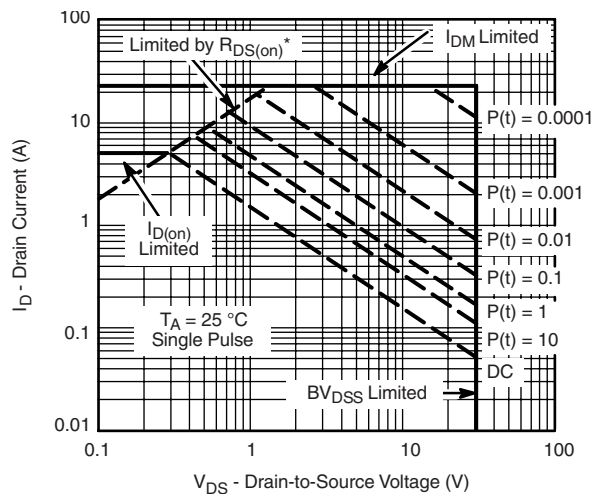
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



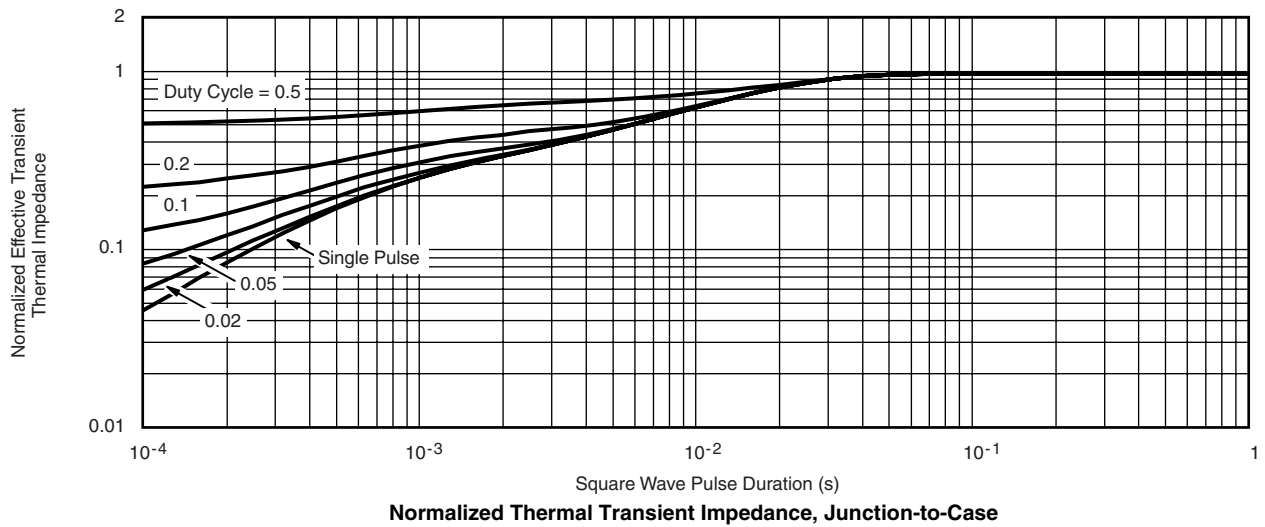
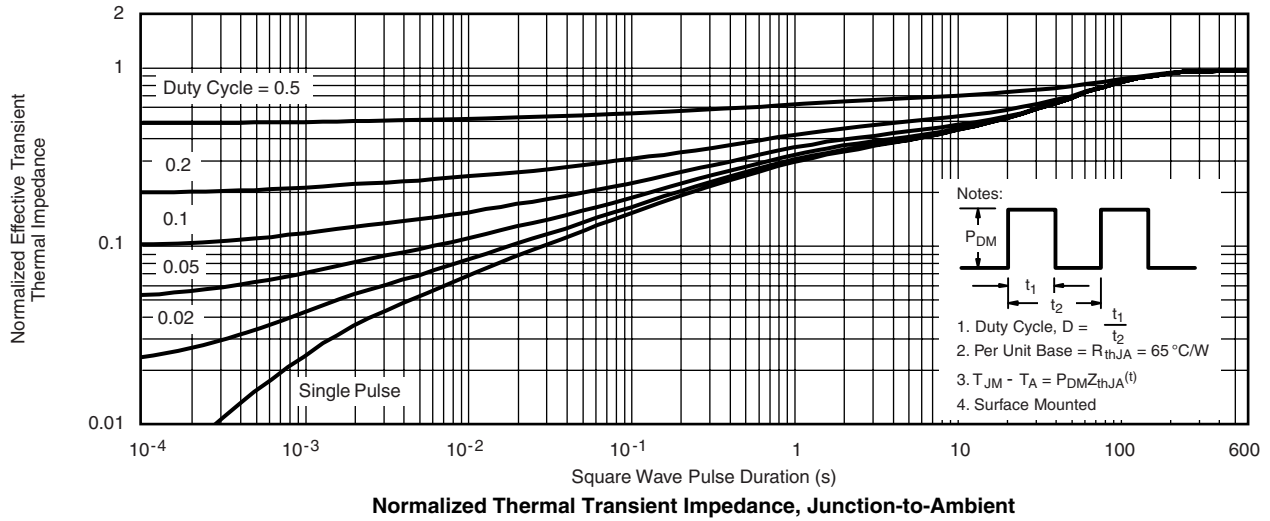
Single Pulse Power



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area

N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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