

## P-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) (MAX.)	I <sub>D</sub> (A) <sup>e</sup>	Q <sub>g</sub> (TYP.)
-12	0.026 at V <sub>GS</sub> = -4.5 V	-16	21 nC
	0.035 at V <sub>GS</sub> = -2.5 V	-16	
	0.055 at V <sub>GS</sub> = -1.8 V	-13	
	0.092 at V <sub>GS</sub> = -1.5 V	-2.5	



**Marking Code:** xxxx = 8483  
xxx = Date / lot traceability code

**Ordering Information:**  
Si8483DB-T2-E1 (Lead (Pb)-free and halogen-free)

### FEATURES

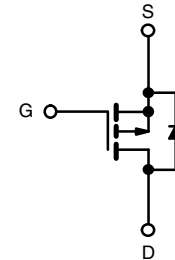
- TrenchFET® power MOSFET
- Ultra-small 1.5 mm x 1 mm maximum outline
- Ultra-thin 0.59 mm maximum height
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Load switch for smart phones, tablet PCs, and mobile computing
- Low voltage drop
- Low power consumption
- Increased battery life



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	-12	V
Gate-Source Voltage	V <sub>GS</sub>	± 10	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	-16
		T <sub>C</sub> = 70 °C	-15
		T <sub>A</sub> = 25 °C	-8.7 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	-7 <sup>a, b</sup>
Pulsed Drain Current	I <sub>DM</sub>	-25	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	
		T <sub>A</sub> = 25 °C	-2.3 <sup>a, b</sup>
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	13
		T <sub>C</sub> = 70 °C	8.4
		T <sub>A</sub> = 25 °C	2.77 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	1.77 <sup>a, b</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Package Reflow Conditions <sup>c</sup>	IR/Convection	260	

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient <sup>a, f</sup>	R <sub>thJA</sub>	37	45	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	7	9.5	

### Notes

- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
- Case is defined as the top surface of the package.
- Based on T<sub>C</sub> = 25 °C.
- Maximum under steady state conditions is 85 °C/W.



SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0, I <sub>D</sub> = -250 μA	-12	-	-	V	
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = -250 μA	-	-7	-	mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>		-	2.8	-		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	-0.4	-	-0.8	V	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 10 V	-	-	± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -12 V, V <sub>GS</sub> = 0 V	-	-	-1	μA	
		V <sub>DS</sub> = -12 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	-10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	-5	-	-	A	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.5 A	-	0.022	0.026	Ω	
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -1.5 A	-	0.028	0.035		
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -1 A	-	0.040	0.055		
		V <sub>GS</sub> = -1.5 V, I <sub>D</sub> = -0.5 A	-	0.056	0.092		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -6 V, I <sub>D</sub> = -1.5 A	-	10	-	S	
<b>Dynamic<sup>b</sup></b>							
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = -6 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	1840	-	pF	
Output Capacitance	C <sub>OSS</sub>		-	410	-		
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	380	-		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -1.5 A	-	43	65	nC	
			V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.5 A	-	21		32
				-	2.1		-
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> = -6 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.5 A	-	4.8	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>		-	2.1	-		
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> = -0.1 V, f = 1 MHz	-	2.2	-	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -6 V, R <sub>L</sub> = 4 Ω I <sub>D</sub> ≅ -1.5 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 1 Ω	-	20	40	ns	
Rise Time	t <sub>r</sub>		-	25	50		
Turn-Off Delay Time	t <sub>d(off)</sub>		-	40	80		
Fall Time	t <sub>f</sub>		-	10	20		
Turn-On Delay Time	t <sub>d(on)</sub>		-	10	20		
Rise Time	t <sub>r</sub>		-	10	20		
Turn-Off Delay Time	t <sub>d(off)</sub>		-	40	80		
Fall Time	t <sub>f</sub>		-	10	20		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	-10.8	A	
Pulse Diode Forward Current	I <sub>SM</sub>		-	-	-25	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = -1.5 A, V <sub>GS</sub> = 0	-	-0.8	-1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = -1.5 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	30	60	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	12	25	nC	
Reverse Recovery Fall Time	t <sub>a</sub>		-	11.5	-	ns	
Reverse Recovery Rise Time	t <sub>b</sub>		-	18.5	-		

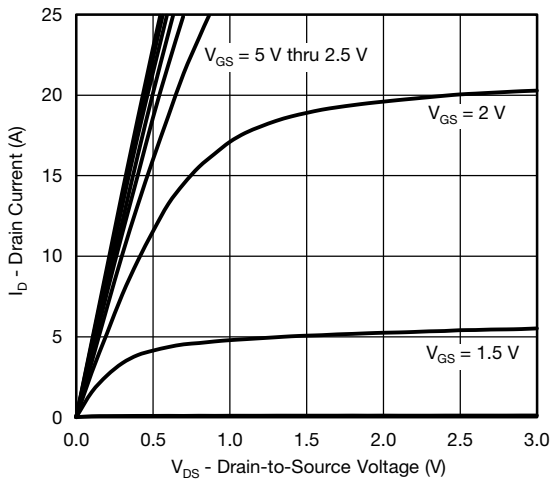
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

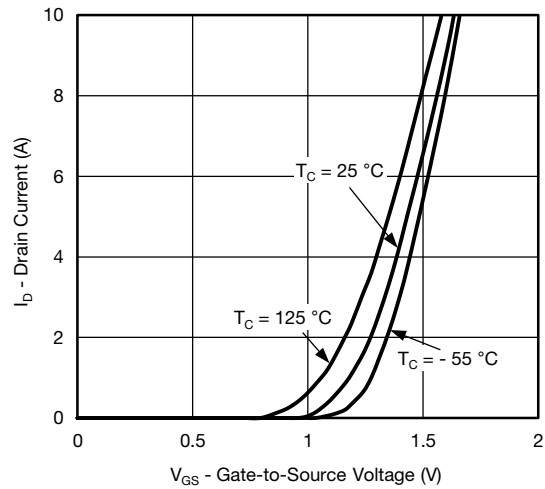
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



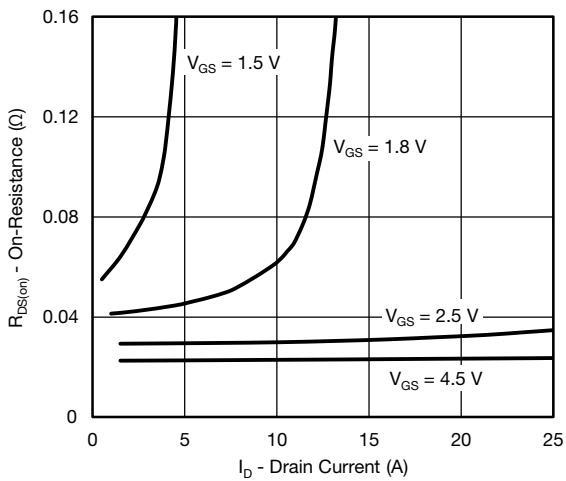
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



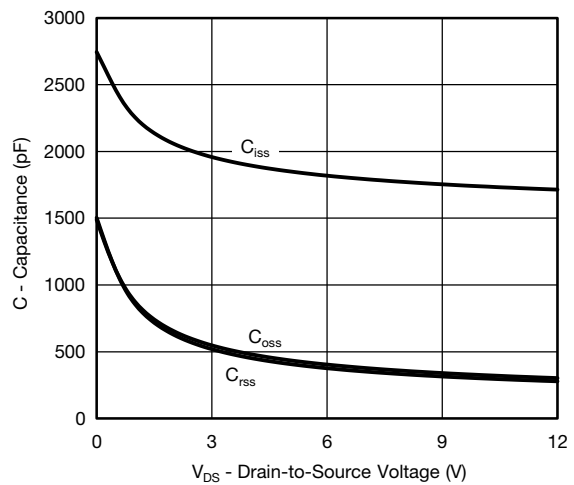
Output Characteristics



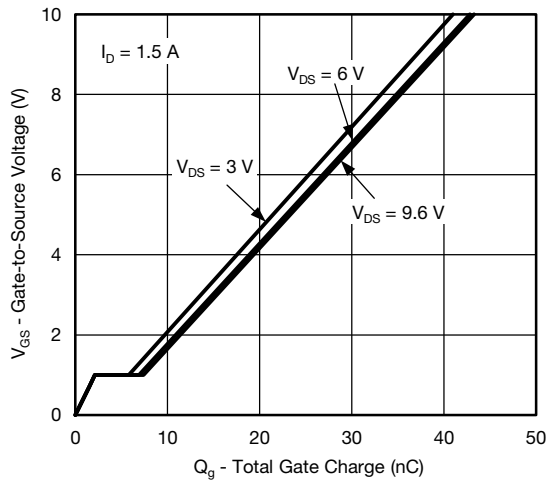
Transfer Characteristics



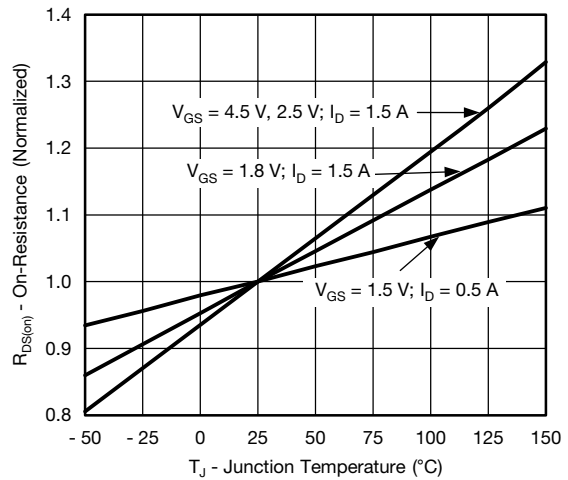
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

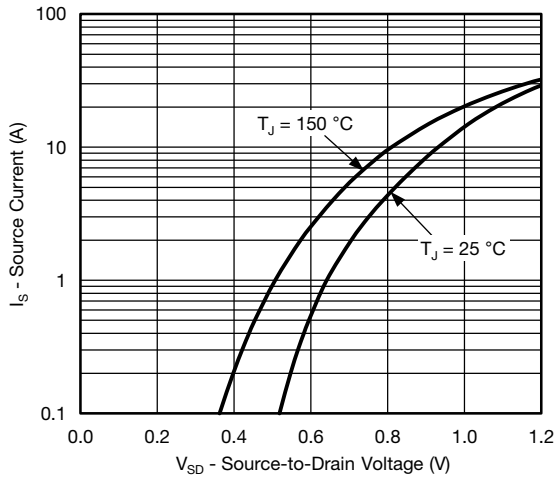


Gate Charge

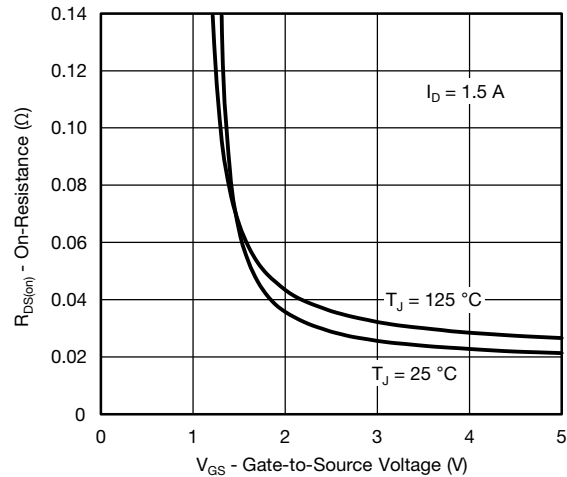


On-Resistance vs. Junction Temperature

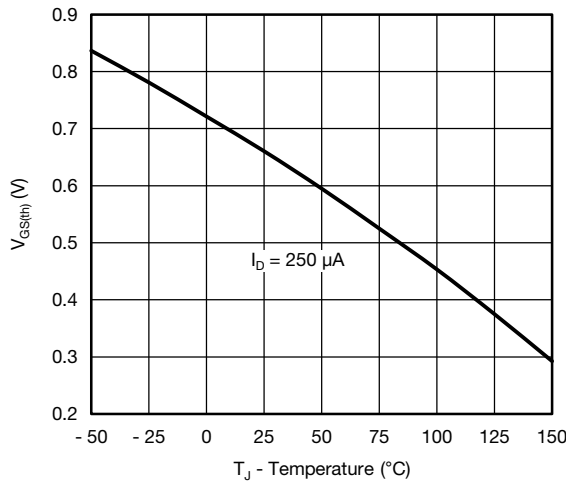
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



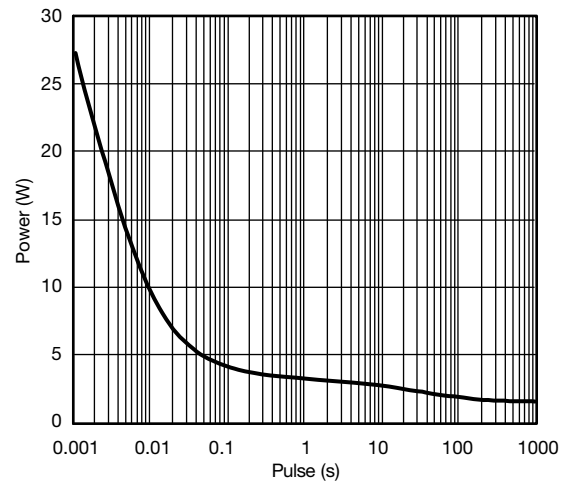
**Source-Drain Diode Forward Voltage**



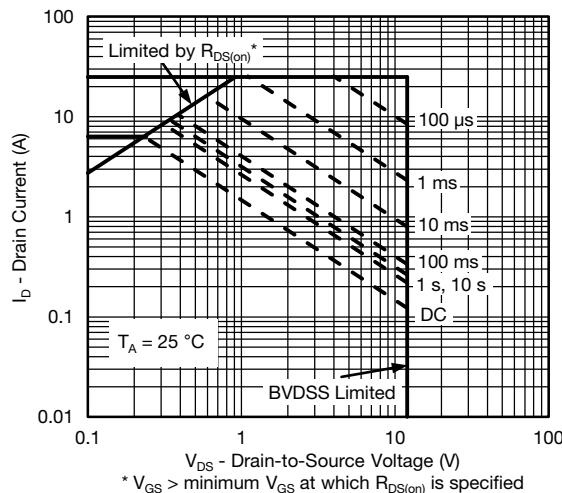
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



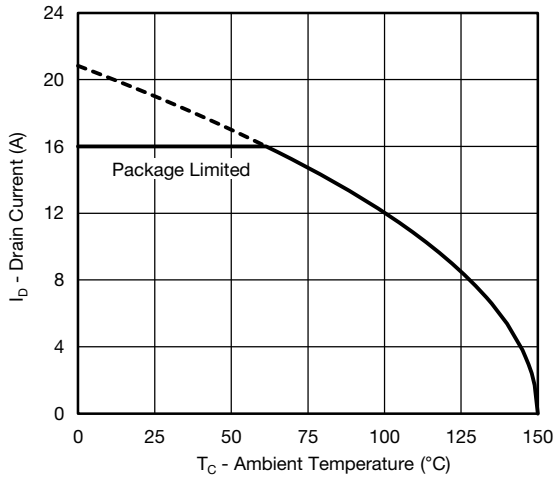
**Single Pulse Power, Junction-to-Ambient**



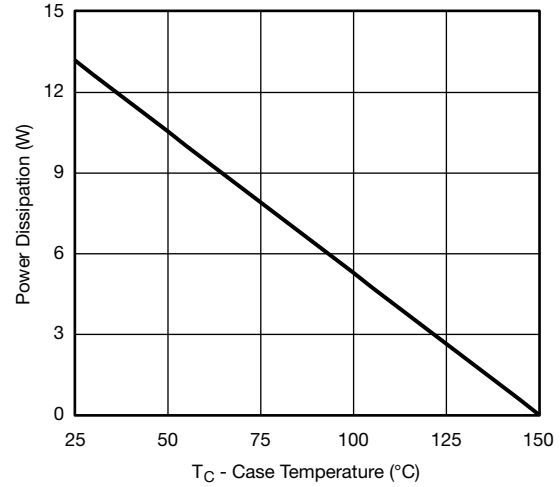
**Safe Operating Area, Junction-to-Ambient**



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



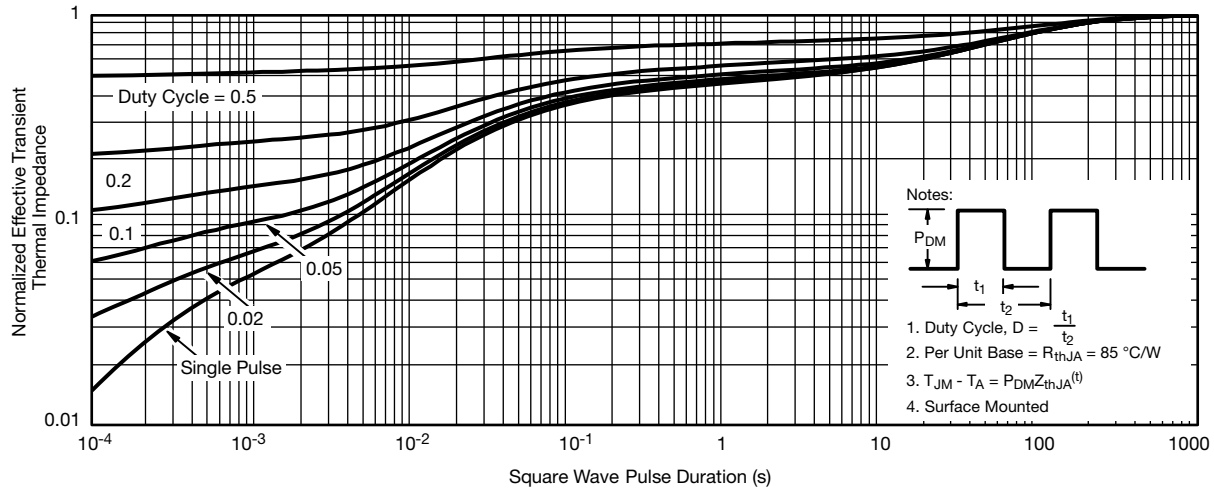
**Current Derating\***



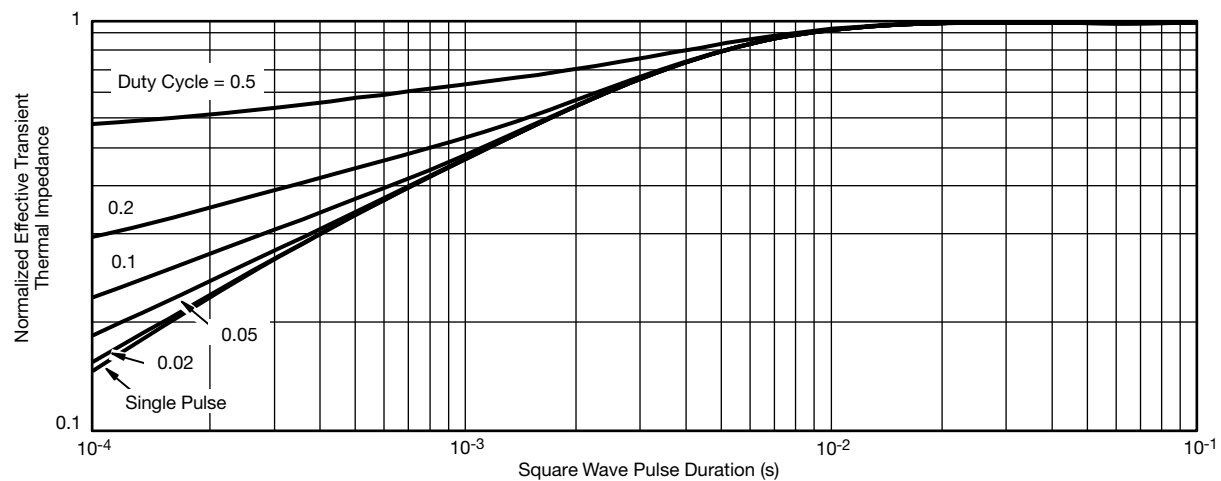
**Power Derating**

\* The power dissipation P<sub>D</sub> is based on T<sub>J</sub> (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?63553](http://www.vishay.com/ppg?63553).

## MICRO FOOT®: 6-Bump (1.5 mm x 1 mm, 0.5 mm Pitch, 0.250 mm Bump Height)



### Notes

(unless otherwise specified)

1. Six (6) solder bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.
5. "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.510	0.575	0.590	0.0201	0.0226	0.0232
A <sub>1</sub>	0.220	0.250	0.280	0.0087	0.0098	0.0110
A <sub>2</sub>	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.297	0.330	0.363	0.0116	0.0129	0.0143
b1		0.250			0.0098	
e		0.500			0.0197	
s	0.210	0.230	0.250	0.0082	0.0090	0.0098
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
E	1.420	1.460	1.500	0.0559	0.0575	0.0591
K	0.028	0.065	0.102	0.0011	0.0025	0.0040

### Note

- Use millimeters as the primary measurement.

ECN: T15-0140-Rev. A, 20-Apr-15  
DWG: 6035



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