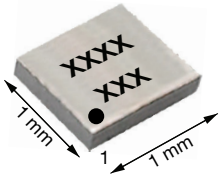
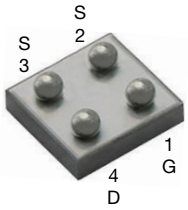
P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω) MAX.	I_D (A) [a, e]	Q_g (TYP.)
-20	0.044 at V_{GS} = -10 V	-5.4	9.5 nC
	0.054 at V_{GS} = -4.5 V	-4.9	
	0.082 at V_{GS} = -2.5 V	-3.9	

MICRO FOOT® 1 x 1



Backside View



Bump Side View

Marking Code: xxxx = 8489
xxx = Date / lot traceability code

Ordering Information:
Si8489EDB-T2-E1 (lead (Pb)-free and halogen-free)

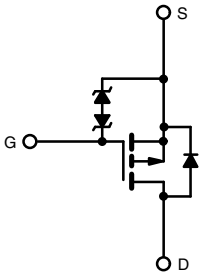
FEATURES

- TrenchFET® power MOSFET
- Small 1 mm x 1 mm max. outline area
- Low 0.548 mm max. profile
- Typical ESD protection 2500 V HBM
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Load switches and charger switches
- Battery management
- For smart phones and tablet PCs



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C)	T_A = 25 °C	I_D	-5.4 [a]	A
	T_A = 70 °C		-4.3 [a]	
	T_A = 25 °C		-3.6 [b]	
	T_A = 70 °C		-2.8 [b]	
Pulsed Drain Current (t = 300 µs)		I_{DM}	-20	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	-1.5 [a]	
	T_A = 25 °C		-0.65 [b]	
Maximum Power Dissipation	T_A = 25 °C	P_D	1.8 [a]	W
	T_A = 70 °C		1.1 [a]	
	T_A = 25 °C		0.78 [b]	
	T_A = 70 °C		0.5 [b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Package Reflow Conditions [c]	VPR		260	
	IR/Convection		260	

Notes

a. Surface mounted on 1" x 1" FR4 board with full copper, t = 10 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 10 s.
c. Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
e. Based on T_A = 25 °C.

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THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYPICAL**	**MAXIMUM**	**UNIT**
Maximum Junction-to-Ambient [a, b]	t = 10 s	R_{thJA}	55	70	°C/W
Maximum Junction-to-Ambient [c, d]	t = 10 s		125	160	

Notes

a. Surface mounted on 1" x 1" FR4 board with full copper.
b. Maximum under steady state conditions is 100 °C/W.
c. Surface mounted on 1" x 1" FR4 board with minimum copper.
d. Maximum under steady state conditions is 190 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-20	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = -250 µA	-	-15	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	2.4	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-0.5	-	-1.2	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V	-	-	± 1	µA
		V_{DS} = 0 V, V_{GS} = ± 12 V	-	-	± 5	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -20 V, V_{GS} = 0 V	-	-	-1	
		V_{DS} = -20 V, V_{GS} = 0 V, T_J = 70 °C	-	-	-10	
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} \leq$ -5 V, V_{GS} = -4.5 V	-10	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V, I_D = -1.5 A	-	0.036	0.044	Ω
		V_{GS} = -4.5 V, I_D = -1.5 A	-	0.045	0.054	
		V_{GS} = -2.5 V, I_D = -1 A	-	0.065	0.082	
Forward Transconductance [a]	g_{fs}	V_{DS} = -10 V, I_D = -1.5 A	-	10	-	S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz	-	765	-	pF
Output Capacitance	C_{oss}		-	125	-	
Reverse Transfer Capacitance	C_{rss}		-	115	-	
Total Gate Charge	Q_g	V_{DS} = -10 V, V_{GS} = -10 V, I_D = -1.5 A	-	17.5	27	nC
		V_{DS} = -10 V, V_{GS} = -4.5 V, I_D = -1.5 A	-	8.6	13	
Gate-Source Charge	Q_{gs}		-	1.5	-	
Gate-Drain Charge	Q_{gd}		-	2.6	-	
Gate Resistance	R_g	V_{GS} = -0.1 V, f = 1 MHz	-	14	-	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 10 Ω $I_D \cong$ -1.5 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	27	50	ns
Rise Time	t_r		-	20	40	
Turn-Off Delay Time	$t_{d(off)}$		-	50	100	
Fall Time	t_f		-	25	50	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 10 Ω $I_D \cong$ -1.5 A, V_{GEN} = -8 V, R_g = 1 Ω	-	6	15	
Rise Time	t_r		-	8	20	
Turn-Off Delay Time	$t_{d(off)}$		-	68	130	
Fall Time	t_f		-	28	60	

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SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_A = 25 °C	-	-	-1.5	A
Pulse Diode Forward Current	I_{SM}		-	-	-20	
Body Diode Voltage	V_{SD}	I_S = -1.5 A, V_{GS} = 0 V	-	-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = -1.5 A, dI/dt = 100 A/µs, T_J = 25 °C	-	25	50	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	9	20	nC
Reverse Recovery Fall Time	t_a		-	15	-	ns
Reverse Recovery Rise Time	t_b		-	10	-	

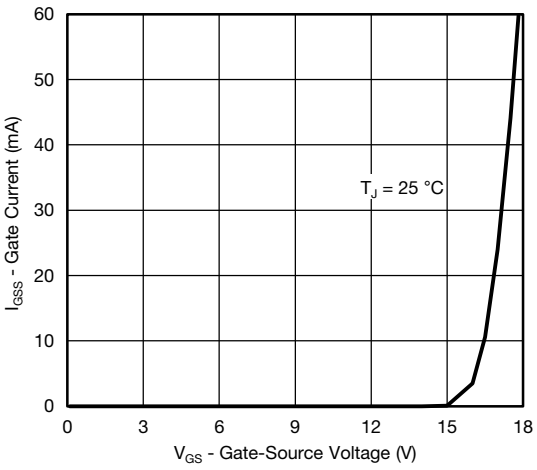
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

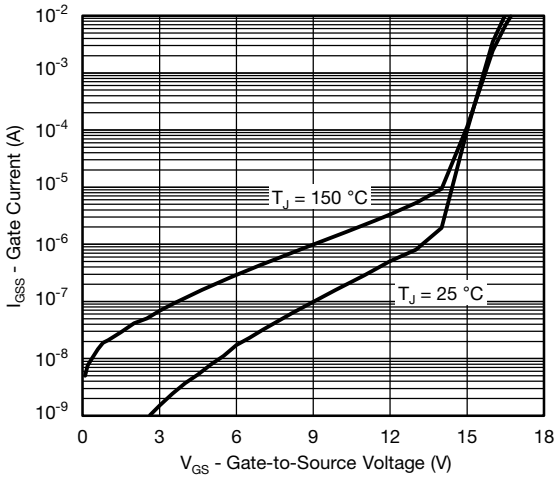
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

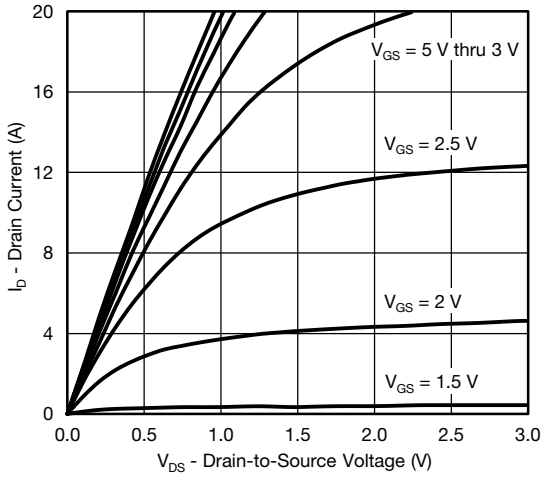
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



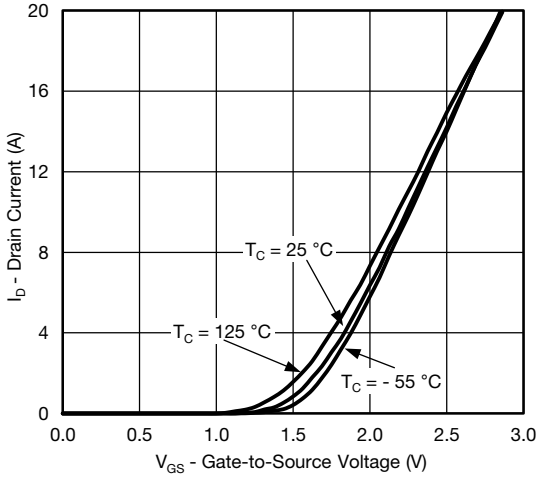
Gate Current vs. Gate-Source Voltage



Gate Current vs. Gate-Source Voltage



Output Characteristics



Transfer Characteristics

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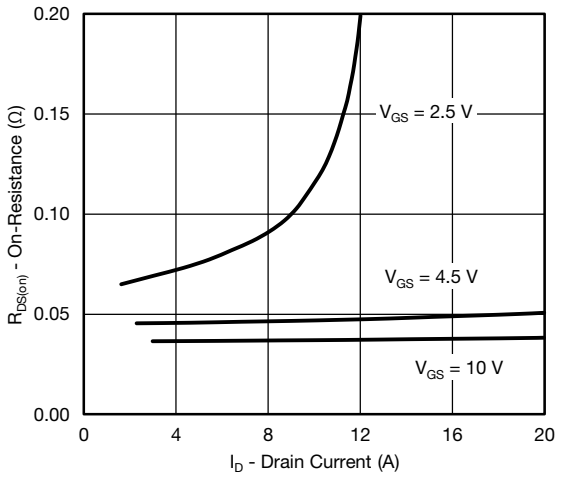
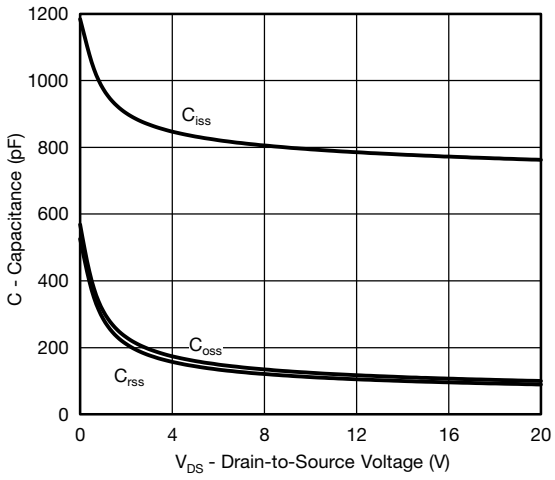
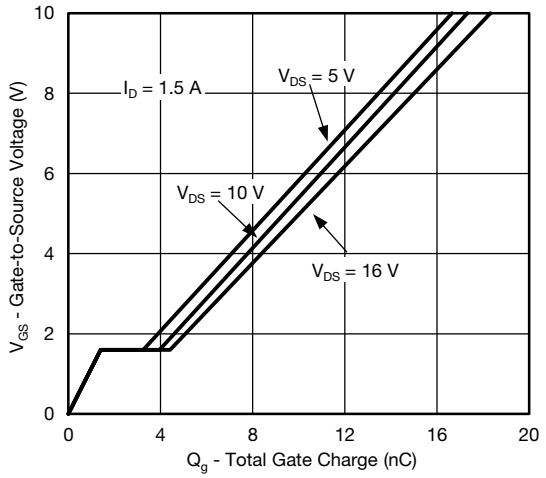


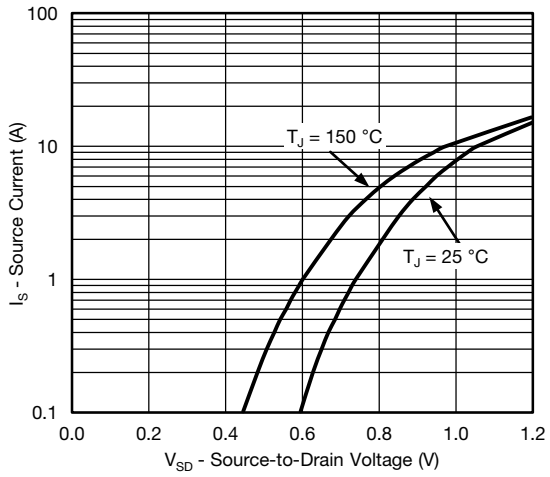
On-Resistance vs. Drain Current and Gate Voltage



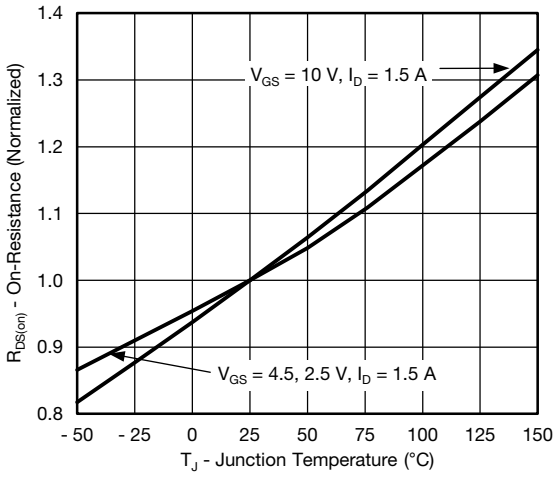
Capacitance



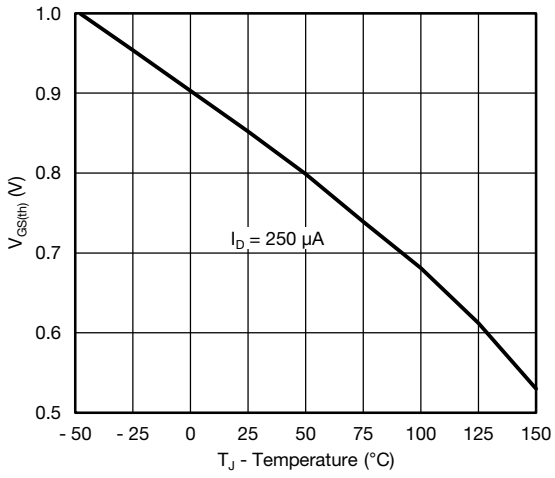
Gate Charge



Source-Drain Diode Forward Voltage



On-Resistance vs. Junction Temperature



Threshold Voltage

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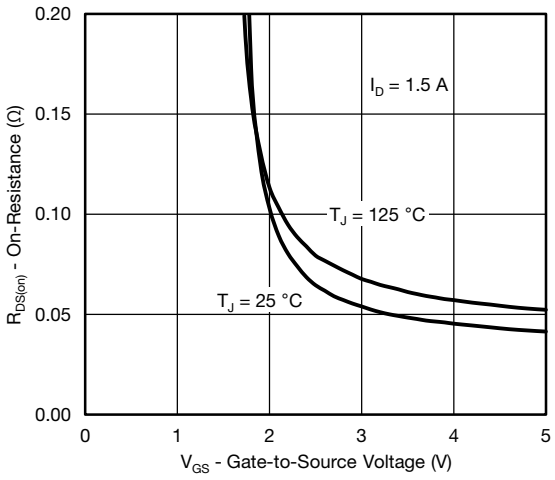
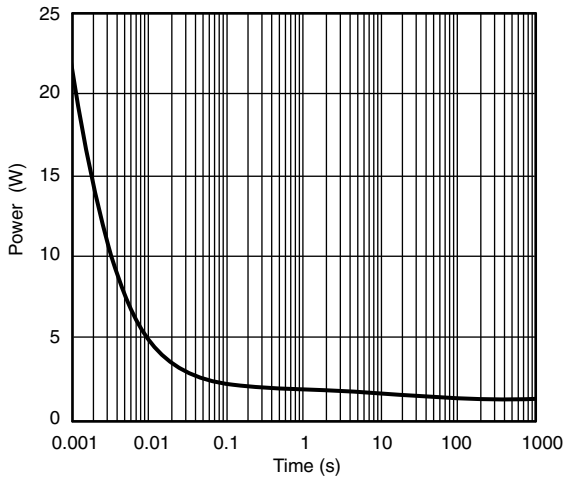
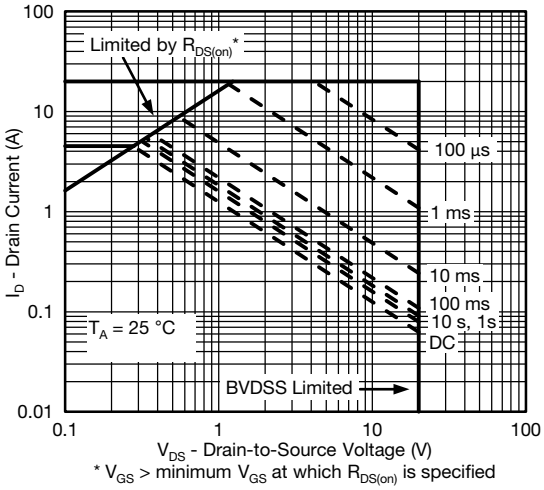


On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



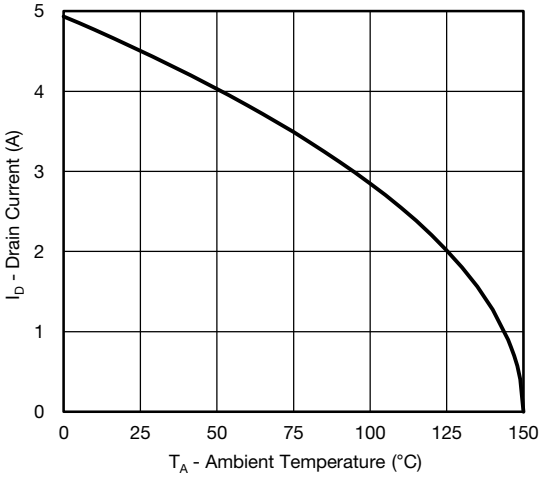
Safe Operating Area, Junction-to-Ambient

Note

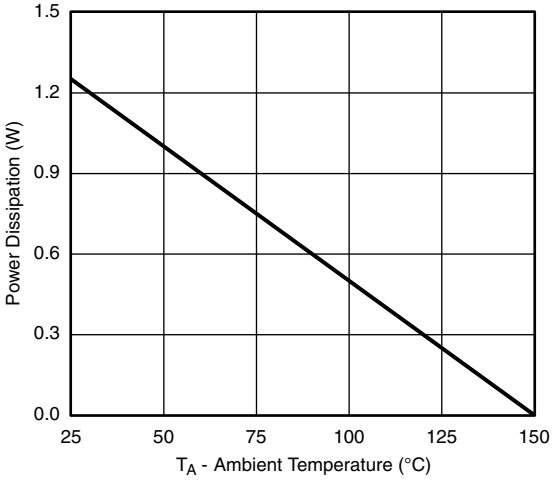
- When mounted on 1" x 1" FR4 with full copper.

Note

a. The power dissipation P_D is based on T_J (max.) = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Current Derating [a]



Power Derating

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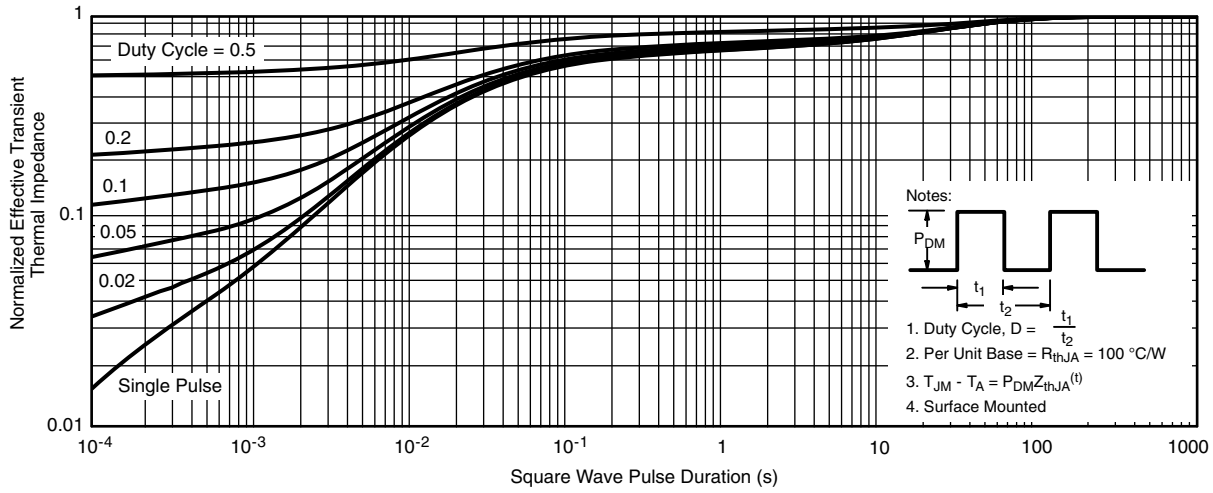
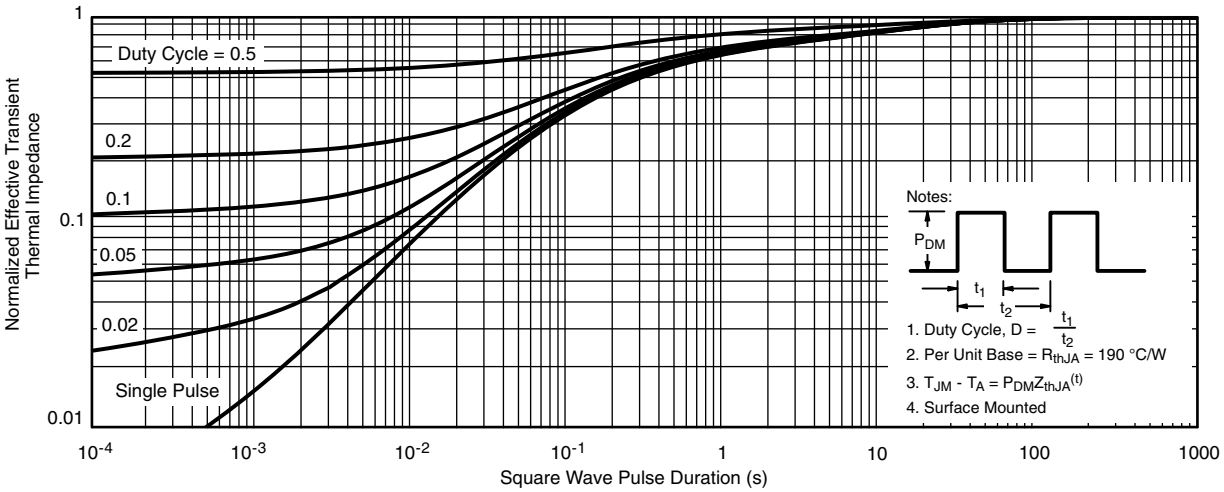


Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Full Copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (1" x 1" FR4 Board with Minimum Copper)

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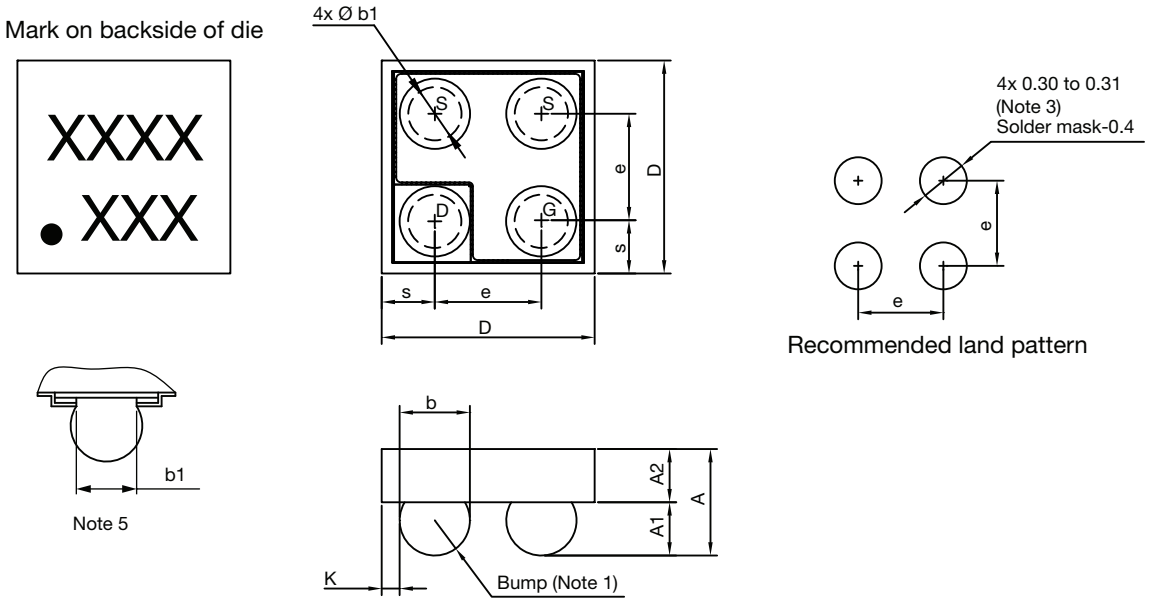
MICRO FOOT®: 4-Bumps
(1 mm x 1 mm, 0.5 mm Pitch, 0.286 mm Bump Height)



Notes

1. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser mark on the backside surface of die.
5. “b1” is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.458	0.504	0.550	0.0180	0.0198	0.0217
A1	0.214	0.250	0.286	0.0084	0.0098	0.0113
A2	0.244	0.254	0.264	0.0096	0.0100	0.0104
b	0.297	0.330	0.363	0.0117	0.0130	0.0143
b1		0.250			0.0098	
e		0.500			0.0197	
s	0.210	0.230	0.250	0.0083	0.0091	0.0096
D	0.920	0.960	1.000	0.0362	0.0378	0.0394
K	0.029	0.065	0.102	0.0011	0.0026	0.0040

Note

- Use millimeters as the primary measurement.

ECN: T15-0176-Rev. A, 27-Apr-15
DWG: 6039

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