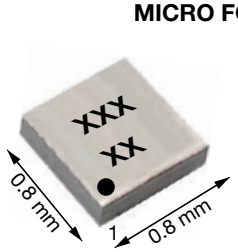
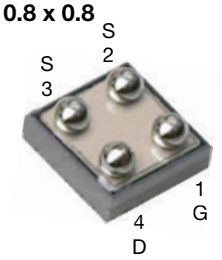
# P-Channel 20 V (D-S) MOSFET

**MICRO FOOT® 0.8 x 0.8**




Backside View




Bump Side View

## FEATURES

- TrenchFET® Gen III p-channel power MOSFET
- Compact 0.8 mm x 0.8 mm outline area
- Low 0.4 mm max. profile
- $R_{DS(on)}$ rating at $V_{GS}$ = -1.5 V
- Typical ESD protection: 1900 V HBM
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

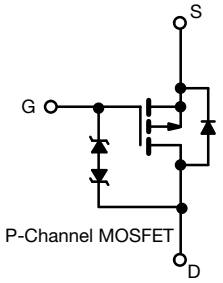
Pb-free

RoHS COMPLIANT

HALOGEN FREE

## APPLICATIONS

- Load switch
- Power management in battery-operated, mobile, and wearable devices




| PRODUCT SUMMARY | |
|---|---|
| $V_{DS}$ (V) | -20 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = -4.5 V | 0.095 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = -2.5 V | 0.120 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = -1.8 V | 0.200 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = -1.5 V | 0.335 |
| $Q_g$ typ. (nC) | 6.6 |
| $I_D$ (A) | -2.7 [a] |
| Configuration | Single |

| ORDERING INFORMATION | |
|---|---|
| Package | MICRO FOOT |
| Lead (Pb)-free and halogen-free | Si8823EDB-T2-E1 |

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25 °C, unless otherwise noted)

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DS}$ | -20 | V |
| Gate-source voltage | | $V_{GS}$ | ± 8 | |
| Continuous drain current ($T_J$ = 150 °C) | $T_A$ = 25 °C | $I_D$ | -2.7 [a] | A |
| | $T_A$ = 70 °C | | -2.1 [a] | |
| | $T_A$ = 25 °C | | -1.9 [b] | |
| | $T_A$ = 70 °C | | -1.5 [b] | |
| Pulsed drain current (t = 100 µs) | | $I_{DM}$ | -15 | |
| Continuous source-drain diode current | $T_A$ = 25 °C | $I_S$ | -0.7 [a] | |
| | $T_A$ = 70 °C | | -0.4 [b] | |
| Maximum power dissipation | $T_A$ = 25 °C | $P_D$ | 0.9 [a] | W |
| | $T_A$ = 70 °C | | 0.6 [a] | |
| | $T_A$ = 25 °C | | 0.5 [b] | |
| | $T_A$ = 70 °C | | 0.3 [b] | |
| Operating junction and storage temperature range | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Package reflow conditions [c] | | VPR | 260 | |
| | | IR / convection | | |

**THERMAL RESISTANCE RATINGS**

| PARAMETER | | SYMBOL | TYPICAL | MAXIMUM | UNIT |
|---|---|---|---|---|---|
| Maximum junction-to-ambient [a, f] | t = 5 s | $R_{thJA}$ | 105 | 135 | °C/W |
| Maximum junction-to-ambient [b, g] | | | 200 | 260 | |

**Notes**

a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
c. Refer to IPC / JEDEC® (J-STD-020), no manual or hand soldering.
d. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.
e. Based on $T_A$ = 25 °C.
f. Maximum under steady state conditions is 185 °C/W.
g. Maximum under steady state conditions is 330 °C/W.

| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = -250 µA | -20 | - | - | V |
| $V_{DS}$ temperature coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = -250 µA | - | -12.5 | - | mV/°C |
| $V_{GS(th)}$ temperature coefficient | $\Delta V_{GS(th)}/T_J$ | | - | 2.3 | - | |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$ , $I_D$ = -250 µA | -0.4 | - | -0.8 | V |
| Gate-source leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 4.5 V | - | - | ± 0.5 | µA |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = ± 8 V | - | - | ± 5 | |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ = -20 V, $V_{GS}$ = 0 V | - | - | -1 | |
| | | $V_{DS}$ = -20 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | - | - | -10 | |
| On-state drain current [a] | $I_{D(on)}$ | $V_{DS} \geq$ -5 V, $V_{GS}$ = -4.5 V | -5 | - | - | A |
| Drain-source on-state resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = -4.5 V, $I_D$ = -1 A | - | 0.077 | 0.095 | Ω |
| | | $V_{GS}$ = -2.5 V, $I_D$ = -1 A | - | 0.100 | 0.120 | |
| | | $V_{GS}$ = -1.8 V, $I_D$ = -0.5 A | - | 0.137 | 0.185 | |
| | | $V_{GS}$ = -1.5 V, $I_D$ = -0.5 A | - | 0.200 | 0.335 | |
| Forward transconductance [a] | $g_{fs}$ | $V_{DS}$ = -5 V, $I_D$ = -1 A | - | 6 | - | S |
| **Dynamic [b]** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{DS}$ = -10 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 580 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 165 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 75 | - | |
| Total gate charge | $Q_g$ | $V_{DS}$ = -10 V, $V_{GS}$ = -8 V, $I_D$ = -1 A | - | 11 | 17 | nC |
| | | $V_{DS}$ = -10 V, $V_{GS}$ = -4.5 V, $I_D$ = -1 A | - | 6.6 | 10 | |
| Gate-source charge | $Q_{gs}$ | $V_{DS}$ = -10 V, $V_{GS}$ = -4.5 V, $I_D$ = -1 A | - | 1 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 1.5 | - | |
| Gate resistance | $R_g$ | f = 1 MHz | - | 20 | - | Ω |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = -10 V, $R_L$ = 10 Ω, $I_D \cong$ -1 A, $V_{GEN}$ = -4.5 V, $R_g$ = 1 Ω | - | 16 | 30 | ns |
| Rise time | $t_r$ | | - | 30 | 60 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 60 | 120 | |
| Fall time | $t_f$ | | - | 40 | 80 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = -10 V, $R_L$ = 10 Ω, $I_D \cong$ -1 A, $V_{GEN}$ = -8 V, $R_g$ = 1 Ω | - | 7 | 15 | |
| Rise time | $t_r$ | | - | 20 | 40 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 75 | 150 | |
| Fall time | $t_f$ | | - | 35 | 70 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous source-drain diode current | $I_S$ | $T_A$ = 25 °C | - | - | -0.7 | A |
| Pulse diode forward current | $I_{SM}$ | | - | - | -15 | |
| Body diode voltage | $V_{SD}$ | $I_S$ = -1 A, $V_{GS}$ = 0 V | - | -0.8 | -1.2 | V |
| Body diode reverse recovery time | $t_{rr}$ | $I_F$ = -1 A, dI/dt = 100 A/µs, $T_J$ = 25 °C | - | 20 | 40 | ns |
| Body diode reverse recovery charge | $Q_{rr}$ | | - | 7 | 15 | nC |
| Reverse recovery fall time | $t_a$ | | - | 12.5 | - | ns |
| Reverse recovery rise time | $t_b$ | | - | 7.5 | - | |

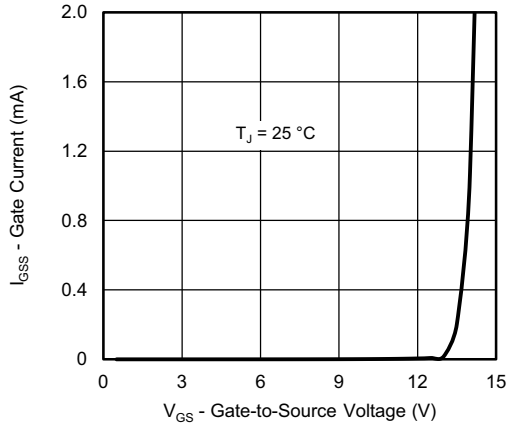
**Notes**

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

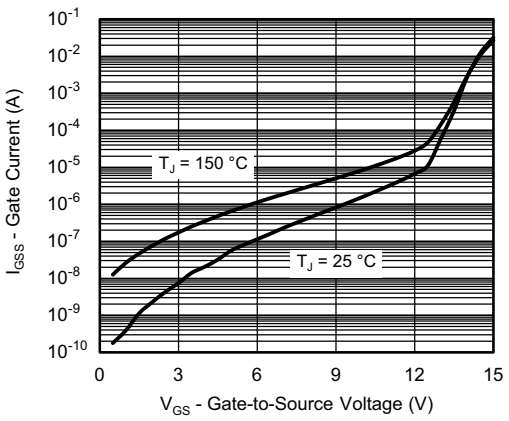
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

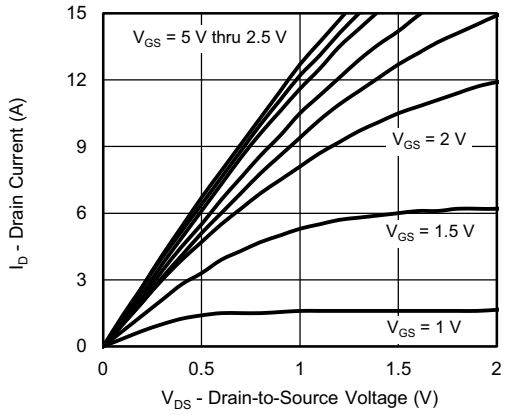
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



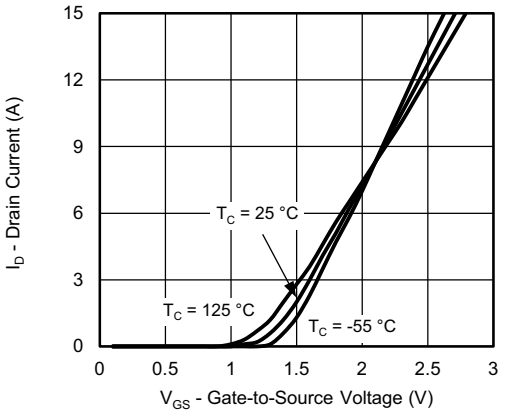

**Gate-Current vs. Gate-Source Voltage**



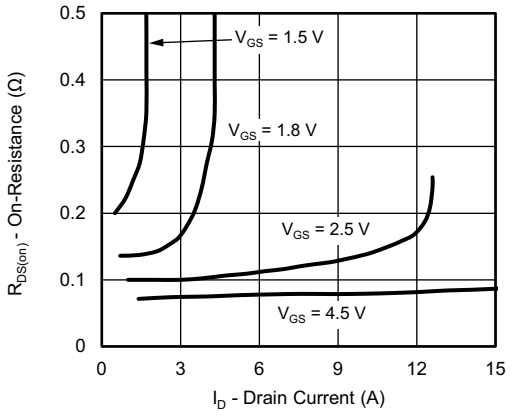

**Gate-Current vs. Gate-Source Voltage**



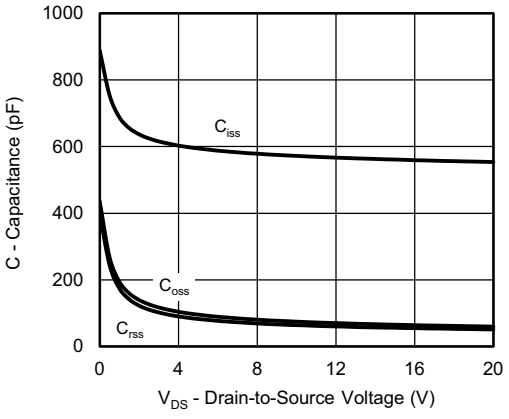

**Output Characteristics**




**Transfer Characteristics**

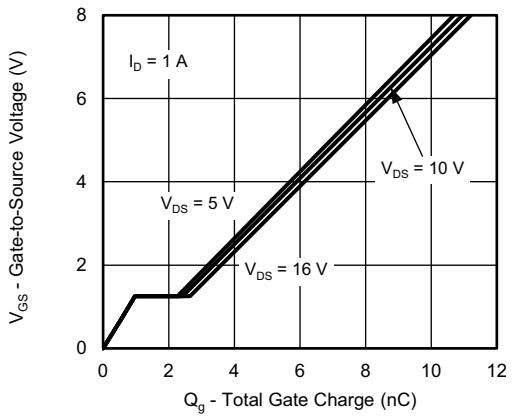



**On-Resistance vs. Drain Current and Gate Voltage**

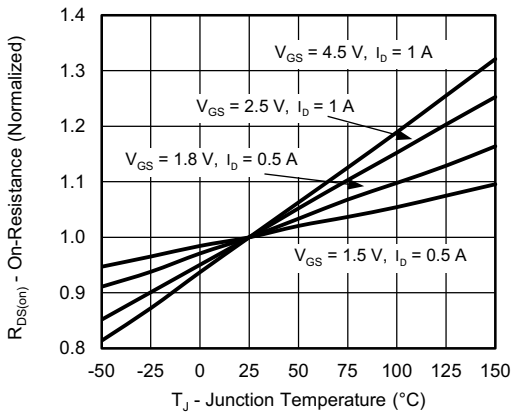



**Capacitance**

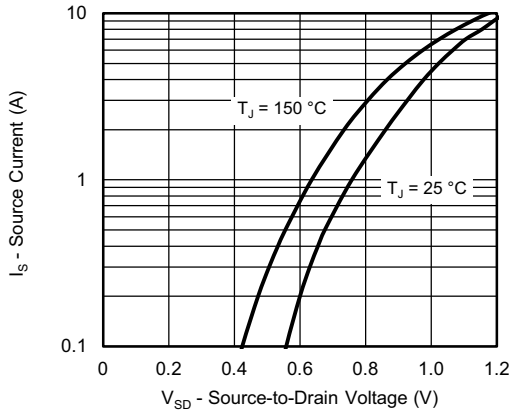
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



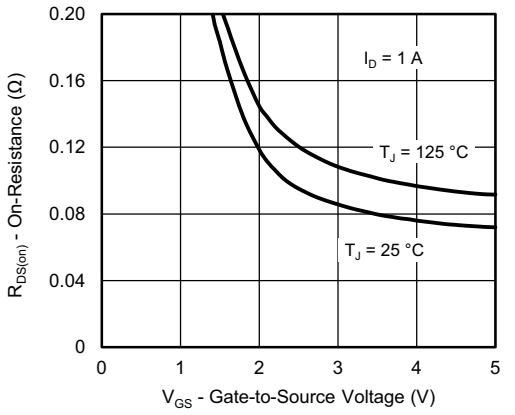

**Gate Charge**



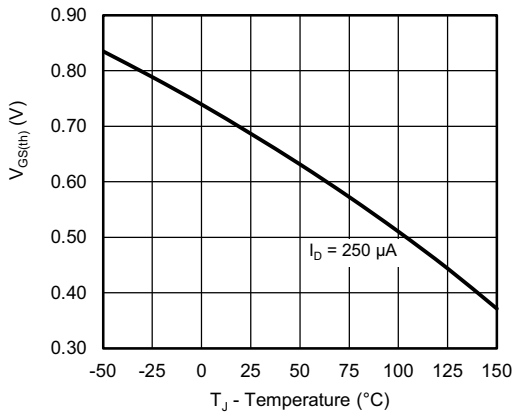

**On-Resistance vs. Junction Temperature**



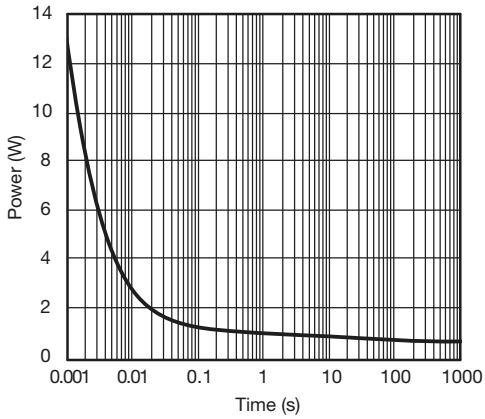

**Source-Drain Diode Forward Voltage**




**On-Resistance vs. Gate-to-Source Voltage**

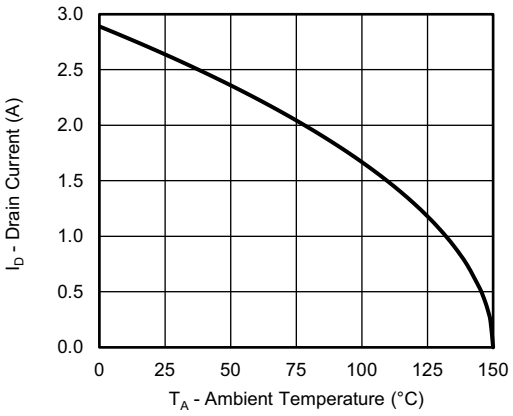



**Threshold Voltage**

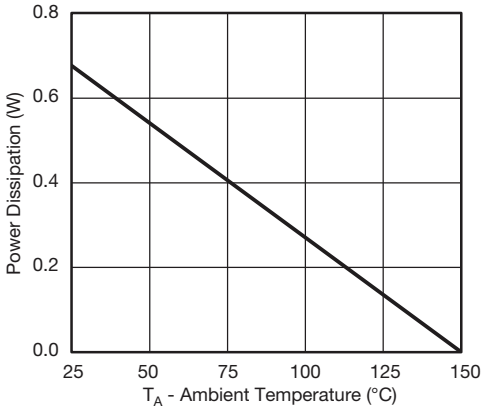



**Single Pulse Power, Junction-to-Ambient**

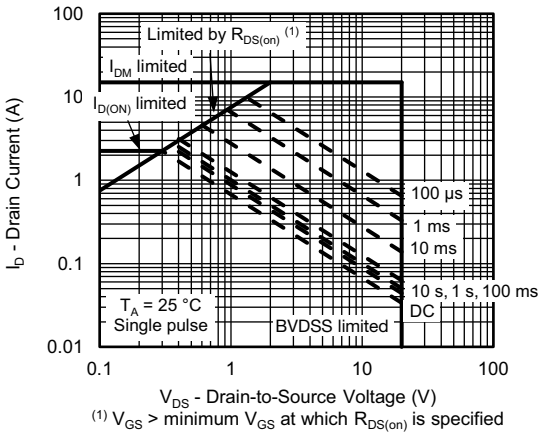
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)




**Current Derating [a]**




**Power, Junction-to-Ambient**

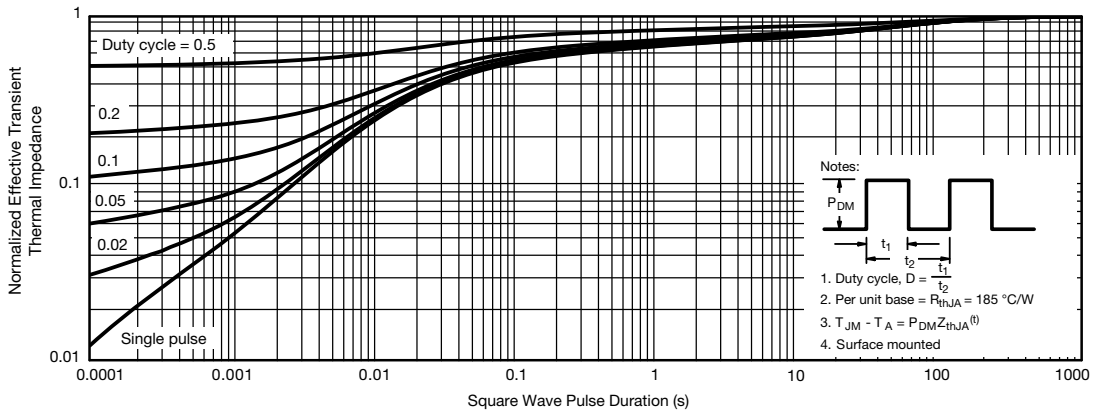



**Safe Operating Area, Junction-to-Ambient**

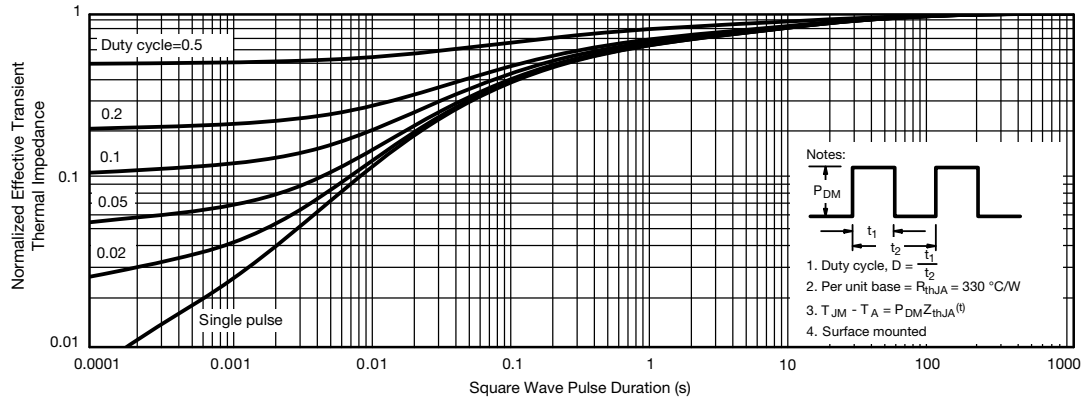
**Note**

a. The power dissipation $P_D$ is based on $T_J$ max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with maximum copper)**




**Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with minimum copper)**

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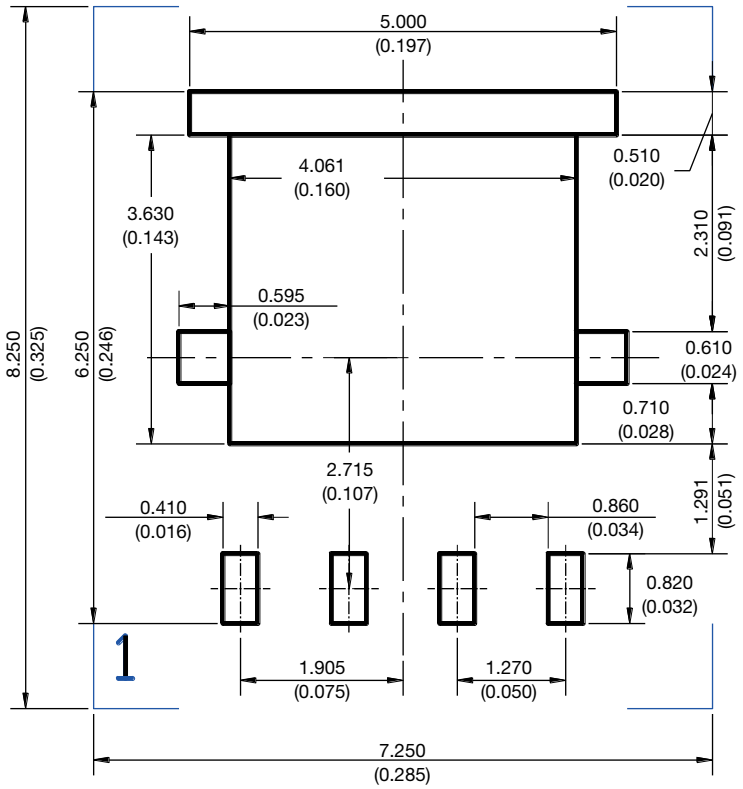
## RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE




Recommended Minimum Pads
Dimensions in mm (inches)

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