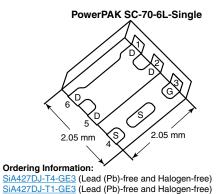


P-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY									
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)						
	0.016 at V _{GS} = - 4.5 V	- 12 ^a							
- 8	0.0215 at V _{GS} = - 2.5 V	- 12 ^a							
	0.026 at V _{GS} = - 1.8 V	- 12 ^a	30 nC						
	0.032 at V _{GS} = - 1.5 V	- 12 ^a							
	0.095 at V _{GS} = - 1.2 V	- 3							



FEATURES

- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_a Tested
- Material categorization:

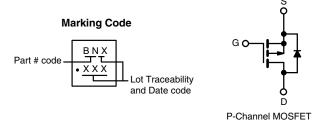
For definitions of compliance please see www.vishay.com/doc?99912



COMPLIANT HALOGEN **FREE**

APPLICATIONS

Load Switch, for 1.2 V Power Line for Portable and Handheld Devices



ABSOLUTE MAXIMUM RATINGS	(1A = 25 C, unit		.64)	
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	- 8	V
Gate-Source Voltage		V _{GS}	± 5	v
	T _C = 25 °C		- 12 ^a	
Continuous Dunin Comment (T. 150 °C)	T _C = 70 °C		- 12 ^a	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	- 12 ^{a, b, c}	
	T _A = 70 °C		- 9.9 ^{b, c}	Α
Pulsed Drain Current	•	I _{DM}	- 50	
Ocaliana Come Desira Diada Ocana	T _C = 25 °C		- 12 ^a	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 2.9 ^{b, c}	
	T _C = 25 °C		19	
Maximum Dawar Dissination	T _C = 70 °C	Б	12	14/
Maximum Power Dissipation	T _A = 25 °C	P _D	3.5 ^{b, c}	W
	T _A = 70 °C		2.2 ^{b, c}	
Operating Junction and Storage Temperature Ra	ange	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature	e) ^{d, e}	Ü	260	

THERMAL RESISTANCE RATINGS									
Parameter		Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	28	36	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.3	6.5] 5/**				

Notes:

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 80 °C/W.

Document Number: 66711 S12-1141-Rev. C, 21-May-12 For more information please contact: pmostechsupport@vishay.com

SiA427DJ

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	V _{GS} = 0, I _D = - 250 μA	- 8			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 A		- 5.8		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		2.4			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	- 0.35		- 0.8	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 5 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -8 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	μΑ	
Zero Gate Voltage Drain Current		V_{DS} = -8 V, V_{GS} = 0 V, T_{J} = 55 °C			- 10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le$ - 5 V, $V_{GS} =$ - 4.5 V	- 10			Α	
		$V_{GS} = -4.5 \text{ V}, I_D = -8.2 \text{ A}$		0.013	0.016	Ω	
		$V_{GS} = -2.5 \text{ V}, I_D = -7.2 \text{ A}$		0.018	0.0215		
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -1.8 \text{ V}, I_D = -6.6 \text{ A}$		0.021	0.026		
		V _{GS} = - 1.5 V, I _D = - 1 A	0.032				
		V _{GS} = - 1.2 V, I _D = - 1 A	0.037 0.095				
Forward Transconductance ^a	g _{fs}	V _{DS} = - 4 V, I _D = - 8.2 A		37		S	
Dynamic ^b							
Input Capacitance	C _{iss}			2300		pF	
Output Capacitance	C _{oss}	$V_{DS} = -4 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		735			
Reverse Transfer Capacitance	C _{rss}			690			
Total Cata Charge	Qg	V _{DS} = - 4 V, V _{GS} = - 5 V, I _D = - 10 A		33	50	nC	
Total Gate Charge				30	45		
Gate-Source Charge	Q_{gs}	$V_{DS} = -4 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -10 \text{ A}$		3			
Gate-Drain Charge	Q_{gd}			6.6			
Gate Resistance	R_g	f = 1 MHz	2	9	18	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	t _r	$V_{DD} = -4 \text{ V}, R_{L} = 0.4 \Omega$		20	30	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 9.8 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		70	105		
Fall Time	t _f			40	60	1	
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 12	٨	
Pulse Diode Forward Current	I _{SM}				- 50	Α	
Body Diode Voltage	V_{SD}	$I_S = -9.8 \text{ A}, V_{GS} = 0$		- 0.8	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			40	80	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	1 00 A 41/44 100 A/45 T 05 00		12	25	nC	
Reverse Recovery Fall Time	t _a	$I_F = -9.8 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		14			
Reverse Recovery Rise Time	t _b			26		ns	

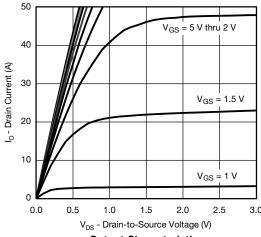
Notes:

- a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

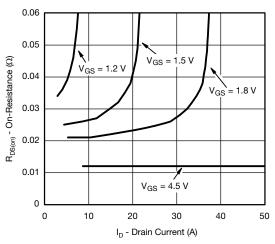
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



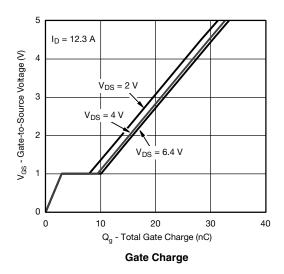
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

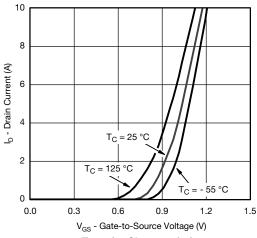


Output Characteristics

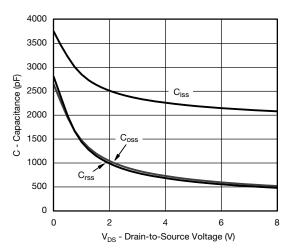


On-Resistance vs. Drain Current and Gate Voltage

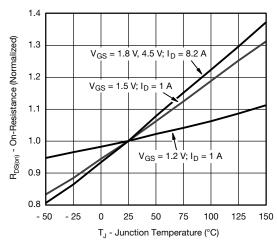




Transfer Characteristics



Capacitance

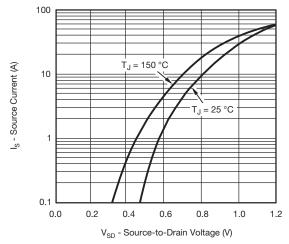


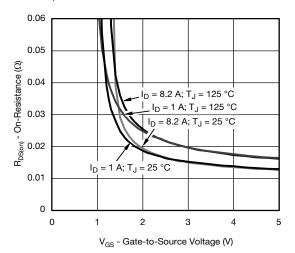
On-Resistance vs. Junction Temperature

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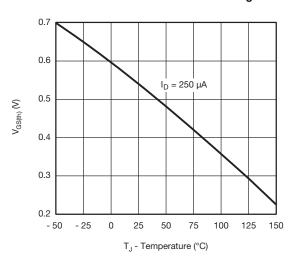
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

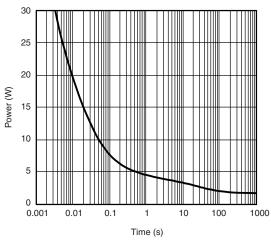




Soure-Drain Diode Forward Voltage

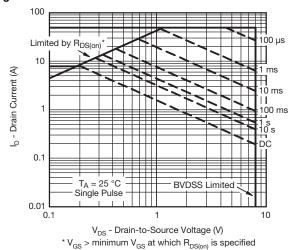
On-Resistance vs. Gate-to-Source Voltage





Threshold Voltage

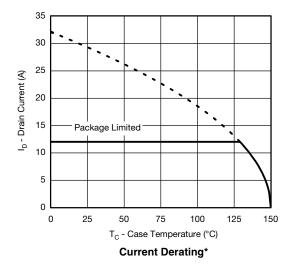
Single Pulse Power, Junction-to-Ambient

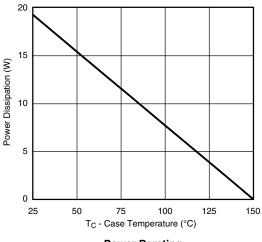


Safe Operating Area, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





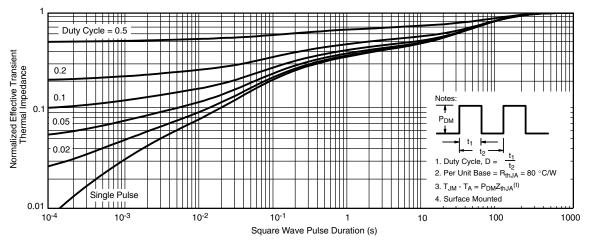
Power Derating

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

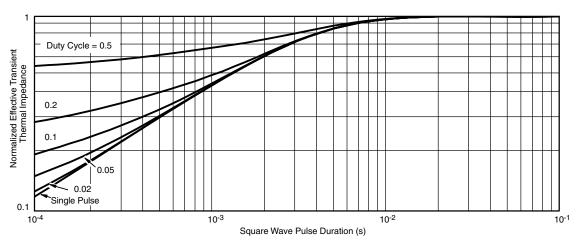
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



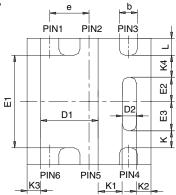
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?66711.





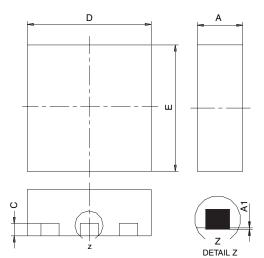
PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

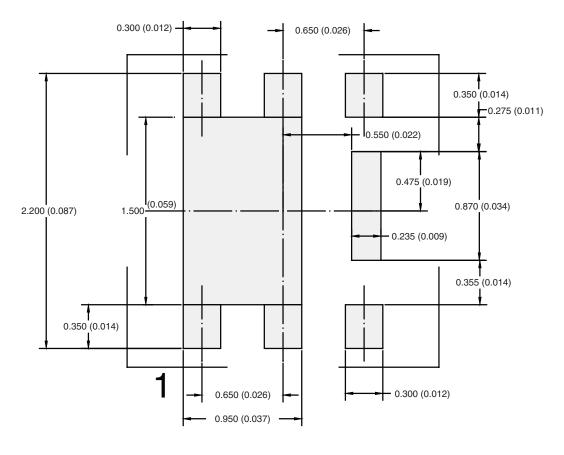
	SINGLE PAD						DUAL PAD					
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A 1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC		
K		0.275 TYP	١		0.011 TYP		0.275 TYP			0.011 TYP		
K1		0.400 TYP	١		0.016 TYP		0.320 TYP			0.013 TYP		
K2		0.240 TYP 0.009 TYP			0.252 TYP			0.010 TYP				
К3		0.225 TYP	1	0.009 TYP								
K4		0.355 TYP		0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
Т							0.05	0.10	0.15	0.002	0.004	0.006
FCN: C-07431 - Bey C. 06-Aug-07												

DWG: 5934

Document Number: 73001 06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

Return to Index

ATTLICATION NOT



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Revision: 02-Oct-12 Document Number: 91000

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