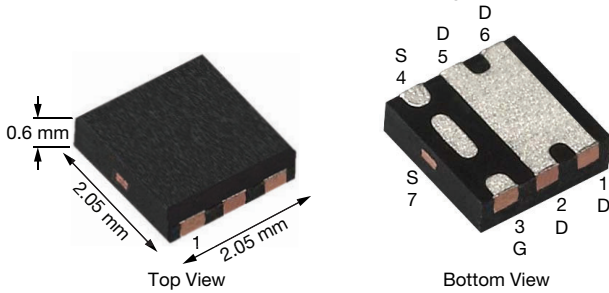


## P-Channel 20 V (D-S) MOSFET

Thin PowerPAK® SC-70-6L Single



Marking code: BP

PRODUCT SUMMARY	
$V_{DS}$ (V)	-20
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -4.5$ V	0.0205
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -2.5$ V	0.0270
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -1.8$ V	0.0360
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = -1.5$ V	0.0600
$Q_g$ typ. (nC)	24.5
$I_D$ (A) <sup>a</sup>	-12
Configuration	Single

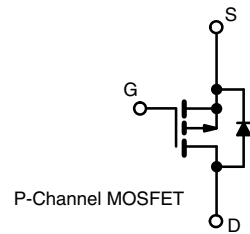
### FEATURES

- TrenchFET® power MOSFET
- New thermally enhanced PowerPAK® SC-70 package
  - Small footprint area
  - Ultra-thin 0.6 mm height
  - Low on-resistance
- 100 %  $R_g$  tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### APPLICATIONS

- Load switch and charger switch for portable devices
- DC/DC converter



ORDERING INFORMATION	
Package	Thin PowerPAK SC-70
Lead (Pb)-free and halogen-free	SiA429DJT-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	-20	V
Gate-source voltage	$V_{GS}$	$\pm 8$	V
Continuous drain current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	-12 <sup>a</sup>
		$T_C = 70$ °C	-12 <sup>a</sup>
		$T_A = 25$ °C	-10.6 <sup>b, c</sup>
		$T_A = 70$ °C	-8.5 <sup>b, c</sup>
Pulsed drain current ( $t = 300$ $\mu$ s)	$I_{DM}$	-30	A
Continuous source-drain diode current	$I_S$	$T_C = 25$ °C	-12 <sup>a</sup>
		$T_A = 25$ °C	-2.9 <sup>b, c</sup>
Maximum power dissipation	$P_D$	$T_C = 25$ °C	19
		$T_C = 70$ °C	12
		$T_A = 25$ °C	3.5 <sup>b, c</sup>
		$T_A = 70$ °C	2.2 <sup>b, c</sup>
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>d, e</sup>		260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b, f</sup>	$t \leq 5$ s	$R_{thJA}$	28	36	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	5.3	6.5	

### Notes

- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 5$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 80 °C/W



<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = -250\text{ }\mu\text{A}$	-	-12	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$		-	2.7	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-0.4	-	-1	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	-	-	-10	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$	-20	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -6\text{ A}$	-	0.0170	0.0205	$\Omega$
		$V_{GS} = -2.5\text{ V}, I_D = -2\text{ A}$	-	0.0220	0.0270	
		$V_{GS} = -1.8\text{ V}, I_D = -2\text{ A}$	-	0.0290	0.0360	
		$V_{GS} = -1.5\text{ V}, I_D = -1\text{ A}$	-	0.0380	0.0600	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -10\text{ V}, I_D = -6\text{ A}$	-	30	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{iss}$	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	1750	-	pF
Output capacitance	$C_{oss}$		-	270	-	
Reverse transfer capacitance	$C_{rss}$		-	240	-	
Total gate charge	$Q_g$	$V_{DS} = -10\text{ V}, V_{GS} = -8\text{ V}, I_D = -10\text{ A}$	-	41	62	nC
Gate-source charge	$Q_{gs}$	$V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -10\text{ A}$	-	24.5	37	
Gate-drain charge	$Q_{gd}$		-	2.4	-	
Gate resistance	$R_g$		-	6.7	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	1.3	6.3	13	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1.2\text{ }\Omega$ $I_D \cong -8.5\text{ A}, V_{GEN} = -4.5\text{ V}, R_g = 1\text{ }\Omega$	-	22	35	ns
Rise time	$t_r$		-	25	40	
Turn-off delay time	$t_{d(off)}$		-	70	105	
Fall time	$t_f$		-	25	40	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = -10\text{ V}, R_L = 1.2\text{ }\Omega$ $I_D \cong -8.5\text{ A}, V_{GEN} = -8\text{ V}, R_g = 1\text{ }\Omega$	-	10	15	
Rise time	$t_r$		-	10	15	
Turn-off delay time	$t_{d(off)}$		-	80	120	
Fall time	$t_f$		-	25	40	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	-12	A
Pulse diode forward current	$I_{SM}$		-	-	-30	
Body diode voltage	$V_{SD}$	$I_S = -8.5\text{ A}, V_{GS} = 0\text{ V}$	-	-0.8	-1.2	V
Body diode reverse recovery time	$t_{rr}$	$I_F = -8.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $T_J = 25\text{ }^\circ\text{C}$	-	35	60	ns
Body diode reverse recovery charge	$Q_{rr}$		-	18	30	nC
Reverse recovery fall time	$t_a$		-	13	-	ns
Reverse recovery rise time	$t_b$		-	22	-	

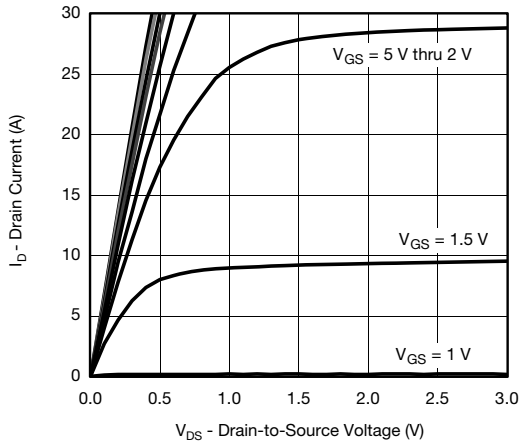
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing

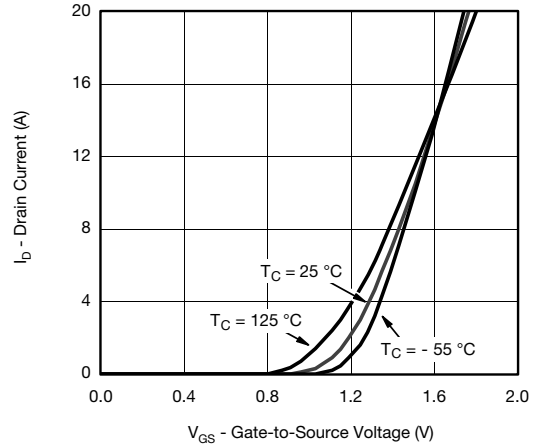
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



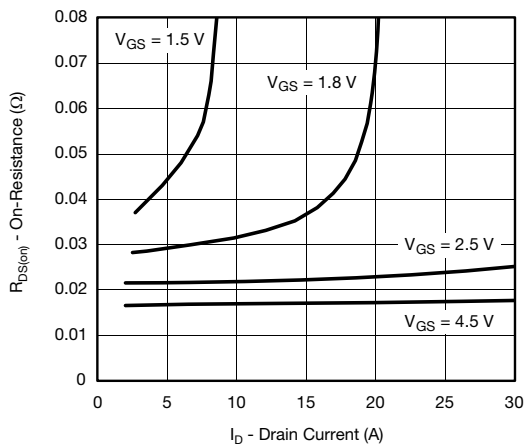
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



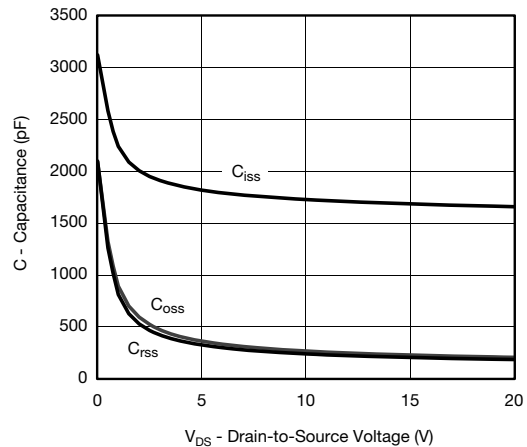
**Output Characteristics**



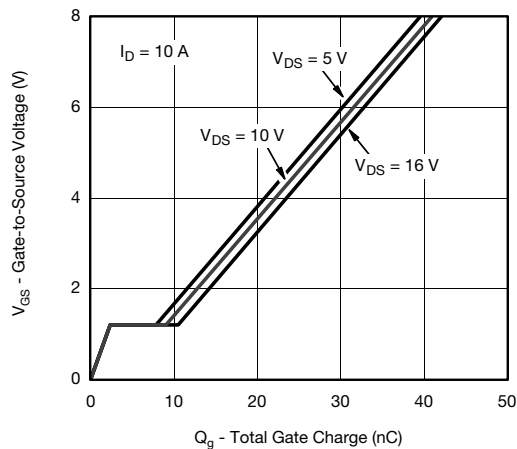
**Transfer Characteristics**



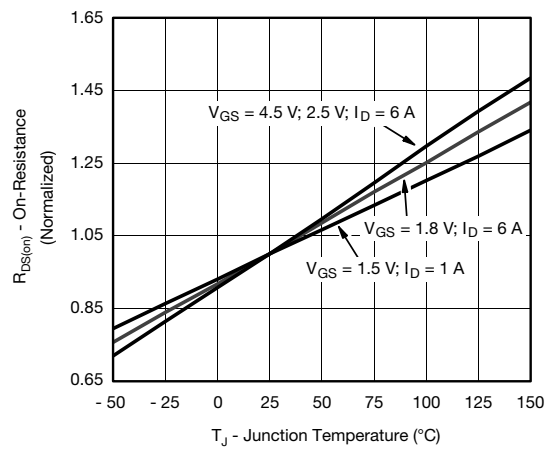
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



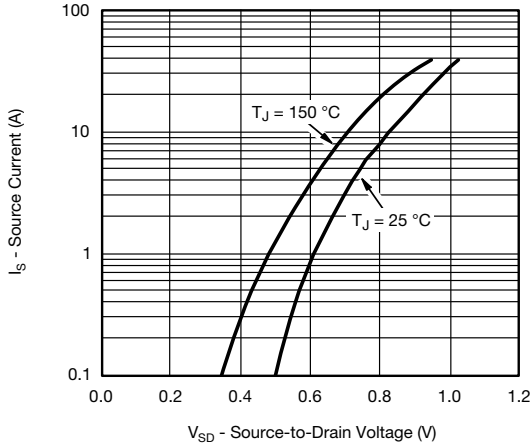
**Gate Charge**



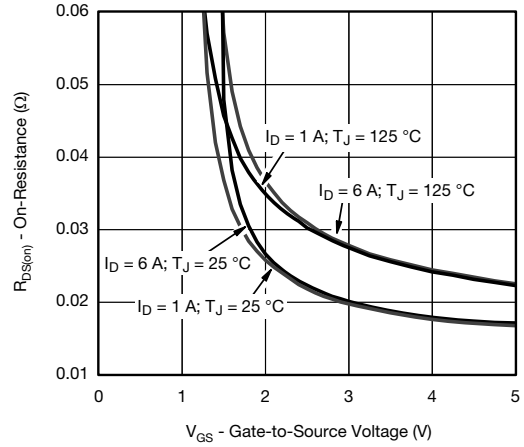
**On-Resistance vs. Junction Temperature**



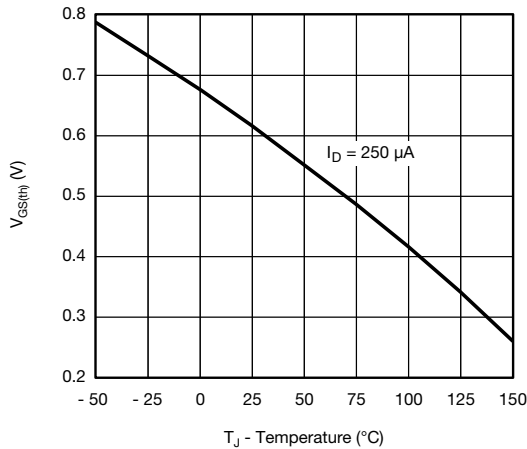
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



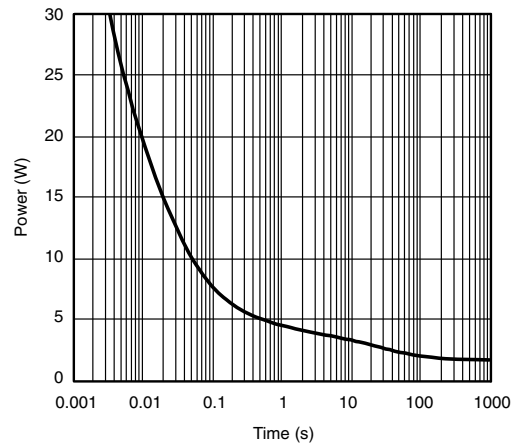
**Source-Drain Diode Forward Voltage**



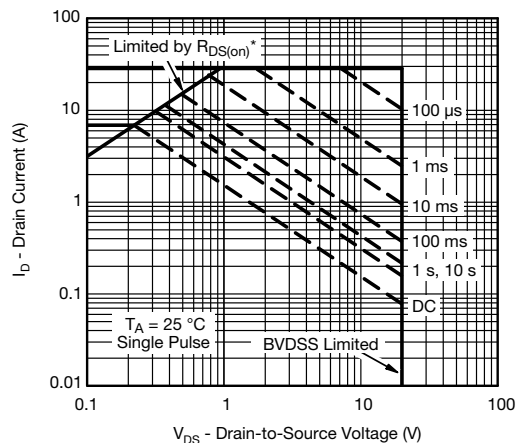
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



**Single Pulse Power, Junction-to-Ambient**

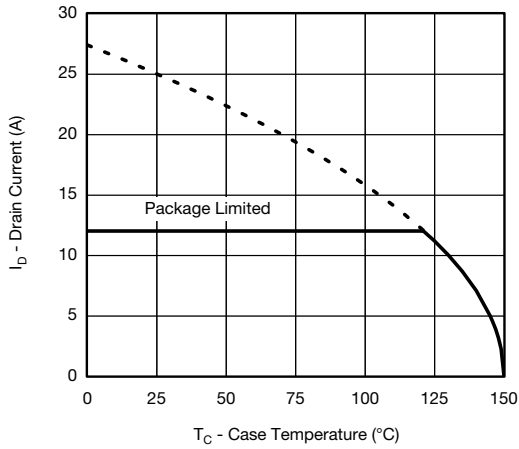


\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

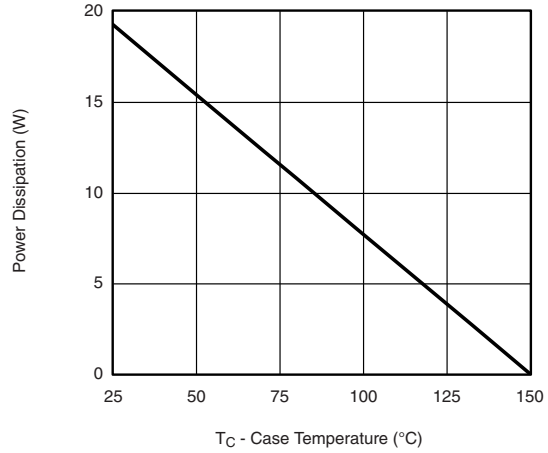
**Safe Operating Area, Junction-to-Ambient**



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



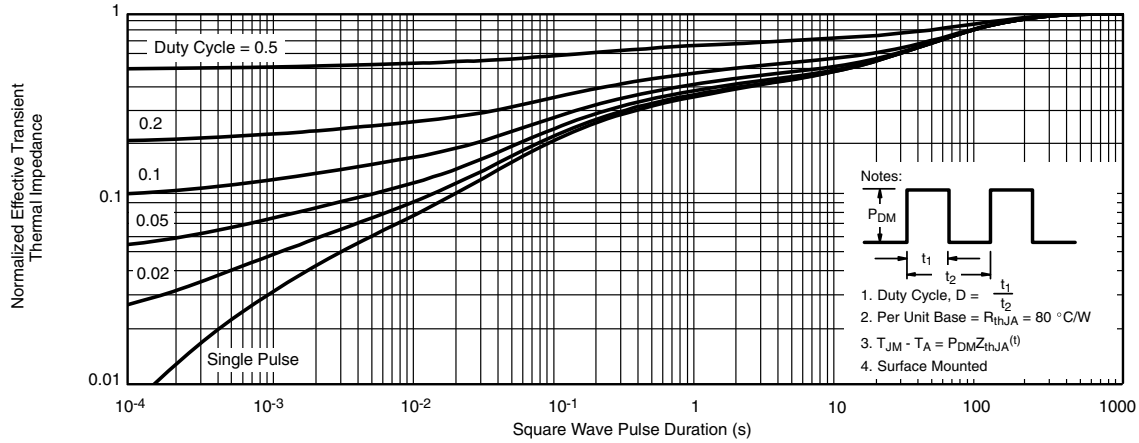
**Power Derating**

**Note**

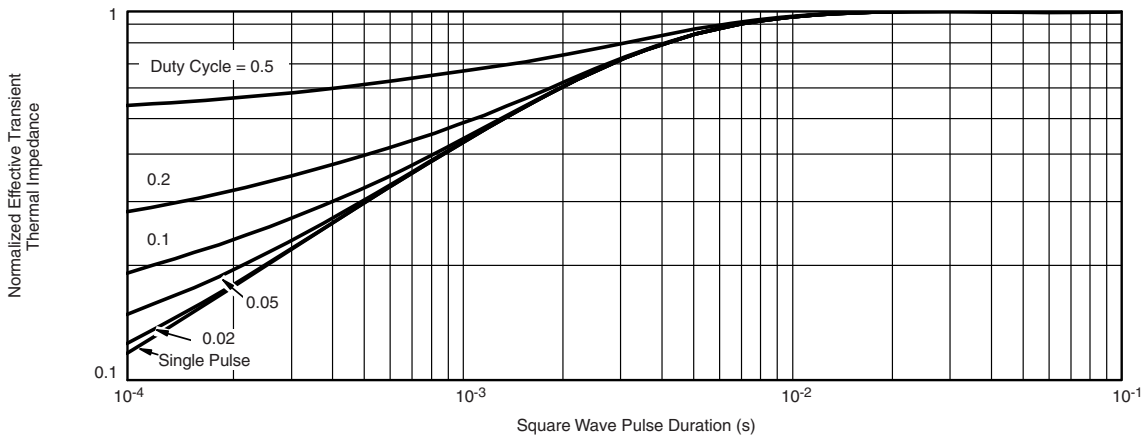
- a. The power dissipation  $P_D$  is based on  $T_J \text{ max.} = 150 \text{ }^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

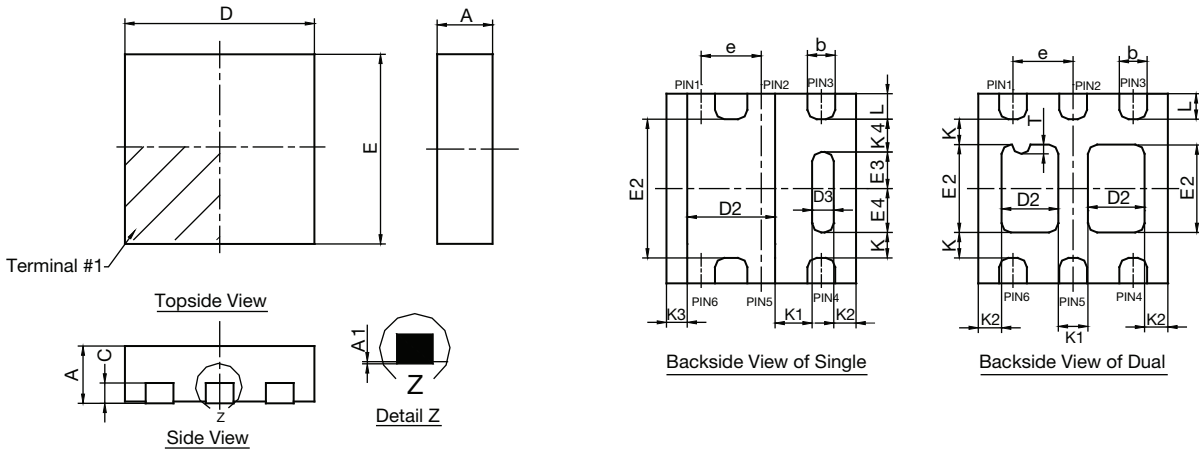


**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for silicon technology and package reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?67038](http://www.vishay.com/ppg?67038).



### Case Outline for PowerPAK® SC70T



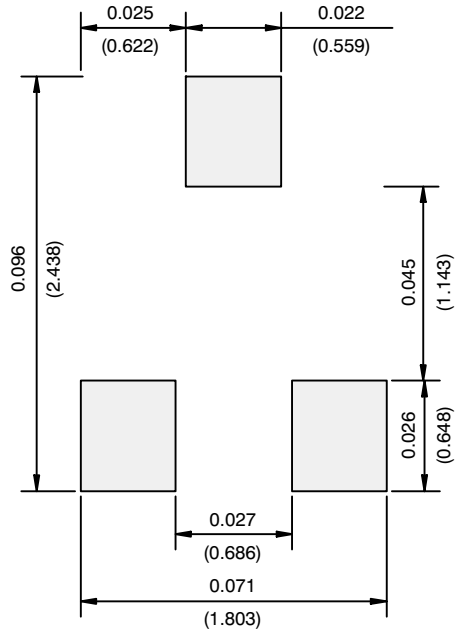
DIM.	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.525	0.60	0.65	0.0206	0.024	0.026	0.525	0.60	0.65	0.0206	0.024	0.026
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D2	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D3	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E2	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E3	0.345	0.395	0.445	0.014	0.016	0.018						
E4	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP.			0.011 TYP.			0.275 TYP.			0.011 TYP.		
K1	0.400 TYP.			0.016 TYP.			0.320 TYP.			0.013 TYP.		
K2	0.240 TYP.			0.009 TYP.			0.252 TYP.			0.010 TYP.		
K3	0.225 TYP.			0.009 TYP.								
K4	0.355 TYP.			0.014 TYP.								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C12-0160-Rev. B, 05-Mar-12  
DWG: 5994

**Notes**

1. All dimensions are in millimeter. Millimeters will govern.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating

## RECOMMENDED MINIMUM PADS FOR SC-70: 3-Lead

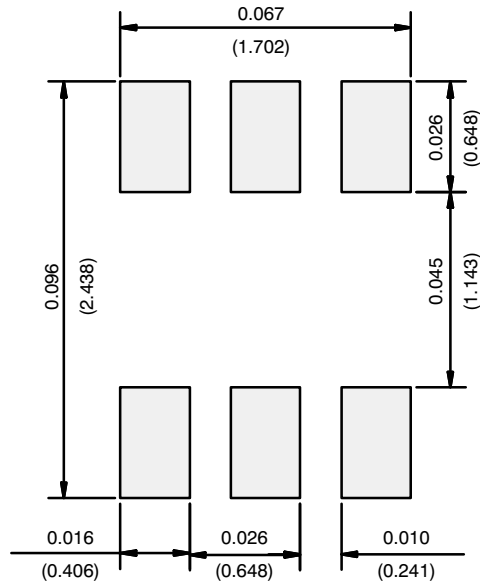


Recommended Minimum Pads  
Dimensions in Inches/(mm)

[Return to Index](#)



## RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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