

## N-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY									
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>b, c</sup>	Q <sub>g</sub> (Typ.)						
20	$0.0135$ at $V_{GS} = 10 \text{ V}$	12 <sup>a</sup>	5.3 nC						
	0.0185 at V <sub>GS</sub> = 4.5 V	10.8	5.3 NC						

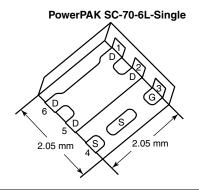
#### **FEATURES**

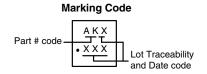
- TrenchFET® Power MOSFET
- Thermally Enhanced PowerPAK® SC-70 Package
  - Small Footprint Area
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912



#### **APPLICATIONS**

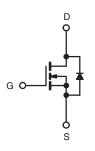
· Load Switch





#### Ordering Information:

SiA430DJ-T1-GE3 (Lead (Pb)-free and Halogen-free) SiA430DJ-T4-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> (T <sub>A</sub> = 25 °C, unless otherwise noted)								
Parameter		Symbol	Limit	Unit				
Drain-Source Voltage		$V_{DS}$	20	V				
Gate-Source Voltage		$V_{GS}$	± 20	v				
	T <sub>C</sub> = 25 °C		12 <sup>a</sup>					
Continuous Drain Current (T <sub>.1</sub> = 150 °C)	T <sub>C</sub> = 70 °C	I <sub>D</sub>	12 <sup>a</sup>					
Continuous Brain Current (1) = 130 C)	T <sub>A</sub> = 25 °C		12 <sup>a, b, c</sup>					
	T <sub>A</sub> = 70 °C		10.1 <sup>b, c</sup>	A				
Pulsed Drain Current	•	I <sub>DM</sub>	40					
Continuous Source-Drain Diode Current	T <sub>C</sub> = 25 °C		12 <sup>a</sup>					
Continuous Source-Diam Diode Current	T <sub>A</sub> = 25 °C	I <sub>S</sub>	2.9 <sup>b, c</sup>					
	T <sub>C</sub> = 25 °C		19.2					
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	12.3	w				
Maximum Fower Dissipation	T <sub>A</sub> = 25 °C	1 'D	3.5 <sup>b, c</sup>	VV				
	T <sub>A</sub> = 70 °C		2.2 <sup>b, c</sup>					
Operating Junction and Storage Temperature	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C					
Soldering Recommendations (Peak Tempera	ature) <sup>d, e</sup>		260					

THERMAL RESISTANCE RATINGS										
Parameter		Symbol	Typical	Maximum	Unit					
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 5 s	$R_{thJA}$	28	36	°C/W					
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	5.3	6.5	0, 44					

#### Notes:

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board.
- c. t = 5 s.
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under steady state conditions is 80 °C/W.

Document Number: 68685 S13-0116-Rev. B, 21-Jan-13 For technical questions, contact: pmostechsupport@vishav.com



<b>SPECIFICATIONS</b> ( $T_J = 25  ^{\circ}C$ , Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static	Symbol	rest conditions	IVIIII.	тур.	wax.	Onic
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$			24		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 5.6		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	1	0.0	3	V
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
	-033	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			10	μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α
_	_	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7 A		0.0108	0.0135	Ω
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$		0.0146	0.0185	
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 7 A		16		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>			800		рF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		200		
Reverse Transfer Capacitance	C <sub>rss</sub>			90		
Total Cata Charga	$Q_g$	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 12 \text{ A}$		12	18	nC
Total Gate Charge				5.3	9	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 12 \text{ A}$		2		
Gate-Drain Charge	$Q_gd$			1.4		
Gate Resistance	$R_g$	f = 1 MHz		2.5		Ω
Turn-On Delay Time	t <sub>d(on)</sub>			16	25	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 1 $\Omega$		10	15	ns
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_a = 1 \Omega$		15	25	
Fall Time	t <sub>f</sub>	.b = 107, 1 GEN 1, 1.g		10	15	
Turn-On Delay Time	t <sub>d(on)</sub>			10	15	
Rise Time	t <sub>r</sub>	$V_{DD} = 10 \text{ V}, R_{I} = 1 \Omega$		8	15	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_q = 1 \Omega$		17	30	
Fall Time	t <sub>f</sub>			8	15	
<b>Drain-Source Body Diode Characteristic</b>	s			•		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			12	Α
Pulse Diode Forward Current	biode Forward Current I <sub>SM</sub>				40	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 5 A, V <sub>GS</sub> = 0 V		0.8	1.2	٧
Body Diode Reverse Recovery Time	t <sub>rr</sub>			18	30	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 10 A, dl/dt = 100 A/μs, T <sub>.I</sub> = 25 °C		7	15	nC
Reverse Recovery Fall Time	t <sub>a</sub>	1 = 10 Λ, αι/αι = 100 Α/μs, 1 J = 25 C		8		no
Reverse Recovery Rise Time	t <sub>b</sub>			10		ns

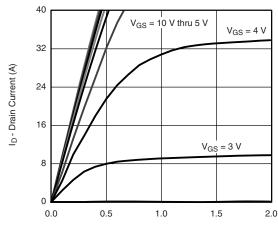
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

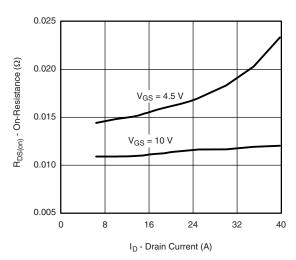


### TYPICAL CHARACTERISTIC (25 °C, unless otherwise noted)

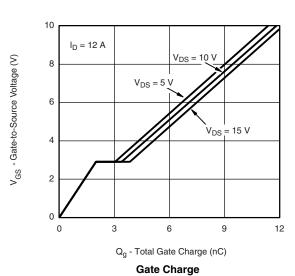


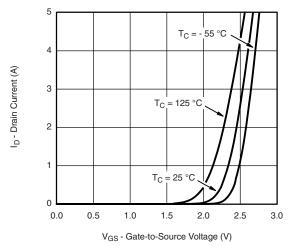
V<sub>DS</sub> - Drain-to-Source Voltage (V)

#### **Output Characteristics**

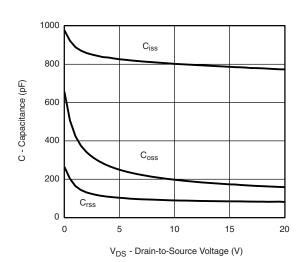


#### On-Resistance vs. Drain Current and Gate Voltage

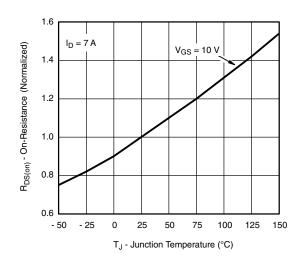




**Transfer Characteristics** 

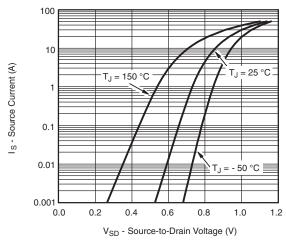


Capacitance

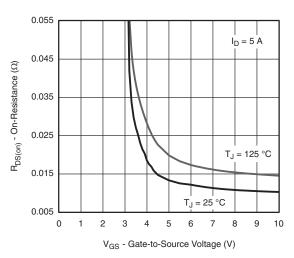


On-Resistance vs. Junction Temperature

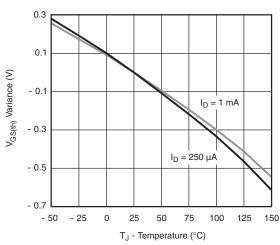
### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



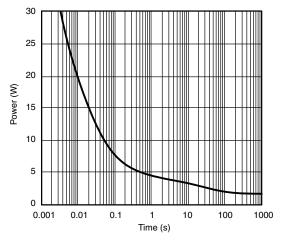
Source-Drain Diode Forward Voltage



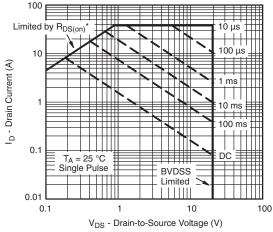
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power (Junction-to-Ambient)



 $^{\star}$   $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

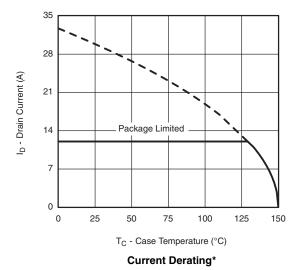
Safe Operating Area, Junction-to-Ambient

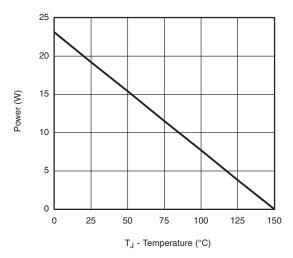






### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

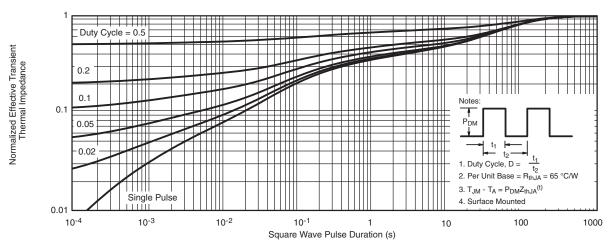




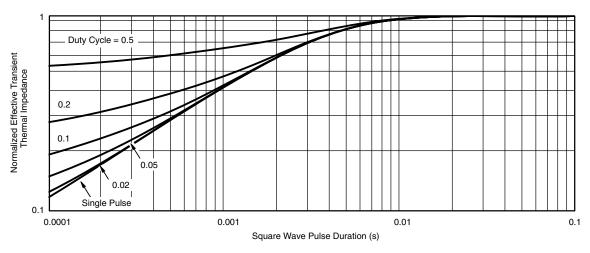
**Power Derating** 

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Ambient



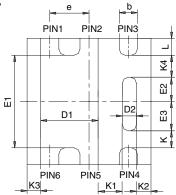
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68685.





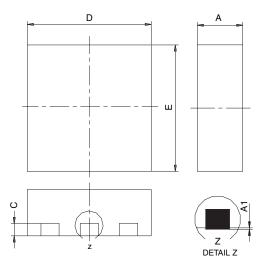
## PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
   Package outline exclusive of mold flash and metal burr
   Package outline inclusive of plating

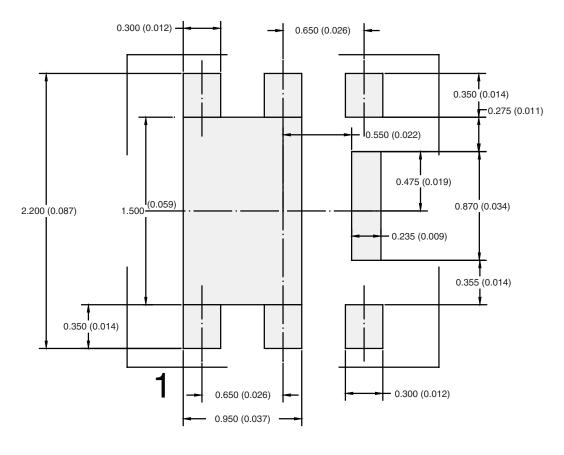
	SINGLE PAD						DUAL PAD						
DIM	MILLIMETERS			INCHES			MILLIMETERS			INCHES			
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032	
<b>A</b> 1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002	
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015	
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010	
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028	
D2	0.135	0.235	0.335	0.005	0.009	0.013							
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085	
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041	
E2	0.345	0.395	0.445	0.014	0.016	0.018							
E3	0.425	0.475	0.525	0.017	0.019	0.021							
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC			
K		0.275 TYP	١		0.011 TYP		0.275 TYP			0.011 TYP			
K1		0.400 TYP	١		0.016 TYP			0.320 TYP			0.013 TYP		
K2		0.240 TYP	0 TYP 0.009 TYP			0.252 TYP			0.010 TYP				
К3		0.225 TYP	1	0.009 TYP									
K4		0.355 TYP		0.014 TYP									
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015	
Т							0.05	0.10	0.15	0.002	0.004	0.006	
FCN: C-07431 – Bey C. 06-Aug-07													

DWG: 5934

Document Number: 73001 06-Aug-07



## RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

Return to Index

ATTLICATION NOT



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Revision: 02-Oct-12 Document Number: 91000

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IPS70R2K0CEAKMA1 BUK954R8-60E DMN3404LQ-7 NTE6400 SQJ402EP-T1-GE3 2SK2614(TE16L1,Q) 2N7002KW-FAI

DMN1017UCP3-7 EFC2J004NUZTDG ECH8691-TL-W FCAB21350L1 P85W28HP2F-7071 DMN1053UCP4-7 NTE221 NTE2384

NTE2903 NTE2941 NTE2945 NTE2946 NTE2960 NTE2967 NTE2969 NTE2976 NTE455 NTE6400A NTE2910 NTE2916 NTE2956

NTE2911 TK10A80W,S4X(S SSM6P69NU,LF DMP22D4UFO-7B