New Product



SiA431DJ Vishay Siliconix

P-Channel 20-V (D-S) MOSFET

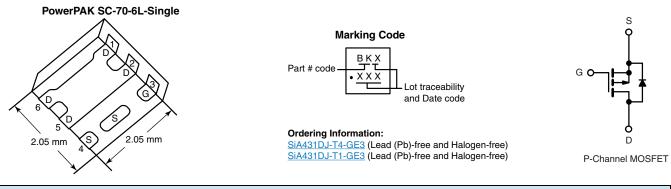
| PRODUCT SUMMARY | | | | |
|---------------------|--|--------------------|-----------------------|--|
| V _{DS} (V) | R_{DS(on)} (Ω) | I _D (A) | Q _g (Typ.) | |
| - 20 | 0.025 at V _{GS} = - 4.5 V | - 12 ^a | | |
| | 0.031 at V _{GS} = - 2.5 V | - 12 ^a | 24 nC | |
| | 0.041 at V _{GS} = - 1.8 V | - 12 ^a | 24 110 | |
| | 0.070 at V _{GS} = - 1.5 V | - 4 | | |

FEATURES

- TrenchFET[®] Power MOSFET New Thermally Enhanced PowerPAK[®]
 - SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g Tested
- FREE Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

Load Switch, PA Switch and Battery Switch for Portable Devices



| Parameter | | Symbol | Limit | Unit | |
|--|--|-----------------------------------|--|------|--|
| Drain-Source Voltage | | V _{DS} | - 20 | V | |
| Gate-Source Voltage | | V _{GS} | ± 8 | | |
| Continuous Drain Current (T _J = 150 °C) | $T_{C} = 25 \text{ °C}$ $T_{C} = 70 \text{ °C}$ | I _D | - 12 ^a - 12 ^a | | |
| | T _A = 25 °C T _A = 70 °C | | - 9.6 ^{b, c} - 7.7 ^{b, c} - 30 | A | |
| Pulsed Drain Current | | DM | | | |
| Continuous Source-Drain Diode Current | $T_{C} = 25 \text{ °C}$ $T_{A} = 25 \text{ °C}$ | I _S | - 12 ^a - 2.9 ^{b, c} | | |
| | T _C = 25 °C | | 19 | | |
| Maximum Power Dissipation | T _C = 70 °C | P _D | 12 | w | |
| | $T_A = 25 \degree C$ $T_A = 70 \degree C$ | | 3.5 ^{b, c} 2.2 ^{b, c} | _ | |
| Operating Junction and Storage Temperature Range | | T _J , T _{stg} | - 55 to 150 | | |
| Soldering Recommendations (Peak Temperature) ^{d, e} | | - 5.9 | 260 | | |

| THERMAL RESISTANCE RATINGS | | | | | | |
|---|--------------|-------------------|---------|---------|------|--|
| Parameter | | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient ^{b, f} | t ≤ 5 s | R _{thJA} | 28 | 36 | °C/W | |
| Maximum Junction-to-Case (Drain) | Steady State | R _{thJC} | 5.3 | 6.5 | 0/11 | |

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. See Solder Profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 80 °C/W.

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COMPLIANT

HALOGEN

SiA431DJ

Vishay Siliconix



| Parameter | Symbol | Test Conditions | Min. | Тур. | Max. | Unit | |
|--|--|---|-------|--------|--------|-------|--|
| Static | - | | | | | | |
| Drain-Source Breakdown Voltage | V _{DS} | $V_{GS} = 0 V, I_D = -250 \mu A$ | - 20 | | | V | |
| V _{DS} Temperature Coefficient | $\Delta V_{DS}/T_{J}$ | L 050 A | | - 14.5 | | mV/°C | |
| V _{GS(th)} Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | I _D = - 250 μΑ | | 2.7 | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | $V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$ | - 0.4 | | - 0.85 | V | |
| Gate-Source Leakage | I _{GSS} | $V_{DS} = 0 V, V_{GS} = \pm 8 V$ | | | ± 100 | nA | |
| Zero Gate Voltage Drain Current | | V _{DS} = - 20 V, V _{GS} = 0 V | | | - 1 | μΑ | |
| | IDSS | $V_{DS} = -20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$ | | | - 10 | | |
| On-State Drain Current ^a | I _{D(on)} | $V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V | - 20 | | | Α | |
| Drain-Source On-State Resistance ^a | _() | V _{GS} = - 4.5 V, I _D = - 6.5 A | | 0.020 | 0.025 | + | |
| | | V _{GS} = - 2.5 V, I _D = - 5.8 A | | 0.025 | 0.031 | Ω | |
| | R _{DS(on)} | V _{GS} = - 1.8 V, I _D = - 2.5 A | | 0.034 | 0.041 | | |
| | | V _{GS} = - 1.5 V, I _D = - 1.5 A | | 0.045 | 0.070 | | |
| Forward Transconductance ^a | 9 _{fs} | V _{DS} = - 10 V, I _D = - 6.5 A | | 31 | | S | |
| Dynamic ^b | | | | | | | |
| Input Capacitance | C _{iss} | | | 1700 | | pF | |
| Output Capacitance | C _{oss} | V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz | | 230 | | | |
| Reverse Transfer Capacitance | C _{rss} | | | 205 | | | |
| T + 1 0 + 0 | $\begin{array}{c} V_{DS} = -10 \text{ V}, \text{ V}_{GS} = -8 \text{ V}, \text{ I}_{D} = -9.6 \text{ A} \\ \hline \\ Q_{gs} & \text{ V}_{DS} = -10 \text{ V}, \text{ V}_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -9.6 \text{ A} \end{array}$ | $V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_{D} = -9.6 \text{ A}$ | | 40 | 60 | - | |
| Total Gate Charge | | | | 24 | 36 | - | |
| Gate-Source Charge | | | 2.4 | | nC | | |
| Gate-Drain Charge | Q _{gd} | | | 6.5 | | | |
| Gate Resistance | Rg | f = 1 MHz | 1.3 | 6.3 | 13 | Ω | |
| Turn-On Delay Time | t _{d(on)} | | | 22 | 35 | | |
| Rise Time | t _r | V_{DD} = - 10 V, R_L = 1.3 Ω | | 25 | 40 | - | |
| Turn-Off Delay Time | t _{d(off)} | $\text{I}_\text{D}\cong$ - 7.7 A, V_GEN = - 4.5 V, R_g = 1 Ω | | 65 | 100 | | |
| Fall Time | t _f | | | 25 | 40 | | |
| Turn-On Delay Time | t _{d(on)} | | | 10 | 15 | ns | |
| Rise Time | t _r | V_{DD} = - 10 V, R_L = 1.3 Ω | | 10 | 15 | - | |
| Turn-Off Delay Time | t _{d(off)} | ${ m I}_{ m D}\cong$ - 7.7 A, ${ m V}_{ m GEN}$ = - 8 V, ${ m R}_{ m g}$ = 1 Ω | | 65 | 100 | | |
| Fall Time | t _f | | | 20 | 30 | | |
| Drain-Source Body Diode Characterist | ics | | | | | | |
| Continuous Source-Drain Diode Current | ا _S | $T_{\rm C} = 25 \ ^{\circ}{\rm C}$ | | | - 12 | Α | |
| Pulse Diode Forward Current | I _{SM} | | | | - 30 | | |
| Body Diode Voltage | V _{SD} | I _S = - 7.7 A, V _{GS} = 0 V | | - 0.8 | - 1.2 | V | |
| Body Diode Reverse Recovery Time t _{rr} | | | | 35 | 60 | ns | |
| Body Diode Reverse Recovery Charge | Q _{rr} | L = 77.0 dt/dt = 100.0 / tra T = 05.00 | | 21 | 35 | nC | |
| Reverse Recovery Fall Time | ta | | | 20 | | | |
| Reverse Recovery Rise Time | t _b | | | 15 | | ns | |

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

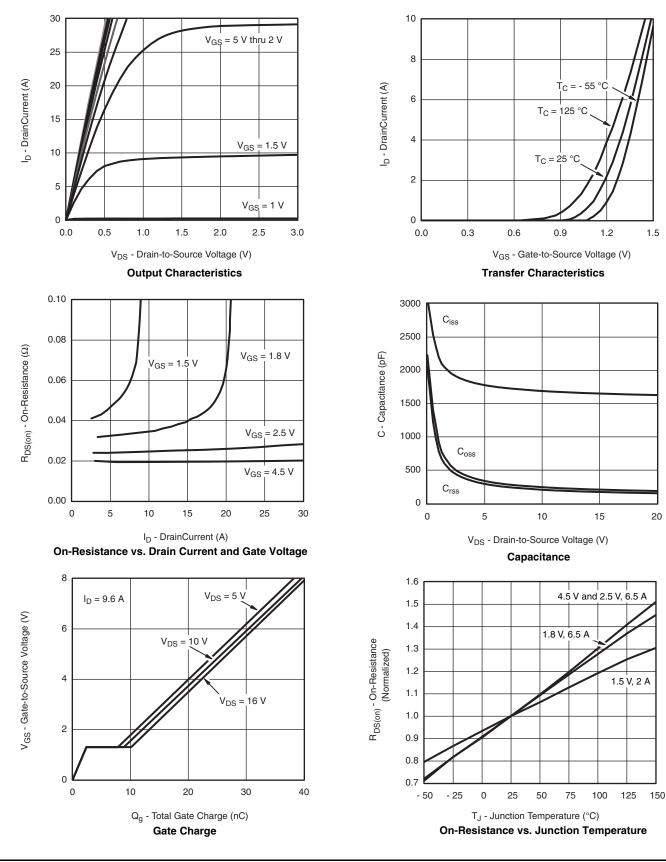
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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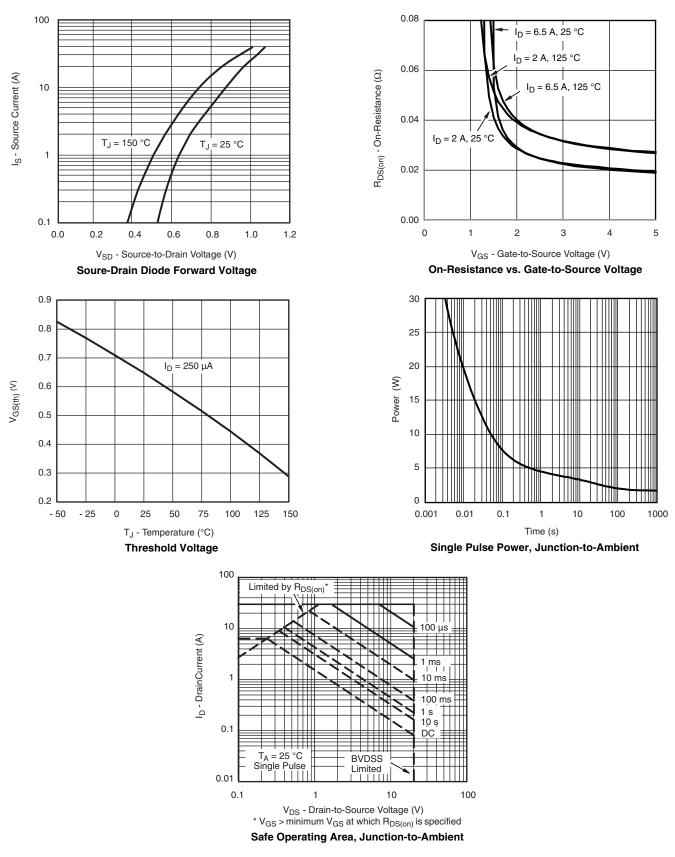
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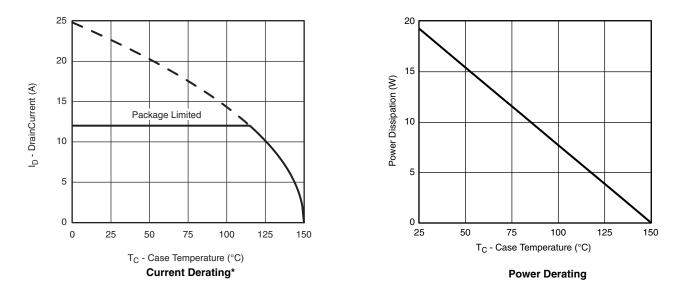
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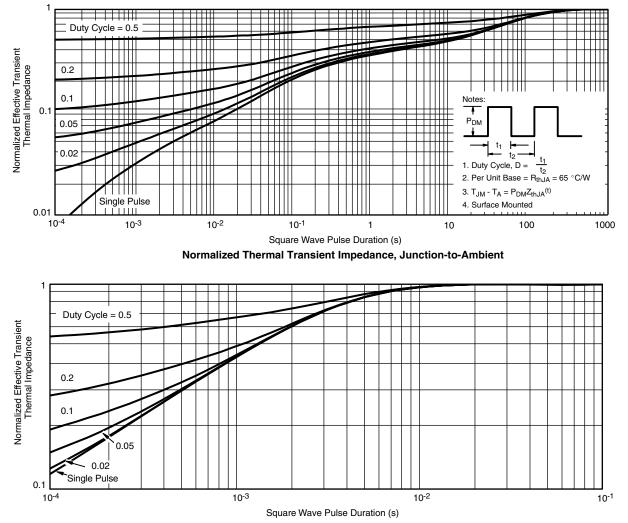
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg265267.

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PowerPAK[®] SC70-6L

VISHA

b PIN2 PIN1 PIN3 _ ₹



b

PIN3

__ ₿

PIN2

PIN1

¥

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¹



RECOMMENDED PAD LAYOUT FOR PowerPAK[®] SC70-6L Single



Dimensions in mm/(Inches)

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Vishay

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