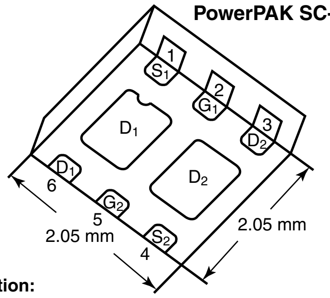
Dual N-Channel 30 V (D-S) MOSFET

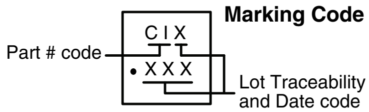
PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω) MAX.	I_D (A)	Q_g (TYP.)
30	0.064 at V_{GS} = 4.5 V	4.5[a]	3.5 nC
	0.072 at V_{GS} = 3.0 V	4.5[a]	
	0.080 at V_{GS} = 2.5 V	4.5[a]	
	0.400 at V_{GS} = 1.8 V	0.2	

PowerPAK SC-70-6 Dual



Ordering Information:
SiA922EDJ-T1-GE3 (Lead (Pb)-free and Halogen-free)



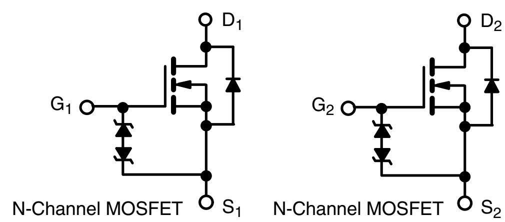
FEATURES

- TrenchFET® Power MOSFET
- Thermally enhanced PowerPAK® SC-70 package
  - Small footprint area
  - Low on-resistance
- Typical ESD protection: 1500 V (HBM)
- 100 % R_g tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Portable devices such as smart phones, tablet PCs and mobile computing
  - Load switch
  - DC/DC converter
  - Power management



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		**SYMBOL**	**LIMIT**	**UNIT**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current (T_J = 150 °C)	T_C = 25 °C	I_D	4.5[a]	A
	T_C = 70 °C		4.5[a]	
	T_A = 25 °C		4.4[b, c]	
	T_A = 70 °C		3.5[b, c]	
Pulsed Drain Current (t = 300 μs)		I_{DM}	15	
Continuous Source-Drain Diode Current	T_C = 25 °C	I_S	4.5[a]	
	T_A = 25 °C		1.6[b, c]	
Maximum Power Dissipation	T_C = 25 °C	P_D	7.8	W
	T_C = 70 °C		5	
	T_A = 25 °C		1.9[b, c]	
	T_A = 70 °C		1.2[b, c]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature)[d,e]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYPICAL**	**MAXIMUM**	**UNIT**
Maximum Junction-to-Ambient[b, f]	t ≤ 5 s	R_{thJA}	52	65	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	12.5	16	

Notes

a. Package limited.
b. Surface mounted on 1" x 1" FR4 board.
c. t = 5 s.
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under steady state condition is 110 °C/W.

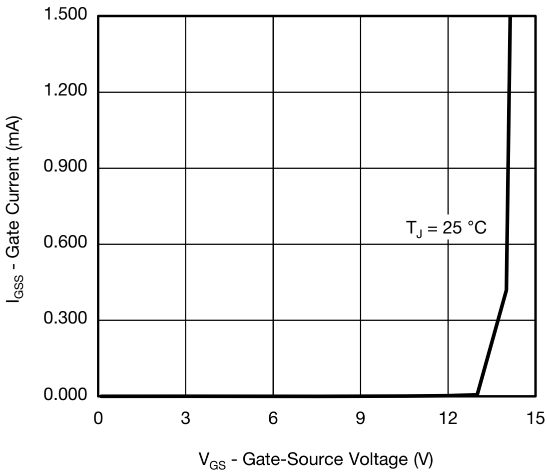
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA		34		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-3.3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	0.6		1.4	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 4.5 V			± 0.5	μA
		V_{DS} = 0 V, V_{GS} = ± 12 V			± 20	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			1	
		V_{DS} = 30 V, V_{GS} = 0 V, T_J = 55 °C			10	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq$ 5 V, V_{GS} = 4.5 V	10			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 3 A		0.049	0.064	Ω
		V_{GS} = 3.0 V, I_D = 3 A		0.055	0.072	
		V_{GS} = 2.5 V, I_D = 1 A		0.060	0.080	
		V_{GS} = 1.8 V, I_D = 0.2 A		0.100	0.400	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 3 A		13		S
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 4 A		7.5	12	nC
		V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 4 A		3.5	5.5	
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			0.7		
Gate Resistance	R_g	f = 1 MHz	0.6	3.3	6.6	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 4.7 Ω $I_D \cong$ 3.2 A, V_{GEN} = 4.5 V, R_g = 1 Ω		20	40	ns
Rise Time	t_r			60	120	
Turn-Off DelayTime	$t_{d(off)}$			25	50	
Fall Time	t_f			45	90	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 4.7 Ω $I_D \cong$ 3.2 A, V_{GEN} = 10 V, R_g = 1 Ω		1.5	5	
Rise Time	t_r			30	60	
Turn-Off DelayTime	$t_{d(off)}$			15	30	
Fall Time	t_f			50	100	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C			3.9	A
Pulse Diode Forward Current	I_{SM}				15	
Body Diode Voltage	V_{SD}	I_S = 3.2 A, V_{GS} = 0 V		0.87	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = 3.2 A, dI/dt = 100 A/μs, T_J = 25 °C		10	20	ns
Body Diode Reverse Recovery Charge	Q_{rr}			4	10	nC
Reverse Recovery Fall Time	t_a			5.3		ns
Reverse Recovery Rise Time	t_b			4.6		

Notes

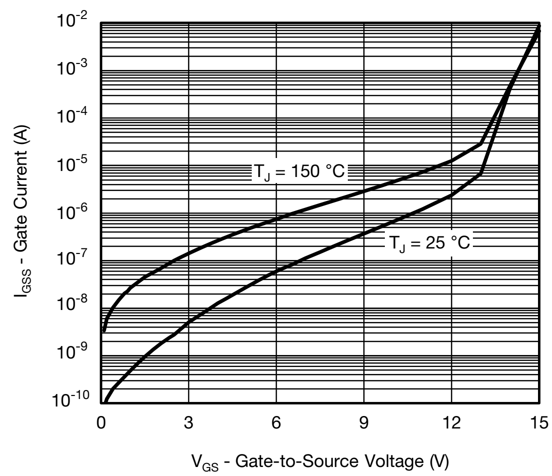
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

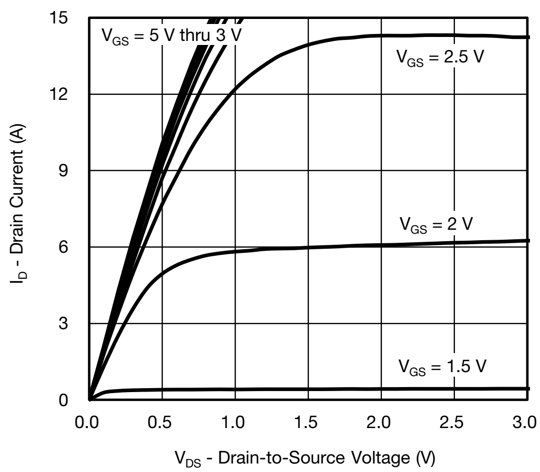
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



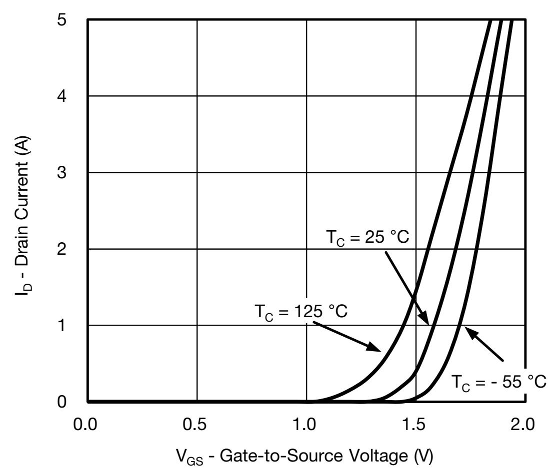
Gate Current vs. Gate-Source Voltage



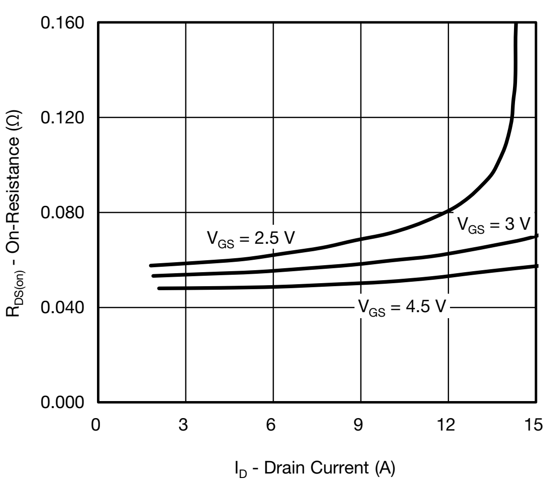
Gate Current vs. Gate-Source Voltage



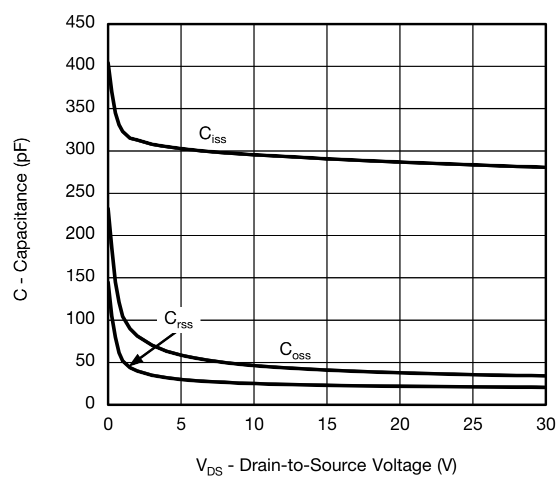
Output Characteristics



Transfer Characteristics

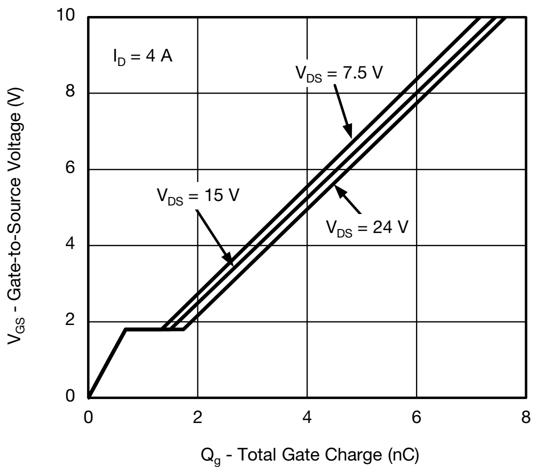


On-Resistance vs. Drain Current and Gate Voltage

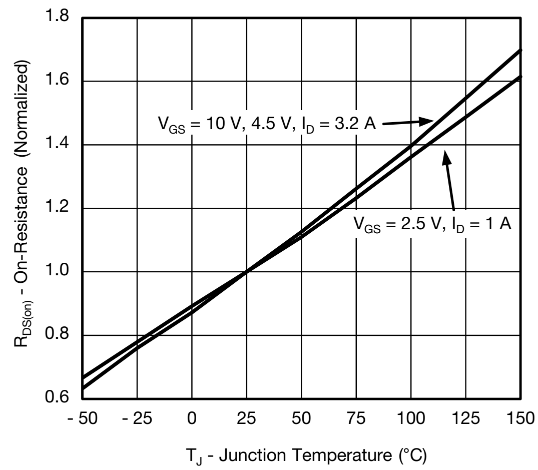


Capacitance

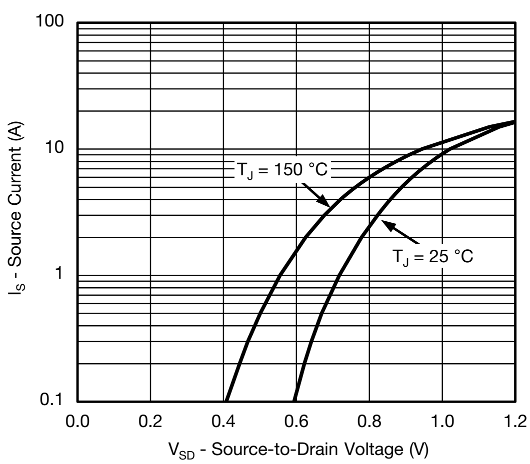
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



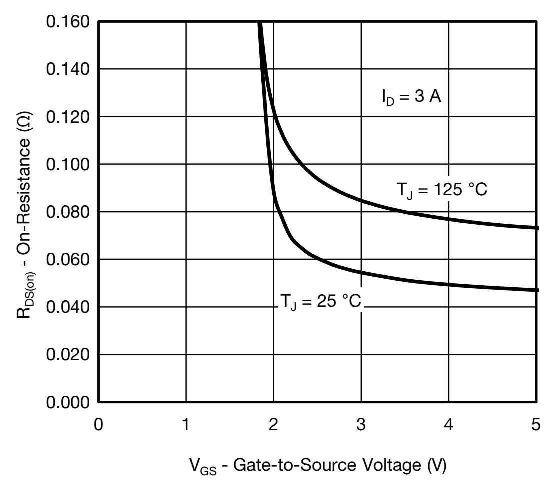
Gate Charge



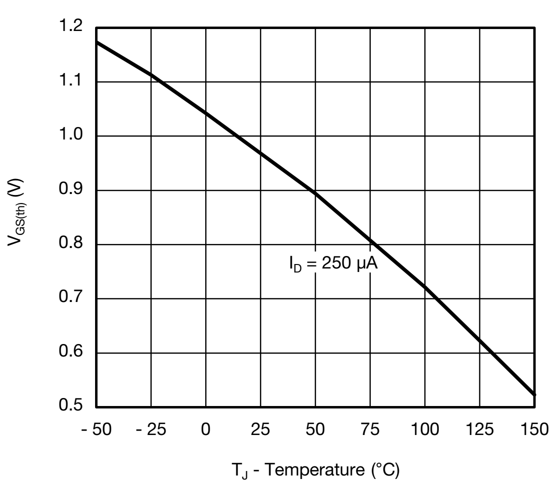
On-Resistance vs. Junction Temperature



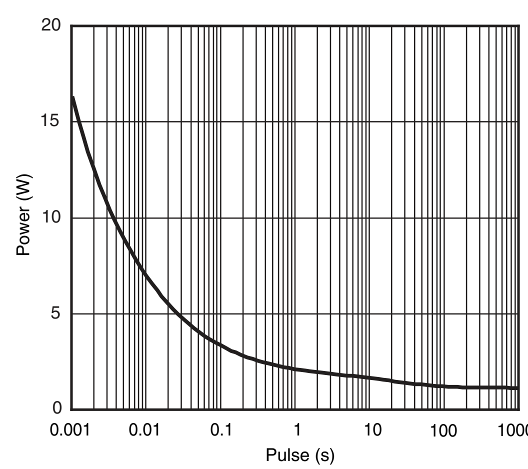
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

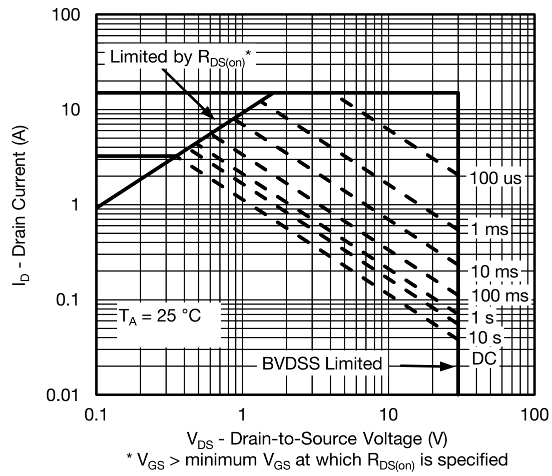


Threshold Voltage

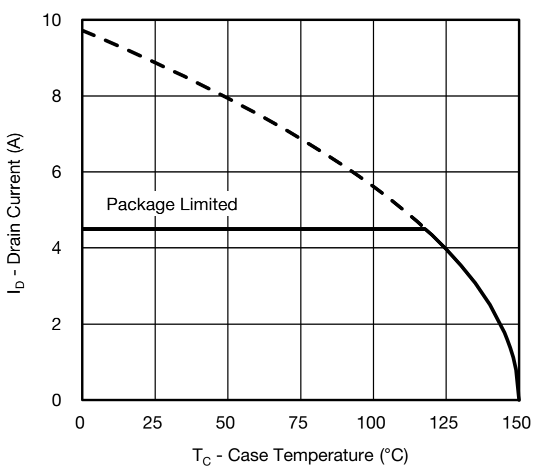


Single Pulse Power (Junction-to-Ambient)

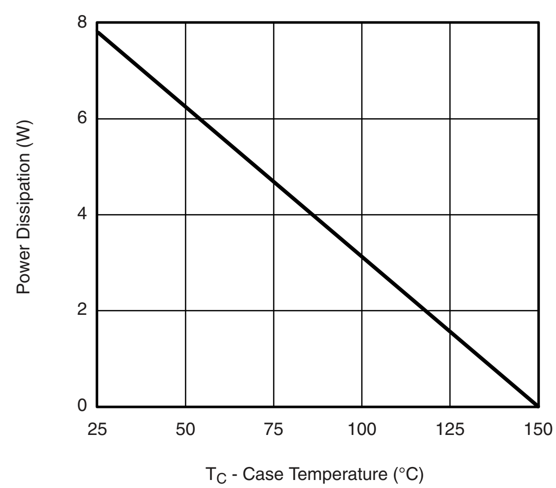
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



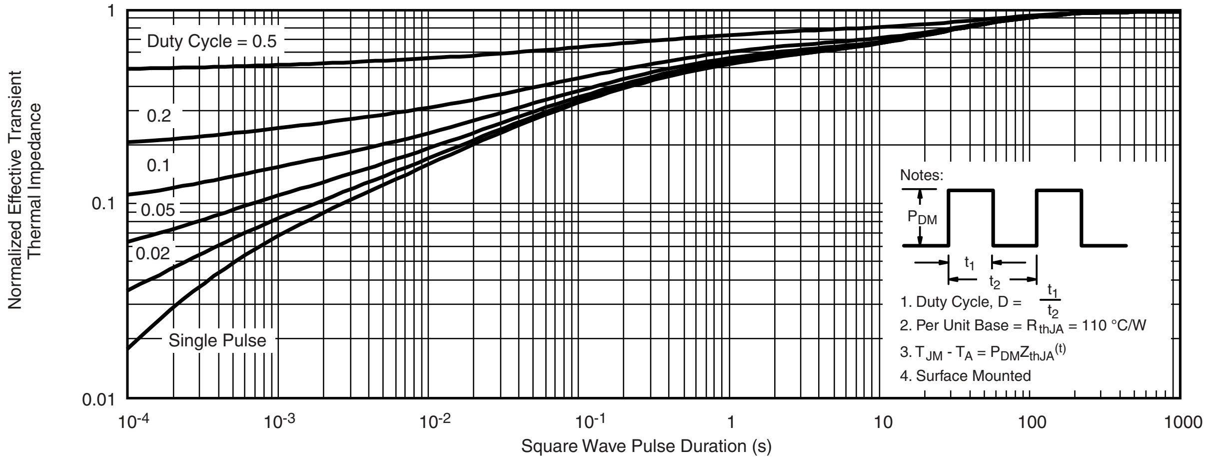
Current Derating*



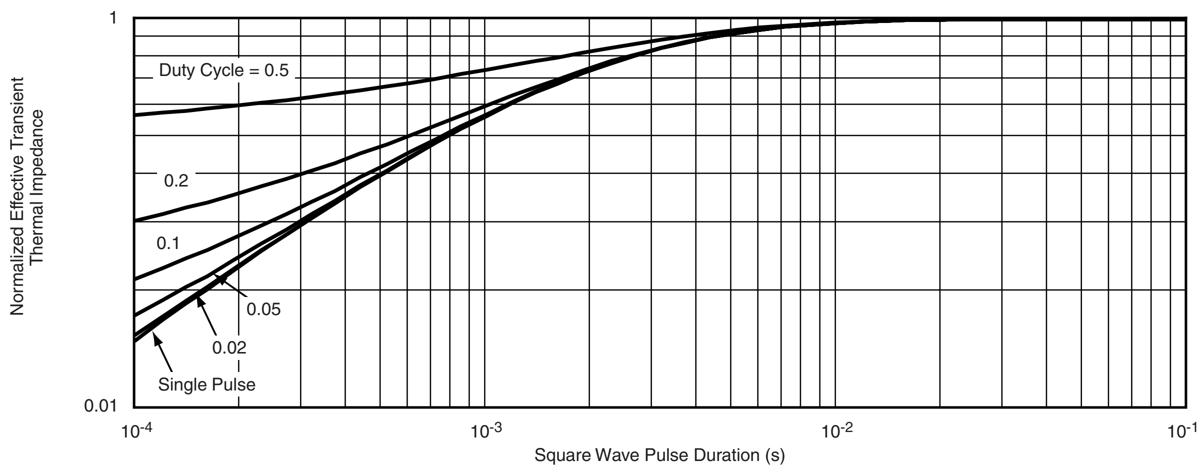
Power Derating

* The power dissipation P_D is based on $T_{J(max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



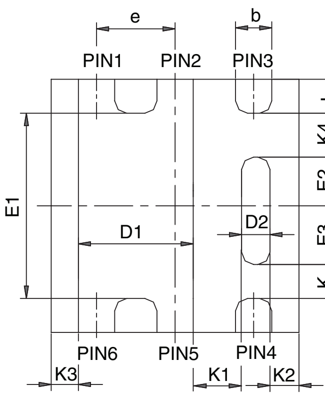
Normalized Thermal Transient Impedance, Junction-to-Ambient



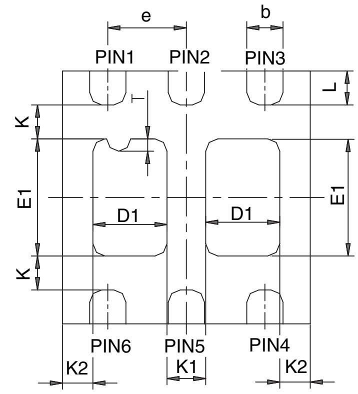
Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62818.

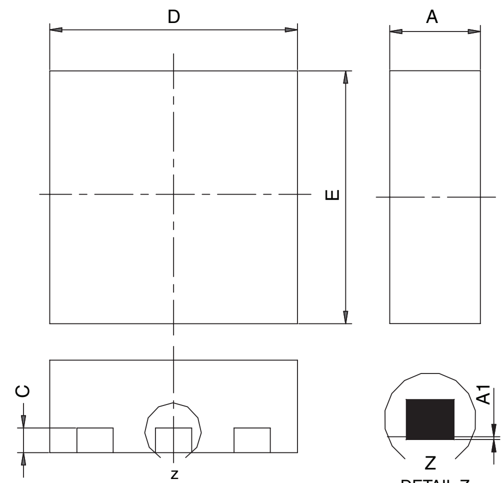
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL



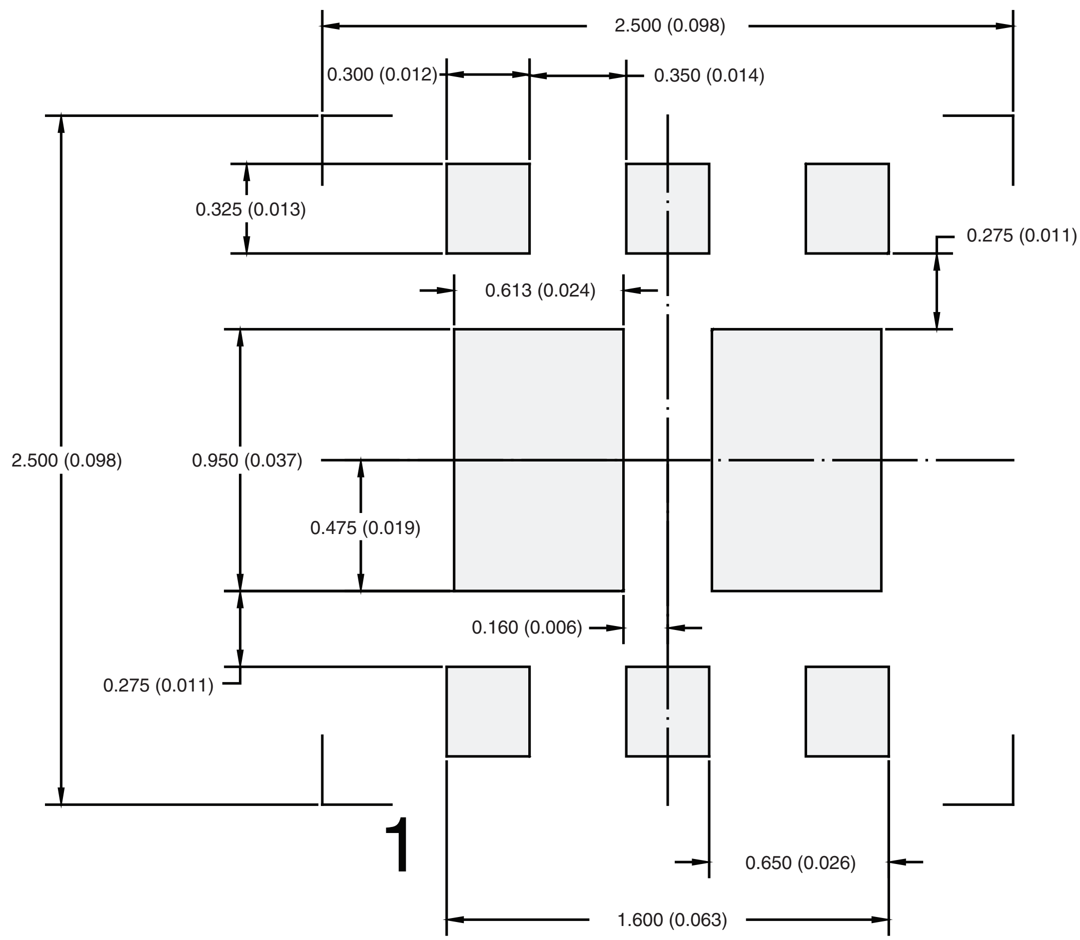
DETAIL Z

Notes:
1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006

ECN: C-07431 − Rev. C, 06-Aug-07
DWG: 5934

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)

Return to Index

Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay’s knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer’s responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and/or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer’s technical experts. Product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.