50 A VRPower® Integrated Power Stage

DESCRIPTION

The SiC631 is integrated power stage solutions optimized for synchronous buck applications to offer high current, high efficiency, and high power density performance. Packaged in Vishay's proprietary 5 mm x 5 mm MLP package, SiC631 enables voltage regulator designs to deliver up to 50 A continuous current per phase.

The internal power MOSFETs utilizes Vishay's state-of-the-art Gen IV TrenchFET technology that delivers industry benchmark performance to significantly reduce switching and conduction losses.

The SiC631 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, an integrated bootstrap Schottky diode, and zero current detection to improve light load efficiency. The driver is also compatible with a wide range of PWM controllers, supports tri-state PWM, and 5 V PWM logic.

A user selectable diode emulation mode (ZCD_EN#) is included to improve the light load performance. The device also supports PS4 mode to reduce power consumption when system operates in standby state.

FEATURES

- Thermally enhanced PowerPAK® MLP55-31L package
- Vishay's Gen IV MOSFET technology and a low-side MOSFET with integrated Schottky diode
- Delivers in excess of 50 A continuous current, 55 A at 10 ms peak current
- High efficiency performance
- High frequency operation up to 2 MHz
- Power MOSFETs optimized for 19 V input stage
- 5 V PWM logic with tri-state and hold-off
- Supports PS4 mode light load requirement for IMVP8 with low shutdown supply current (5 V, 3 µA)
- Under voltage lockout for V_{CIN}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Multi-phase VRDs for computing, graphics card and memory
- Intel IMVP-8 VRPower delivery
  - V_{CORE}, $V_{GRAPHICS}$, $V_{SYSTEM\ AGENT}$ Skylake, Kabylake platforms
  - V_{CCGI} for Apollo Lake platforms
- Up to 24 V rail input DC/DC VR modules

TYPICAL APPLICATION DIAGRAM

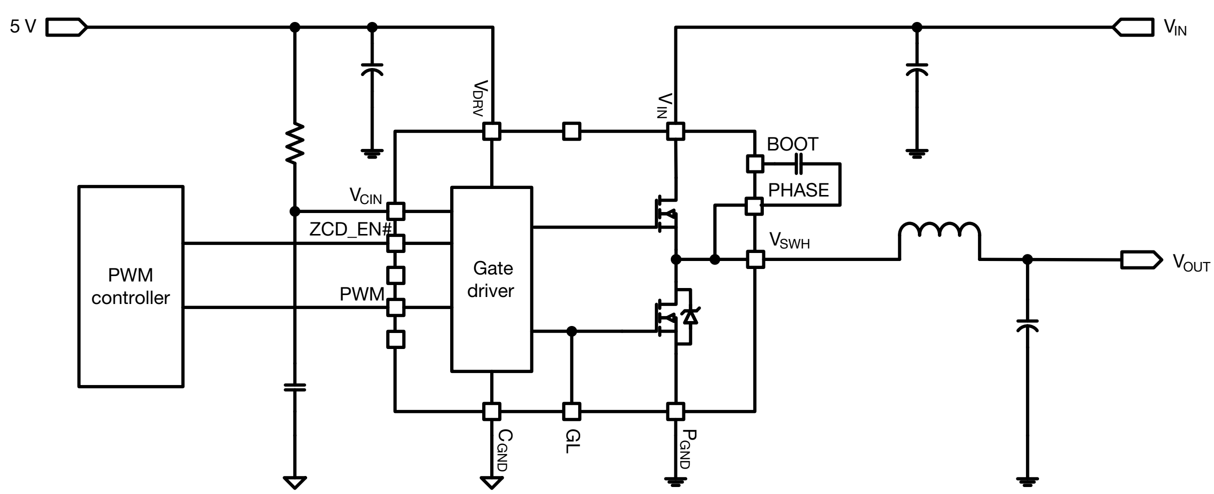


Fig. 1 - SiC631 Typical Application Diagram

PINOUT CONFIGURATION

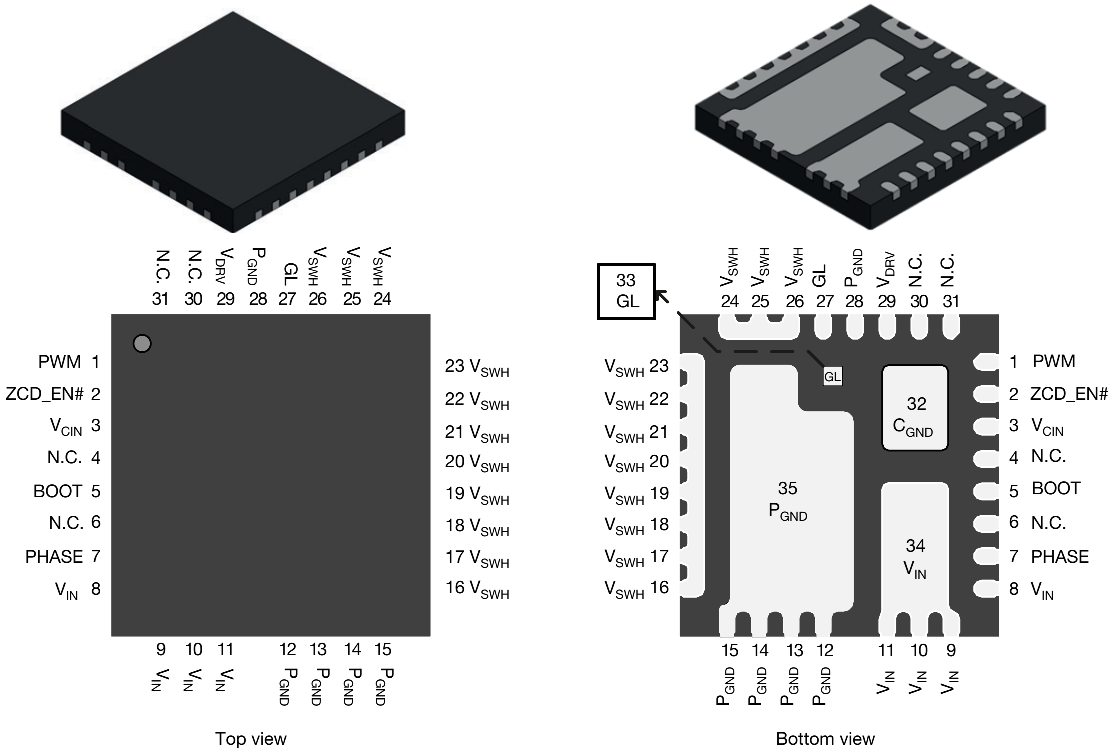
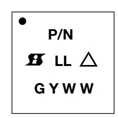
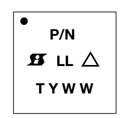
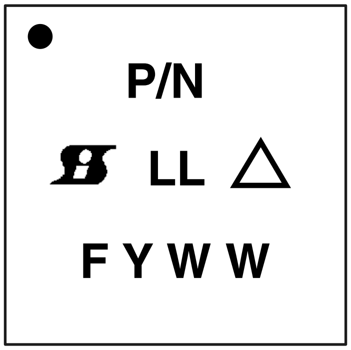


Fig. 2 - SiC631 Pin Configuration

PIN CONFIGURATION		
PIN NUMBER	**NAME**	**FUNCTION**
1	PWM	PWM input logic
2	ZCD_EN#	The ZCD_EN# pin enables or disables diode emulation. When ZCD_EN# is LOW, diode emulation is allowed. When ZCD_EN# is HIGH, continuous conduction mode is forced. ZCD_EN# can also be put in a high impedance mode by floating the pin. If both ZCD_EN# and PWM are floating, the device shuts down and consumes typically 3 μA (9 μA max.) current.
3	V_{CIN}	Supply voltage for internal logic circuitry
5	BOOT	High-side driver bootstrap voltage
4, 6, 30, 31	N.C.	Pin 4 can be either left floating or connected to C_{GND}. Internally it is either connected to GND or not internally connected depending on manufacturing location. Factory code "G" on line 3, pin 4 = C_{GND} Factory code "T" on line 3, pin 4 = not internally connected  
7	PHASE	Return path of high-side gate driver
8 to 11, 34	V_{IN}	Power stage input voltage. Drain of high-side MOSFET
12 to 15, 28, 35	P_{GND}	Power ground
16 to 26	V_{SWH}	Phase node of the power stage
27, 33	GL	Low-side MOSFET gate signal
29	V_{DRV}	Supply voltage for internal gate driver
32	C_{GND}	Signal ground

ORDERING INFORMATION			
PART NUMBER	**PACKAGE**	**MARKING CODE**	**OPTION**
SiC631CD-T1-GE3	PowerPAK MLP55-31L	SiC631	5 V PWM optimized
SiC631DB	Reference board		

PART MARKING INFORMATION



●	=	Pin 1 Indicator
P/N	=	Part Number Code
	=	Siliconix Logo
△	=	ESD Symbol
F	=	Assembly Factory Code
Y	=	Year Code
WW	=	Week Code
LL	=	Lot Code

ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	CONDITIONS	LIMIT	UNIT
Input Voltage	V_{IN}	-0.3 to +28	V
Control Logic Supply Voltage	V_{CIN}	-0.3 to +7	
Drive Supply Voltage	V_{DRV}	-0.3 to +7	
Switch Node (DC voltage)	V_{SWH}	-0.3 to +28	
Switch Node (AC voltage) (1)		-7 to +35	
BOOT Voltage (DC voltage)	V_{BOOT}	33	
BOOT Voltage (AC voltage) (2)		40	
BOOT to PHASE (DC voltage)	$V_{BOOT-PHASE}$	-0.3 to +7	
BOOT to PHASE (AC voltage) (3)		-0.3 to +8	
All Logic Inputs and Outputs (PWM, ZCD_EN#)		-0.3 to V_{CIN} +0.3	
Max. Operating Junction Temperature	T_J	150	°C
Ambient Temperature	T_A	-40 to +125	
Storage Temperature	T_{stg}	-65 to +150	
Electrostatic Discharge Protection	Human body model, JESD22-A114	2000	V
	Charged device model, JESD22-C101	1000	

Notes

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

(1) The specification values indicated "AC" is V_{SWH} to P_{GND} -8 V (< 20 ns, 10 μJ), min. and 35 V (< 50 ns), max.

(2) The specification value indicates "AC voltage" is V_{BOOT} to P_{GND}, 40 V (< 50 ns) max.

(3) The specification value indicates "AC voltage" is V_{BOOT} to V_{PHASE}, 8 V (< 50 ns) max.

RECOMMENDED OPERATING RANGE				
ELECTRICAL PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNIT
Input Voltage (V_{IN})	4.5	-	24	V
Drive Supply Voltage (V_{DRV})	4.5	5	5.5	
Control Logic Supply Voltage (V_{CIN})	4.5	5	5.5	
BOOT to PHASE ($V_{BOOT-PHASE}$, DC voltage)	4	4.5	5.5	
Thermal Resistance from Junction to Ambient	-	10.6	-	°C/W
Thermal Resistance from Junction to Case	-	1.6	-	

ELECTRICAL SPECIFICATIONS (ZCD_EN# = 5 V, V_{IN} = 12 V, V_{DRV} and V_{CIN} = 5 V, T_A = 25 °C, unless otherwise stated)						
PARAMETER	SYMBOL	TEST CONDITION	LIMITS			UNIT
			MIN.	TYP.	MAX.	
POWER SUPPLY						
Control Logic Supply Current	I_{VCIN}	V_{PWM} = FLOAT	-	80	-	µA
		V_{PWM} = FLOAT, $V_{ZCD\_EN\#}$ = 0 V	-	120	-	
		f_S = 300 kHz, D = 0.1	-	300	-	
Drive Supply Current	I_{VDRV}	f_S = 300 kHz, D = 0.1	-	10	20	mA
		f_S = 1 MHz, D = 0.1	-	30	-	
PS4 Mode Supply Current	I_{VCIN} + I_{VDRV}	V_{PWM} = $V_{ZCD\_EN\#}$ = FLOAT, T_A = -10 °C to +100 °C	-	3	9	µA
BOOTSTRAP SUPPLY						
Bootstrap Diode Forward Voltage	V_F	I_F = 2 mA	-	-	0.65	V
PWM CONTROL INPUT						
Rising Threshold	$V_{TH\_PWM\_R}$		3.6	3.9	4.2	V
Falling Threshold	$V_{TH\_PWM\_F}$		0.72	1	1.3	
Tri-state Voltage	V_{TRI}	V_{PWM} = FLOAT	-	2.5	-	
Tri-state Rising Threshold	$V_{TRI\_TH\_R}$		1.1	1.35	1.6	
Tri-state Falling Threshold	$V_{TRI\_TH\_F}$		3.4	3.7	4	
Tri-state Rising Threshold Hysteresis	$V_{HYS\_TRI\_R}$		-	325	-	mV
Tri-state Falling Threshold Hysteresis	$V_{HYS\_TRI\_F}$		-	250	-	
PWM Input Current	I_{PWM}	V_{PWM} = 5 V	-	-	350	µA
		V_{PWM} = 0 V	-	-	-350	
ZCD_EN# CONTROL INPUT						
Rising Threshold	$V_{TH\_ZCD\_EN\#\_R}$		3.3	3.6	3.9	V
Falling Threshold	$V_{TH\_ZCD\_EN\#\_F}$		1.1	1.4	1.7	
Tri-state Voltage	$V_{TRI\_ZCD\_EN\#}$	$V_{ZCD\_EN\#}$ = FLOAT	-	2.5	-	
Tri-state Rising Threshold	$V_{TRI\_ZCD\_EN\#\_R}$		1.5	1.8	2.1	
Tri-state Falling Threshold	$V_{TRI\_ZCD\_EN\#\_F}$		2.9	3.15	3.4	
Tri-state Rising Threshold Hysteresis	$V_{HYS\_TRI\_ZCD\#\_R}$		-	375	-	mV
Tri-state Falling Threshold Hysteresis	$V_{HYS\_TRI\_ZCD\#\_F}$		-	450	-	
ZCD_EN# Input Current	$I_{ZCD\_EN\#}$	$V_{ZCD\_EN\#}$ = 5 V	-	-	100	µA
		$V_{ZCD\_EN\#}$ = 0 V	-	-	-100	
PS4 Exit Latency	$t_{PS4EXIT}$		-	-	5	µs
TIMING SPECIFICATIONS						
Tri-State to GH/GL Rising Propagation Delay	$t_{PD\_TRI\_R}$	No load, see fig. 4	-	20	-	ns
Tri-state Hold-Off Time	t_{TSHO}		-	150	-	
GH - Turn Off Propagation Delay	$t_{PD\_OFF\_GH}$		-	20	-	
GH - Turn On Propagation Delay (Dead time rising)	$t_{PD\_ON\_GH}$		-	15	-	
GL - Turn Off Propagation Delay	$t_{PD\_OFF\_GL}$		-	20	-	
GL - Turn On Propagation Delay (Dead time falling)	$t_{PD\_ON\_GL}$		-	20	-	
PWM Minimum On-Time	$t_{PWM\_ON\_MIN.}$		30	-	-	
PROTECTION						
Under Voltage Lockout	V_{UVLO}	V_{CIN} rising, on threshold	-	3.4	3.9	V
		V_{CIN} falling, off threshold	2.4	2.9	-	
Under Voltage Lockout Hysteresis	V_{UVLO_HYST}		-	500	-	mV

Notes

(1) Typical limits are established by characterization and are not production tested

(2) Guaranteed by design

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-state Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{PWM\_TH\_R}$ the low-side is turned ON and the high-side is turned ON. When PWM input is driven below $V_{PWM\_TH\_F}$ the high-side is turned OFF and the low-side is turned ON. For tri-state logic, the PWM input operates as previously stated for driving the MOSFETs when PWM is logic high and logic low. However, there is an third state that is entered as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC631 to pull the PWM input into the tri-state region (see definition of PWM logic and tri-state, fig. 4). If the PWM input stays in this region for the tri-state hold-off period, t_{TSHO}, both high-side and low-side MOSFETs are turned OFF. The function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC631 incorporates PWM voltage thresholds that are compatible with 5 V.

Diode Emulation Mode and PS4 Mode (ZCD_EN#)

The ZCD_EN# pin enables or disables diode emulation mode. When ZCD_EN# is driven below $V_{TH\_ZCD\_EN\#\_F}$, diode emulation is allowed. When ZCD_EN# is driven above $V_{TH\_ZCD\_EN\#\_R}$, continuous conduction mode is forced. Diode emulation mode allows for higher converter efficiency under light load situations. With diode emulation active, the SiC631 will detect the zero current crossing of the output inductor and turn off the low-side MOSFET. This ensures that discontinuous conduction mode (DCM) is achieved. Diode emulation is asynchronous to the PWM signal, therefore, the SiC631 will respond to the ZCD_EN# input immediately after it changes state.

The ZCD_EN# pin can be floated resulting in a high impedance state. High impedance on the input of ZCD_EN# combined with a tri-stated PWM output will shut down the SiC631, reducing current consumption to typically 5 μA. This is an important feature in achieving the low standby current requirements required in the PS4 state in ultrabooks and notebooks.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The switch node, V_{SWH}, is the circuit power stage output. This is the output applied to the power inductor and output filter to deliver the output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor.

Ground Connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the printed circuit board should be such that the inductance separating C_{GND} and P_{GND} is minimized. Transient differences due to inductance effects between these two pins should not exceed 0.5 V

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap diode and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

Shoot-Through Protection and Adaptive Dead Time

The SiC631 has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFETs are not turned ON at the same time. The adaptive dead time control operates as follows. The high-side and low-side gate voltages are monitored to prevent the one turning ON from tuning ON until the other's gate voltage is sufficiently low (< 1 V). Built in delays also ensure that one power MOS is completely OFF, before the other can be turned ON. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gates low until the supply voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC631 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device.

FUNCTIONAL BLOCK DIAGRAM

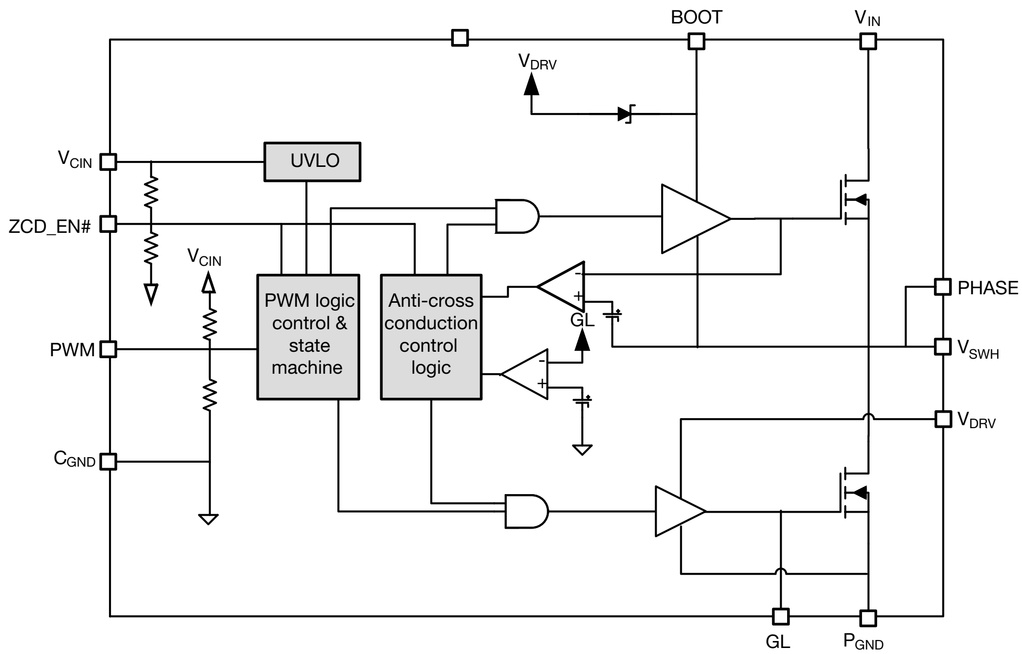


Fig. 3 - SiC631 Functional Block Diagram

DEVICE TRUTH TABLE			
ZCD_EN#	**PWM**	**GH**	**GL**
Tri-state	X	L	L
L	L	L	H, $I_L > 0$ A L, $I_L < 0$ A
L	H	H	L
L	Tri-state	L	L
H	L	L	H
H	H	H	L
H	Tri-state	L	L

PWM TIMING DIAGRAM

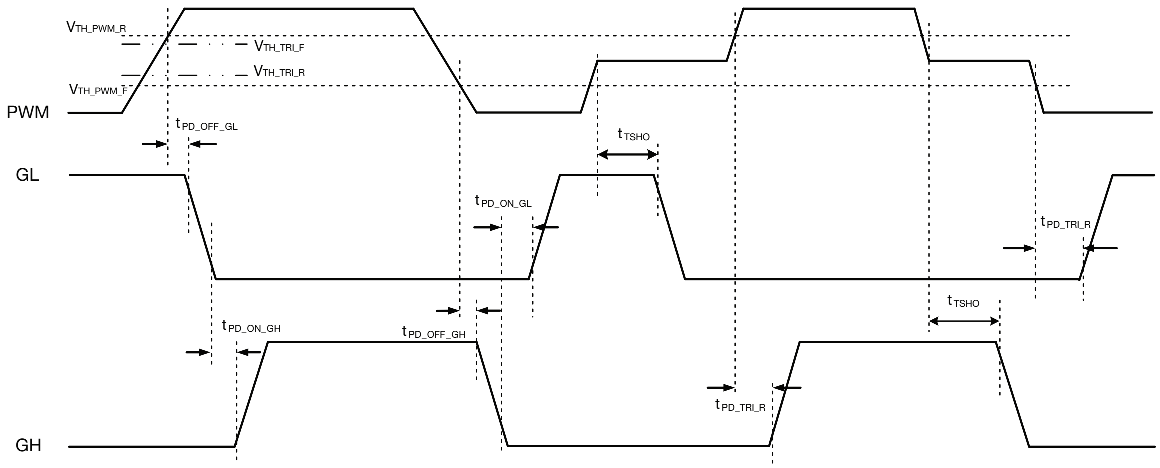


Fig. 4 - Definition of PWM Logic and Tri-state

ZCD_EN# - PS4 EXIT TIMING

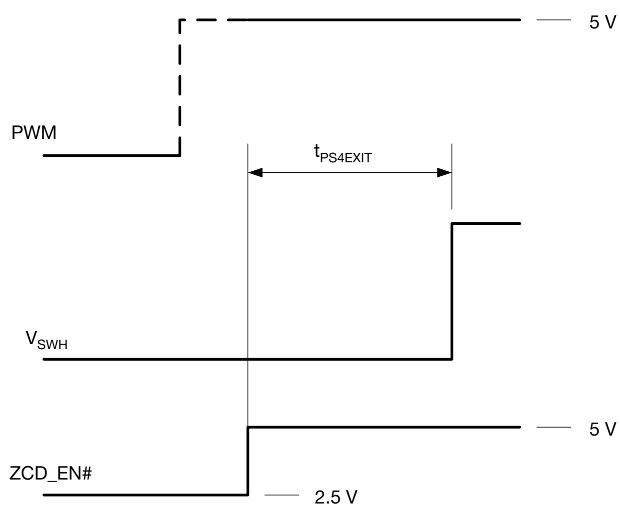


Fig. 5 - ZCD_EN# - PS4 Exit Timing

ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 13 V (unless otherwise stated), V_{DRV} = V_{CIN} = 5 V, ZCD_EN# = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH (DCR = 0.32 mΩ), T_A = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC631 losses only unless otherwise stated)

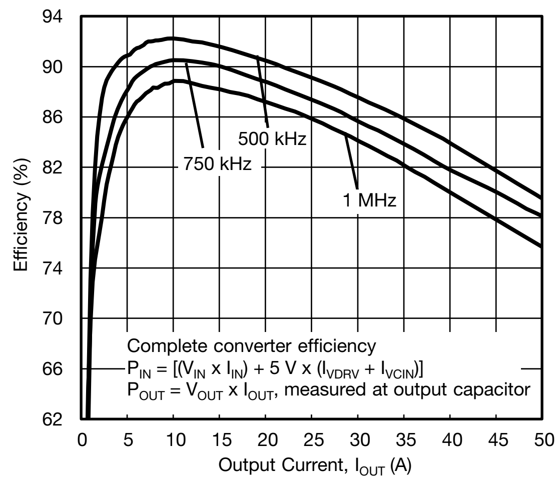


Fig. 6 - Efficiency vs. Output Current (V_{IN} = 12.6 V)

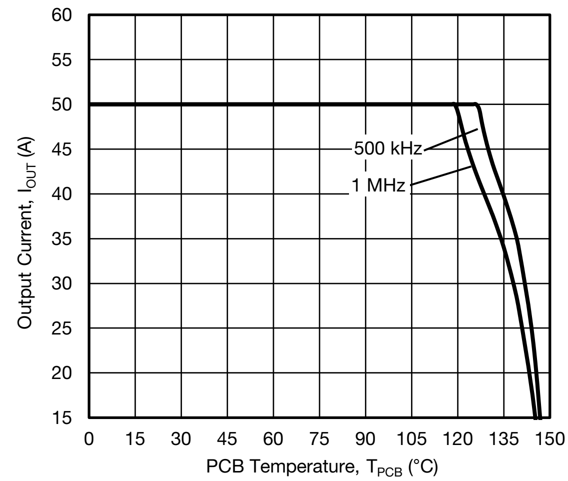


Fig. 9 - Safe Operating Area (V_{IN} = 12.6 V)

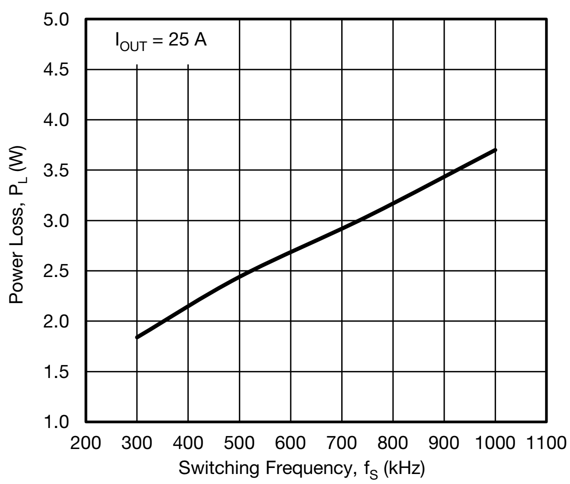


Fig. 7 - Power Loss vs. Switching Frequency (V_{IN} = 12.6 V)

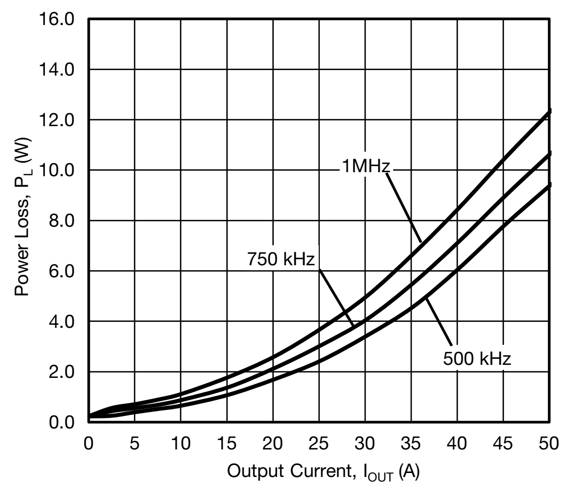


Fig. 10 - Power Loss vs. Output Current (V_{IN} = 12.6 V)

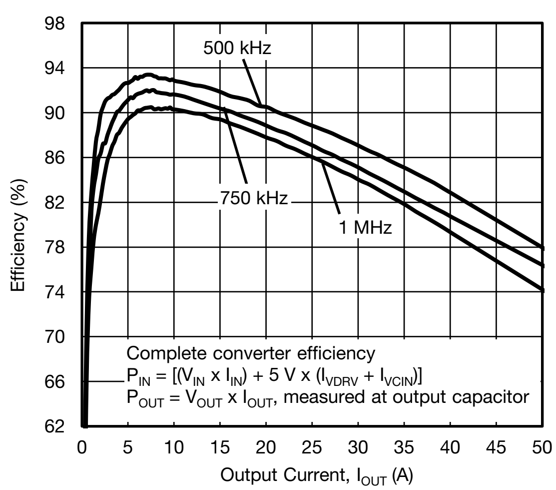


Fig. 8 - Efficiency vs. Output Current (V_{IN} = 9 V)

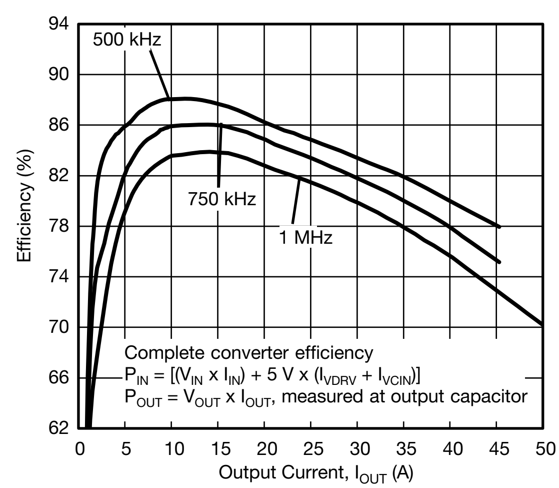


Fig. 11 - Efficiency vs. Output Current (V_{IN} = 19 V)

ELECTRICAL CHARACTERISTICS

Test condition: V_{IN} = 13 V (unless otherwise stated), V_{DRV} = V_{CIN} = 5 V, ZCD_EN# = 5 V, V_{OUT} = 1 V, L_{OUT} = 250 nH (DCR = 0.32 mΩ), T_A = 25 °C, natural convection cooling (All power loss and normalized power loss curves show SiC631 losses only unless otherwise stated)

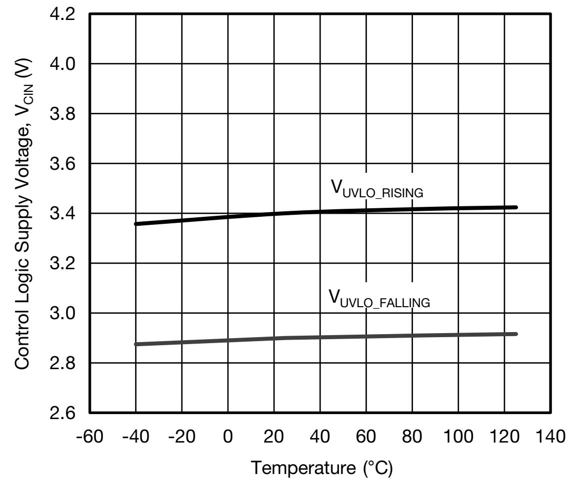


Fig. 12 - UVLO Threshold vs. Temperature

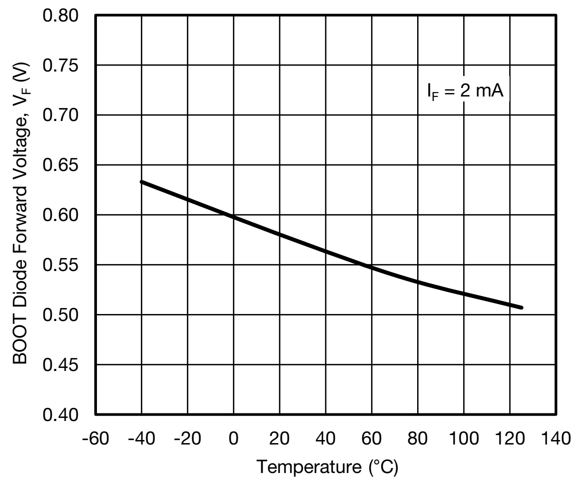


Fig. 15 - BOOT Diode Forward Voltage vs. Temperature

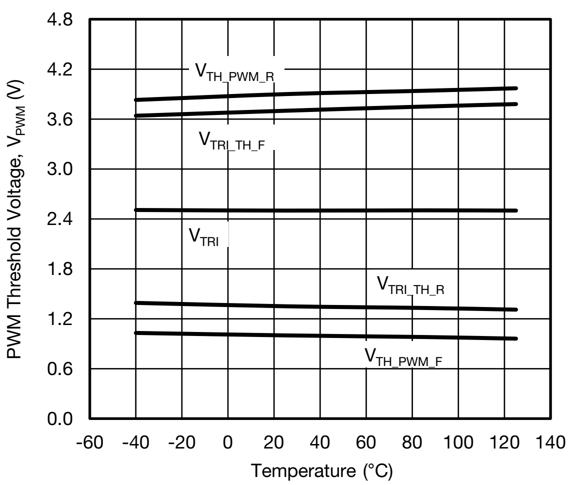


Fig. 13 - PWM Threshold vs. Temperature

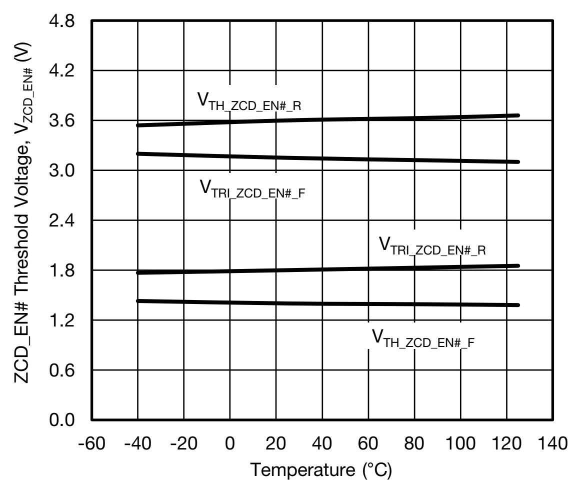


Fig. 16 - ZCD_EN# Threshold vs. Temperature

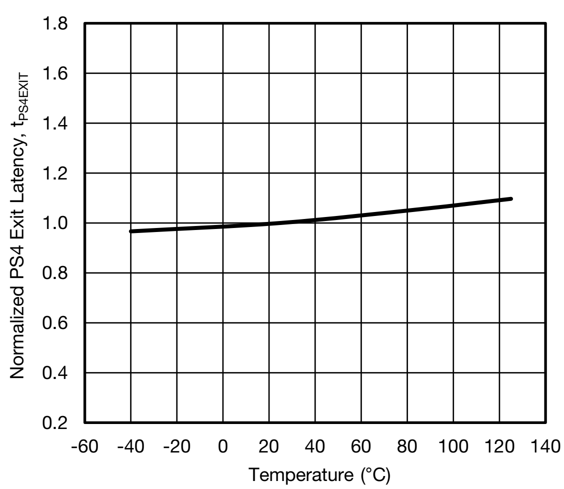


Fig. 14 - PS4 Exit Latency vs. Temperature

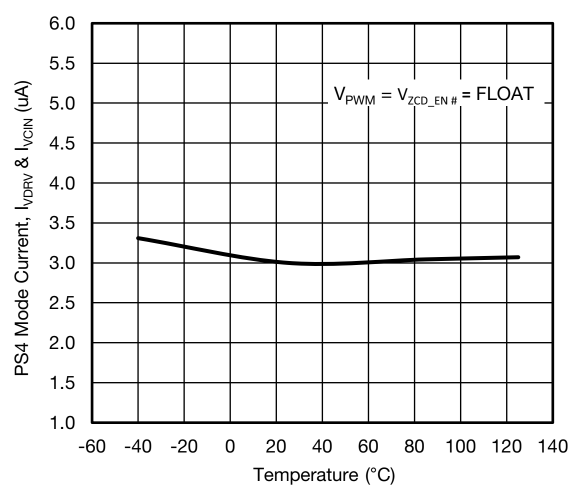
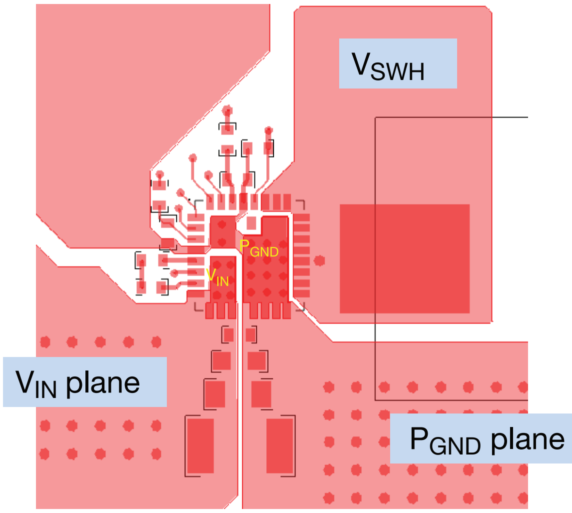


Fig. 17 - PS4 Mode Current vs. Temperature

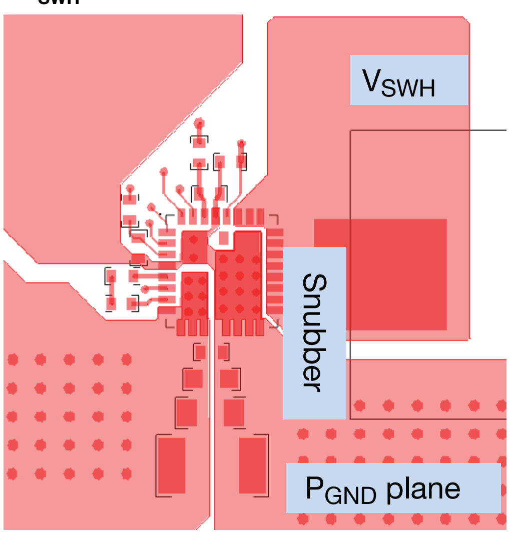
PCB LAYOUT RECOMMENDATIONS

Step 1: V_{IN}/GND Planes and Decoupling



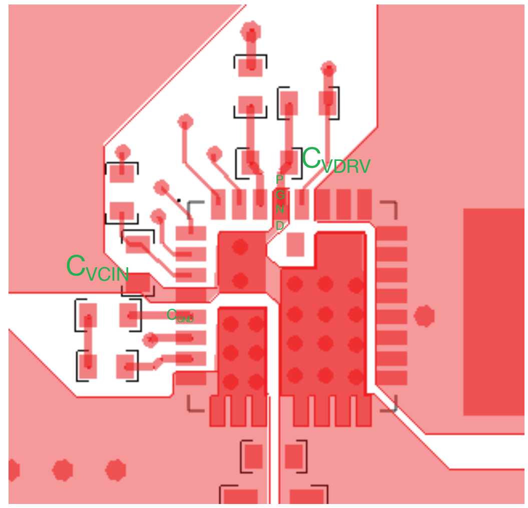
1. Layout V_{IN} and P_{GND} planes as shown above
2. Ceramic capacitors should be placed directly between V_{IN} and P_{GND}, and close to the device for best decoupling effect
3. Different values / packages of ceramic capacitors should be used to cover entire decoupling spectrum e.g. 1210, 0805, 0603 and 0402
4. Smaller capacitance values, closer to device V_{IN} pin(s), - results in better high frequency noise absorbing

Step 2: V_{SWH} Plane



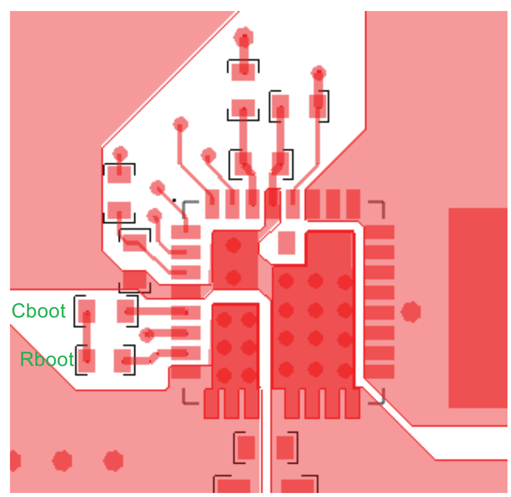
1. Connect output inductor to DrMOS with large plane to lower resistance
2. If a snubber network is required, place the components as shown above, the network can be placed at bottom

Step 3: V_{CIN}/V_{DRV} Input Filter



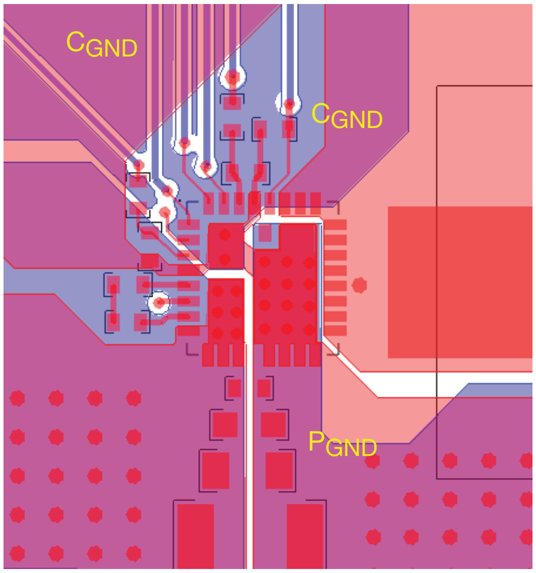
1. The V_{CIN}/V_{DRV} input filter ceramic capacitors should be placed close to IC. It is recommended to connect two caps separately.
2. V_{CIN} capacitor should be placed between pin 3 (V_{CIN}) and pin 4 (C_{GND} of driver IC) to achieve best noise filtering.
3. V_{DRV} capacitor should be placed between pin 28 (P_{GND} of driver IC) and pin 29 (V_{DRV}) to provide maximum instantaneous driver current for low-side MOSFET during switching cycle
4. It is recommended to use a large plane analog ground, C_{GND}, plane to reduce parasitic inductance.

Step 4: BOOT Resistor and Capacitor Placement



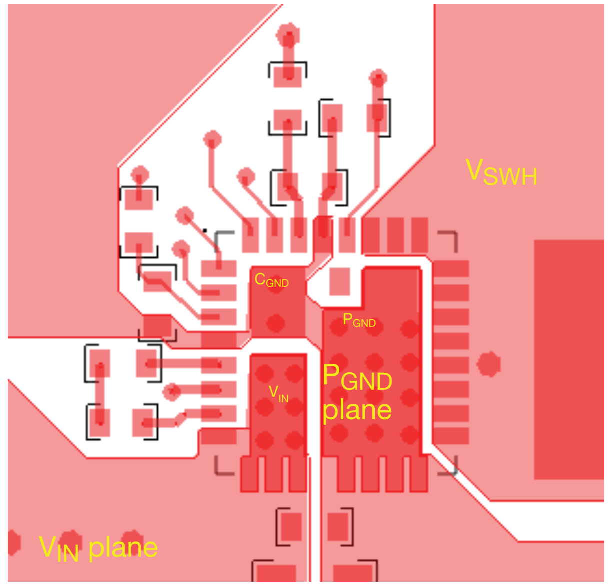
1. The components should be placed close to IC, directly between PHASE (pin 7) and BOOT (pin 5).
2. To reduce parasitic inductance, chip size 0402 can be used.

Step 5: Signal Routing



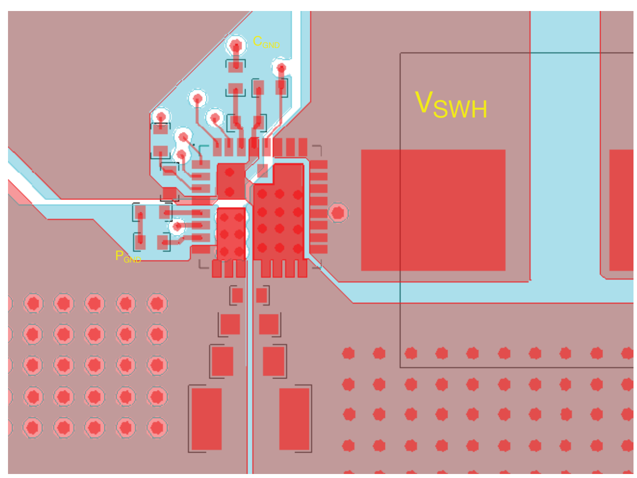
1. Route the PWM / ZCD_EN# signal traces out of the top left corner, next to DrMOS pin 1.
2. PWM is an important signal, both signal and return traces should not cross any power nodes on any layer.
3. It is best to “shield” traces form power switching nodes, e.g. V_{SWH}, to improve signal integrity.
4. GL (pin 27) has been connected with GL pad internally and does not need to connect externally.

Step 6: Adding Thermal Relief Vias



1. Thermal relief vias can be added on the V_{IN} and P_{GND} pads to utilize inner layers for high-current and thermal dissipation.
2. To achieve better thermal performance, additional vias can be added to V_{IN} and P_{GND} planes.
3. V_{SWH} pad is a noise source and not recommended to put vias on this plane.
4. 8 mil vias for pads and 10 mils vias for planes are the optimal via sizes. Vias on pads may drain solder during assembly and cause assembly issue. Please consult with the assembly house for guideline.

Step 7: Ground Connection



1. It is recommended to make a single connection between C_{GND} and P_{GND}, this connection can be done on top layer.
2. It is recommended to make the entire first inner layer (next to top layer) a ground plane and separate it into C_{GND} and P_{GND} plane.
3. These ground planes provide shielding between noise sources on top layer and signal traces on bottom layer.

Multi-Phases VRPower PCB Layout

The following is an example of 6 phase layout. As can be seen, all the VRPower stages are lined in X-direction compactly with decoupling capacitors next to them. The inductors are placed as close as possible to the SiC631 to minimize the PCB copper loss. Vias are applied on all PADs (V_{IN}, P_{GND}, C_{GND}) of the SiC631 to ensure that both electrical and thermal performance are optimized. Large copper planes are used for all high current loops, such as V_{IN}, V_{SWH}, V_{OUT} and P_{GND}. These copper planes are duplicated in other layers to minimize the inductance and resistance. All the control signals are routed from the SiC631 to a controller placed to the north of the power stage through inner layers to avoid the overlap of high current loops. This achieves a compact design with the output from the inductors feeding a load located to the south of the design as shown in the figure.

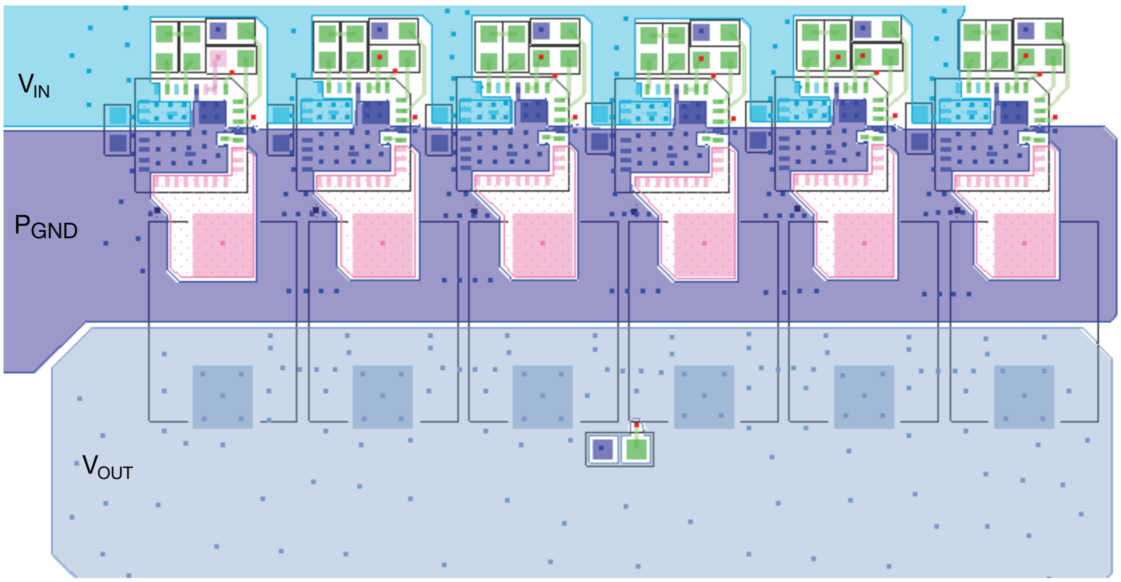


Fig. 18 - Multi - Phase VRPower Layout Top View

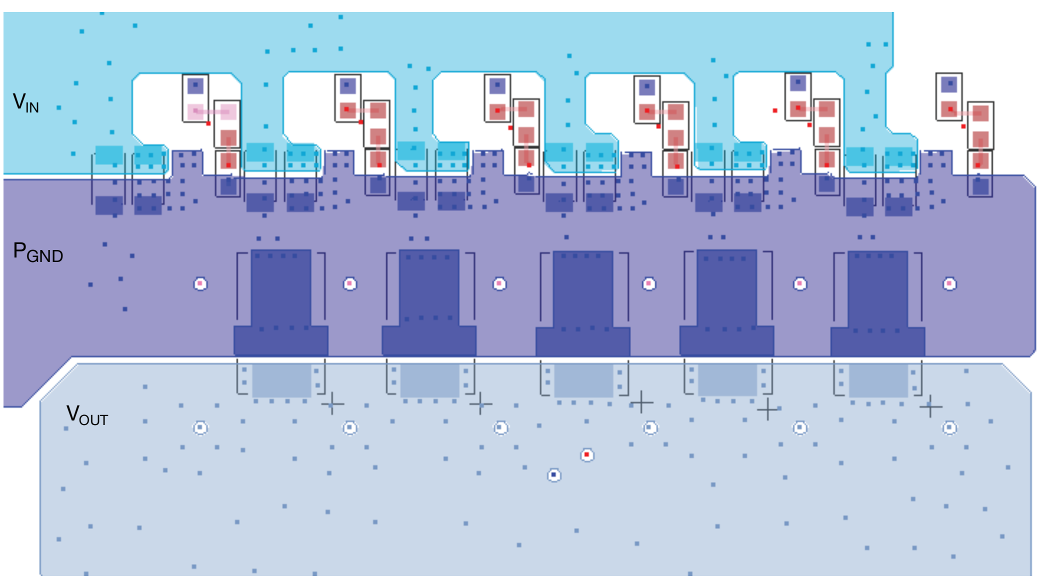
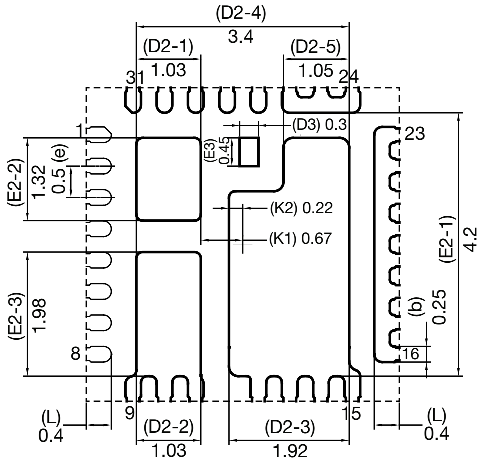


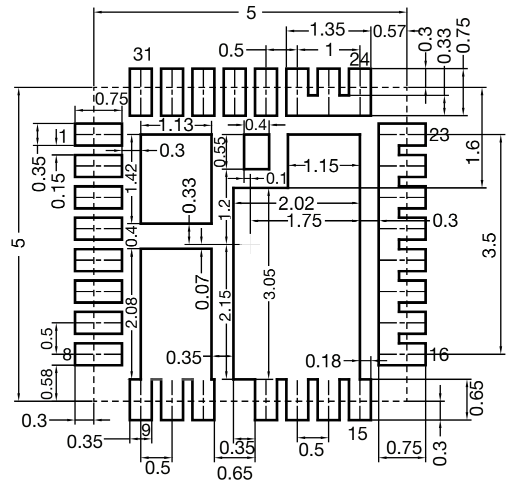
Fig. 19 - Multi - Phase VRPower Layout Bottom View

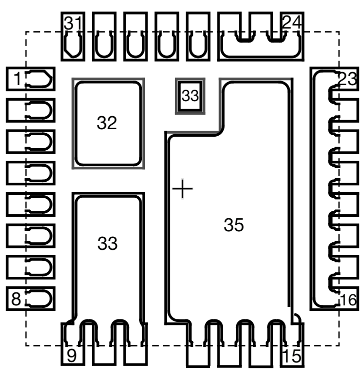
RECOMMENDED LAND PATTERN POWERPAK MLP55-31L

Package outline top view, transparent



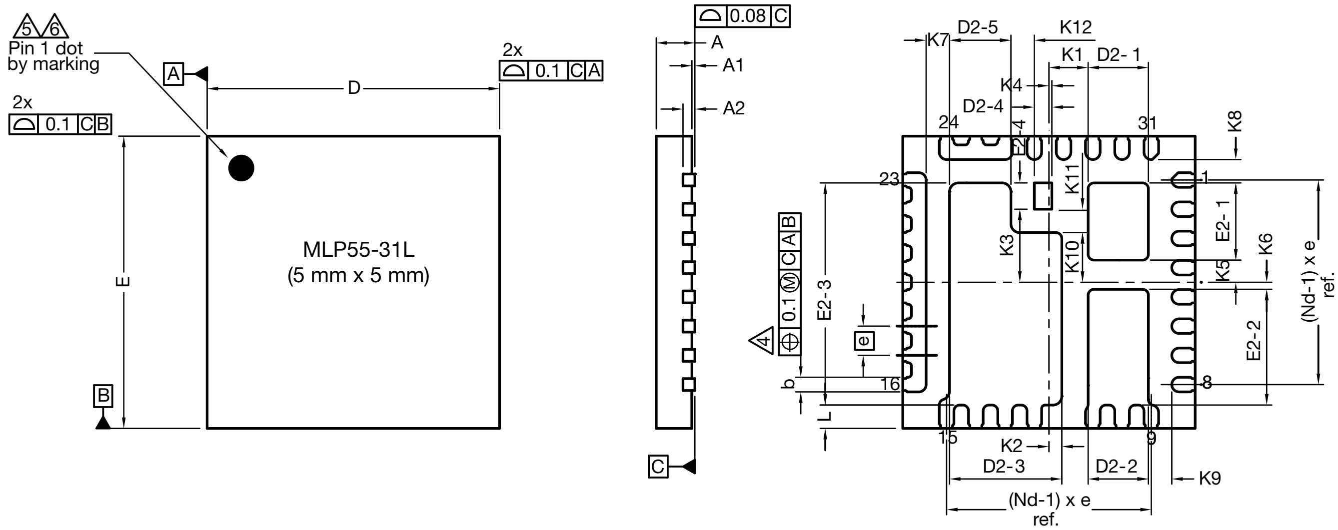
Land pattern for MLP55-31L





All dimensions in millimeters

PACKAGE OUTLINE DRAWING MLP55-31L



Top view Side view Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b (4)	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00 BSC			0.196 BSC		
e	0.50 BSC			0.019 BSC		
E	5.00 BSC			0.196 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)	32			32		
Nd (3)	8			8		
Ne (3)	8			8		
D2-1	0.98	1.03	1.08	0.039	0.041	0.043
D2-2	0.98	1.03	1.08	0.039	0.041	0.043
D2-3	1.87	1.92	1.97	0.074	0.076	0.078
D2-4	0.30 BSC			0.012 BSC		
D2-5	1.00	1.05	1.10	0.039	0.041	0.043
E2-1	1.27	1.32	1.37	0.050	0.052	0.054
E2-2	1.93	1.98	2.03	0.076	0.078	0.080
E2-3	3.75	3.80	3.82	0.148	0.150	0.152
E2-4	0.45 BSC			0.018 BSC		
K1	0.67 BSC			0.026 BSC		
K2	0.22 BSC			0.008 BSC		
K3	1.25 BSC			0.049 BSC		

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
K4		0.05 BSC			0.002 BSC	
K5		0.38 BSC			0.015 BSC	
K6		0.12 BSC			0.005 BSC	
K7		0.40 BSC			0.016 BSC	
K8		0.40 BSC			0.016 BSC	
K9		0.40 BSC			0.016 BSC	
K10		0.85 BSC			0.033 BSC	
K11		0.40 BSC			0.016 BSC	
K12		0.40 BSC			0.016 BSC	

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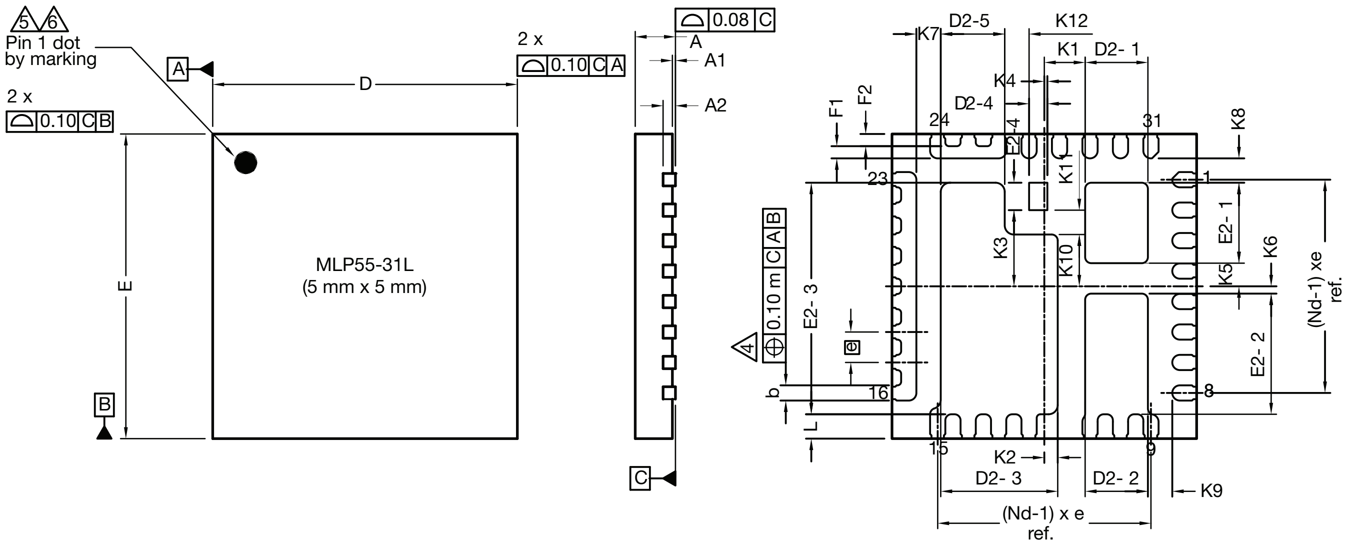
PowerPAK® MLP55-31L Case Outline



Top view Side view Bottom view

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2		0.20 ref.			0.008 ref.	
b (4)	0.20	0.25	0.30	0.008	0.010	0.012
D	4.90	5.00	5.10	0.193	0.196	0.200
e		0.50 BSC			0.019 BSC	
E	4.90	5.00	5.10	0.193	0.196	0.200
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)		32			32	
Nd (3)		8			8	
Ne (3)		8			8	
D2-1	0.98	1.03	1.08	0.039	0.041	0.043
D2-2	0.98	1.03	1.08	0.039	0.041	0.043
D2-3	1.87	1.92	1.97	0.074	0.076	0.078
D2-4		0.30 BSC			0.012 BSC	
D2-5	1.00	1.05	1.10	0.039	0.041	0.043
E2-1	1.27	1.32	1.37	0.050	0.052	0.054
E2-2	1.93	1.98	2.03	0.076	0.078	0.080
E2-3	3.75	3.80	3.82	0.148	0.150	0.152
E2-4		0.45 BSC			0.018 BSC	
F1		0.20 BSC			0.008 BSC	
F2		0.20 BSC			0.008 BSC	
K1		0.67 BSC			0.026 BSC	
K2		0.22 BSC			0.008 BSC	
K3		1.25 BSC			0.049 BSC	
K4		0.05 BSC			0.002 BSC	
K5		0.38 BSC			0.015 BSC	
K6		0.12 BSC			0.005 BSC	

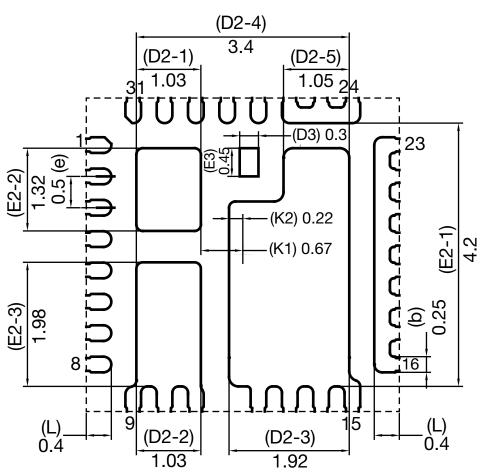
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
K7		0.40 BSC			0.016 BSC	
K8		0.40 BSC			0.016 BSC	
K9		0.40 BSC			0.016 BSC	
K10		0.85 BSC			0.033 BSC	
K11		0.40 BSC			0.016 BSC	
K12		0.40 BSC			0.016 BSC	
ECN: T16-0644-Rev. E, 24-Oct-16 DWG: 6025						

Notes

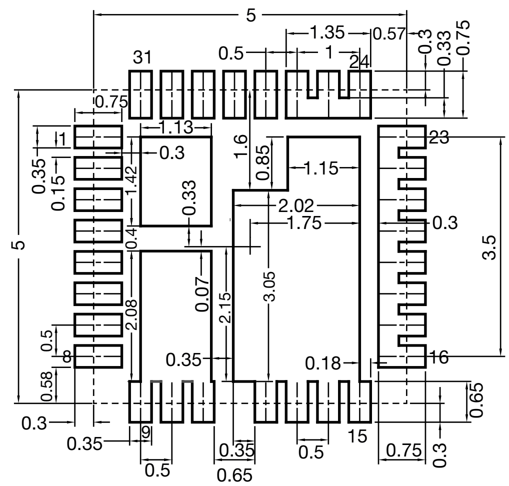
1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals,
   Nd is the number of terminals in X-direction, and
   Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

Recommended Land Pattern
PowerPAK® MLP55-31L for SiC620, SiC620A

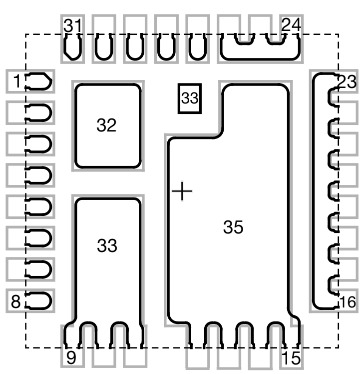
Top side transparent view
(not bottom view)



Land pattern for MLP55-31L



All dimensions in millimeters



Component for MLP55-31L

Land pattern for MLP55-31L

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