Integrated DrMOS Power Stage

DESCRIPTION

The SiC762CD is an integrated solution that contains PWM optimized n-channel MOSFETs (high side and low side) and a full featured MOSFET driver IC. The device complies with the Intel DrMOS standard for desktop and server V_{core} power stages. The SiC762CD delivers up to 35 A continuous output current and operates from an input voltage range of 3 V to 27 V. The integrated MOSFETs are optimized for output voltages in the ranges of 0.8 V to 2.0 V with a nominal input voltage of 24 V. The device can also deliver very high power at 5 V output for ASIC applications.

The SiC762CD incorporates an advanced MOSFET gate driver IC. This IC accepts a single PWM input from the V_R controller and converts it into the high side and low side MOSFET gate drive signals. The driver IC is designed to implement the skip mode (SMOD) function for light load efficiency improvement. Adaptive dead time control also works to improve efficiency at all load points. The SiC762CD has a thermal warning (THDN) that alerts the system of excessive junction temperature. The driver IC includes an enable pin, UVLO and shoot through protection.

The SiC762CD is optimized for high frequency buck applications. Operating frequencies in excess of 1 MHz can easily be achieved.

The SiC762CD is packaged in Vishay Siliconix high performance PowerPAK MLP6 x 6 package. Compact co-packaging of components helps to reduce stray inductance, and hence increases efficiency.

FEATURES

- Integrated Gen III MOSFETs and DrMOS compliant gate driver IC
- Enables V_{core} switching at 1 MHz
- Easily achieve > 90 % efficiency in multi-phase, low output voltage solutions
- Low ringing on the VSWH pin reduces EMI
- Pin compatible with DrMOS 6 x 6 version 3.0
- Tri-state PWM input function prevents negative output voltage swing
- 5 V logic levels on PWM
- MOSFET threshold voltage optimized for 5 V driver bias supply
- Automatic skip mode operation (SMOD) for light load efficiency
- Under-voltage lockout
- Built-in bootstrap schottky diode
- Adaptive deadtime and shoot through protection
- Thermal shutdown warning flag
- Low profile, thermally enhanced PowerPAK® MLP 6 x 6 40 pin package
- **Halogen-free according to IEC 61249-2-21 definition**
- **Compliant to RoHS directive 2002/95/EC**

APPLICATIONS

- CPU and GPU core voltage regulation
- Server, computer, workstation, game console, graphics boards, PC

SIC762CD APPLICATION DIAGRAMM

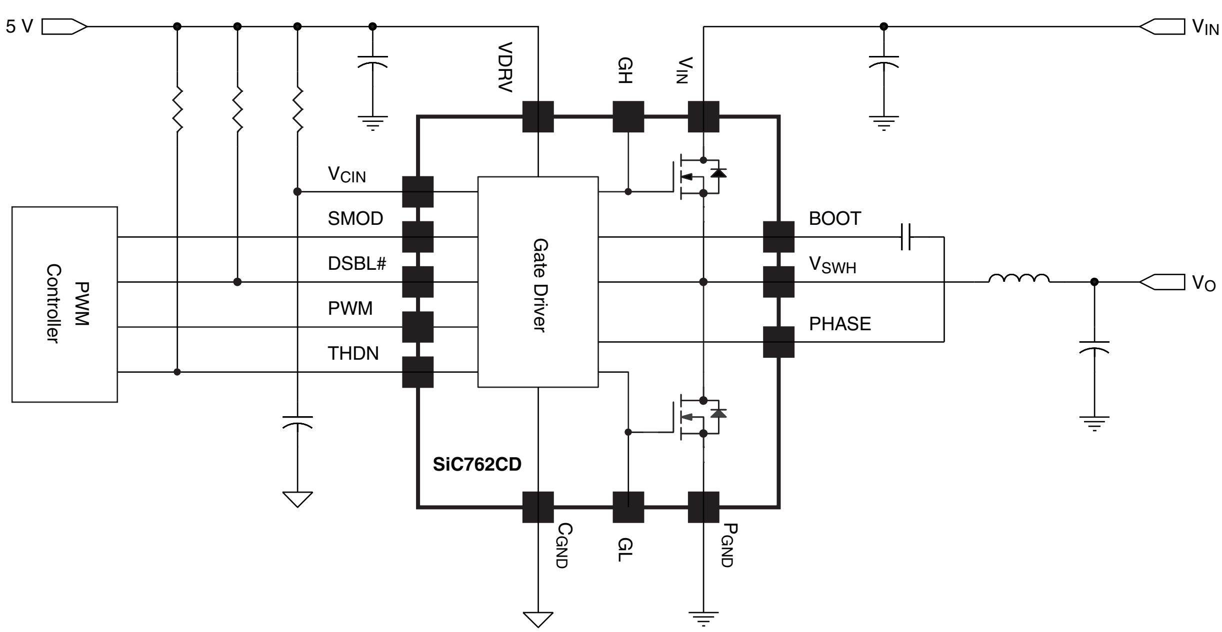

Figure 1

ORDERING INFORMATION	
Part Number	**Package**
SiC762CD-T1-GE3	PowerPAK MLP66-40
SiC762DB	Reference board

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**
Input Voltage	V_{IN}	- 0.3	30	V
Switch Node Voltage (DC)	V_{SW}	- 0.3	30	
Drive Input Voltage	V_{DRV}	- 0.3	7.0	
Control Input Voltage	V_{CIN}	- 0.3	7.0	
Logic Pins	V_{PWM}, $V_{DSBL\#}$, V_{THDN}, V_{SMOD}	- 0.3	V_{CIN} + 0.3	
Boot Voltage DC (referenced to C_{GND})	V_{BS}	- 0.3	33	
Boot to Phase Voltage DC	V_{BS_PH}	- 0.3	7	
Boot to Phase Voltage < 200 ns		- 0.3	9	
Ambient Temperature Range	T_A	- 40	125	°C
Maximum Junction Temperature	T_J		150	
Storage Junction Temperature	T_{STG}	- 65	150	
Soldering Peak Temperature			260	

Note:
a. T_A = 25 °C and all voltages referenced to P_{GND} = C_{GND} unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS					
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Voltage	V_{IN}	3.0	12	24	V
Control Input Voltage	V_{CIN}	4.5		5.5	
Drive Input Voltage	V_{DRV}	4.5		5.5	
Switch Node	V_{SW_DC}		12	24	

Note:
a. Recommended operating conditions are specified over the entire temperature range, and all voltages referenced to P_{GND} = C_{GND} unless otherwise noted.

THERMAL RESISTANCE RATINGS				
Parameter	**Symbol**	**Typ.**	**Max.**	**Unit**
Maximum Power Dissipation at T_{PCB} = 25 °C	P_{D_25C}		25	W
Maximum Power Dissipation at T_{PCB} = 100 °C	P_{D_100C}		10	
Thermal Resistance from Junction to Top	$R_{th\_J\_TOP}$		15	°C/W
Thermal Resistance from Junction to PCB	$R_{th\_J\_PCB}$		5	

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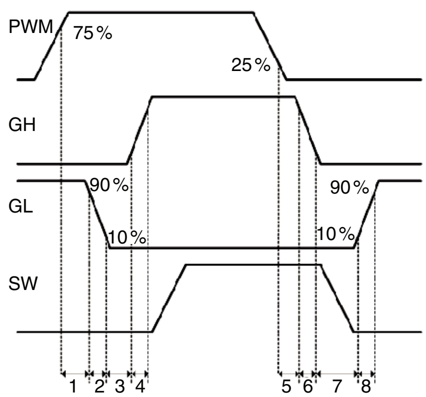
ELECTRICAL SPECIFICATIONS						
Parameter	Symbol	Test Conditions Unless Specified $V_{DSBL\#} = V_{SMOD} = 5$ V, $V_{IN} = 12$ V, $V_{VDRV} = V_{VCIN} = 5$ V, $T_A = 25$ °C	Min.	Typ.[a]	Max.	Unit
Power Supplies						
V_{CIN} Control Input Current	I_{VCIN}	$V_{DSBL\#} = 0$ V, no switching		21		µA
		$V_{DSBL\#} = 5$ V, no switching		350		
		$V_{DSBL\#} = 5$ V, $f_s = 300$ kHz, D = 0.1		500		
Drive Input Current (Dynamic)	I_{VDRV}	$f_s = 300$ kHz, D = 0.1		14	18	mA
		$f_s = 1000$ kHz, D = 0.1		40	54	
Bootstrap Supply						
Bootstrap Switch Forward Voltage	$V_{BS\ Diode}$	$V_{VCIN} = 5$ V, forward bias current 2 mA		0.60	0.75	V
Control Inputs (PWM, DSBL#, SMOD)						
PWM Rising Threshold	$V_{th\_pwm\_r}$		3.5	3.9	4.2	V
PWM Falling Threshold	$V_{th\_pwm\_f}$		0.8	1.0	1.2	
PWM Tristate Rising Threshold	$V_{th\_tri\_r}$		0.9	1.3	1.8	
PWM Tristate Falling Threshold	$V_{th\_tri\_f}$		3.4	3.7	4.0	
PWM Tristate Rising Threshold Hysteresis	$V_{hys\_tri\_r}$			280		mV
PWM Tristate Falling Threshold Hysteresis	$V_{hys\_tri\_f}$			180		
Tristate Hold-Off Time[b]	t_{TSHO}			150		ns
PWM Input Current	I_{PWM}	$V_{PWM} = 5$ V		250		µA
		$V_{PWM} = 0$ V		- 250		
SMOD, DSBL# Logic Input Voltage	V_{LOGIC_LH}	Rising (low to high)	2.0			V
	V_{LOGIC_LH}	Falling (high to low)			0.8	
Pull Down Impedance	R_{THDN}	5 kΩ resistor pull-up to V_{CIN}		40		Ω
THDN Output Low	V_{THDNL}			0.04		V
Protection						
Thermal Warning Flag Set				150		°C
Thermal Warning Flag Clear				135		
Thermal Warning Flag Hysteresis				15		
Under Voltage Lockout V_{CIN}	V_{UVLO}	Rising, on threshold		3.3	3.9	V
Under Voltage Lockout V_{CIN}		Falling, off threshold	2.3	2.95		
Under Voltage Lockout Hysteresis V_{CIN}	V_{UVLO_HYST}			400		mV
High Side Gate Discharge Resistor[b]	R_{HS_DSCRG}	$V_{VDRV} = V_{VCIN} = 0$ V; $V_{IN} = 12$ V		20.2		kΩ

Notes:
a. Typical limits are established by characterization and are not production tested.
b. Guaranteed by design.

TIMING SPECIFICATIONS						
Parameter	Symbol	Test Conditions Unless Specified $V_{VDRV} = V_{VCIN} = V_{DSBL\#} = 5$ V, $V_{VIN} = 12$ V, $T_A = 25$ °C	Min.	Typ.	Max.	Unit
Turn Off Propagation Delay High Side[a]	$t_{d\_off\_HS}$	25 % of PWM to 90 % of GH	10	20	35	ns
Rise Time High Side	t_{r_HS}	10 % to 90 % of GH		10		
Fall Time High Side	t_{f_HS}	90 % to 10 % of GH		8		
Turn Off Propagation Delay Low Side[a]	$t_{d\_off\_LS}$	75 % of PWM to 90 % of GL	10	37	45	
Rise Time Low Side	t_{r_LS}	10 % to 90 % of GL		6		
Fall Time Low Side	t_{f_LS}	90 % to 10 % of GL		5		
Dead Time Rising	t_{dead_on}	10 % of GL to 10 % of GH		27		
Dead Time Falling	t_{dead_off}	10 % of GH to 10 % of GL		19		

Note:
a. Min. and Max. are not 100 % production tested.

TIMING DEFINITIONS



Region	Definition	Symbol
1	Turn off propagation delay LS	$t_{d\_off\_LS}$
2	Fall time LS	t_{f_LS}
3	Dead time rising	t_{dead_on}
4	Rise time HS	t_{r_HS}
5	Turn off propagation delay HS	$t_{d\_off\_HS}$
6	Fall time HS	t_{f_HS}
7	Dead time falling	t_{dead_off}
8	Rise time LS	t_{r_LS}

Note:
GH is referenced to the high side source. GL is referenced to the low side source.

SIC762CD BLOCK DIAGRAM

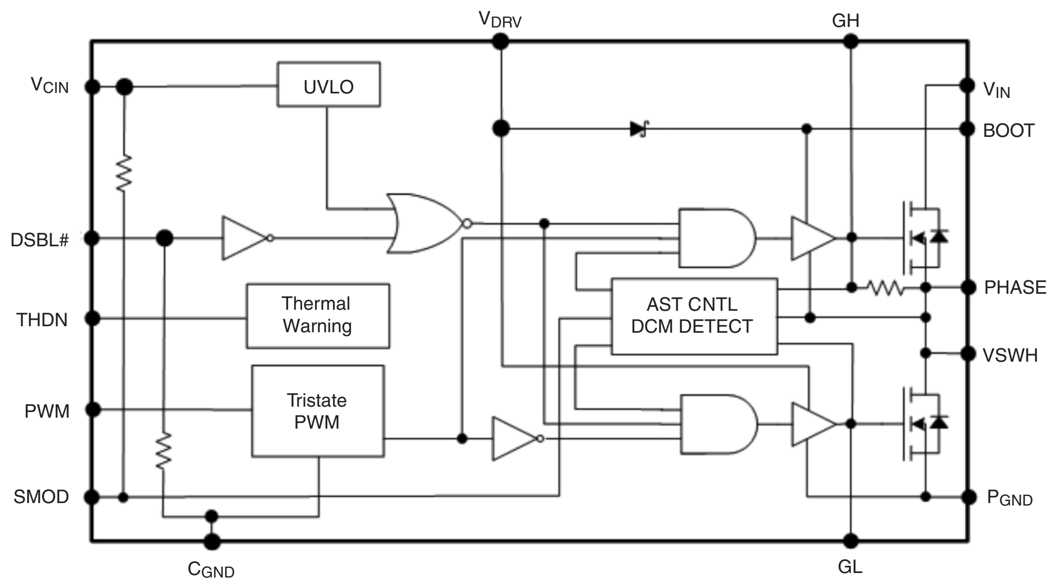


Figure 2

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tristate Function

The PWM input receives the PWM control signal from the V_R controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate Tristate logic (H, L and Tristate) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{th\_pwm\_r}$ the low side is turned off and the high side is turned on. When PWM input is driven below $V_{th\_pwm\_f}$ the high side turns off and the Low side turns on. For Tristate logic, the PWM input operates as above for driving the MOSFETs. However, there is an third state that is entered into as the PWM output of Tristate compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC762CD to pull the PWM input into the Tristate region (see the Tristate Voltage Threshold Diagram below). If the PWM input stays in this region for the Tristate Hold-Off Period, t_{TSHO}, both high side and low side MOSFETs are turned off. This function allows the V_R phase to be disabled without negative output voltage swing caused by inductor ringing and saves a Schottky diode clamp. The PWM and Tristate regions are separated by hysteresis to prevent false triggering. The SiC762CD incorporates PWM voltage thresholds that are compatible with 5 V logic.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFET. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to C_{GND} and shut down the IC.

Diode Emulation Mode (SMOD) Skip Mode

When SMOD pin is low the diode emulation mode is enabled. This is a non-synchronous conversion mode that improves light load efficiency by reducing switching losses. Conducted losses that occur in synchronous buck regulators when inductor current is negative are also reduced. Circuitry in the gate drive IC detects when inductor current crosses zero and automatically stops switching the low side MOSFET. See SMOD Operation Diagram for additional details. This function can also be used for a pre-biased output voltage. If SMOD is left unconnected, an internal pull up resistor will pull the pin up to V_{CIN} (Logic High) to disable the diode emulation function.

Thermal Shutdown Warning (THDN)

The THDN pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 kΩ to pull this pin up to V_{CIN}. An internal temperature sensor detects the junction temperature. The temperature threshold is 150 °C. When this junction temperature is exceeded the THDN flag is set. When the junction temperature drops below 135 °C the device will clear the THDN signal. The SiC762CD does not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side Power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The Switch node V_{SWH} is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the Printed Circuit Board should be such that the inductance separating the C_{GND} and P_{GND} should be a minimum. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV},V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gate drive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

Shoot-Through Protection and Adaptive Dead Time (AST)

The SiC762CD has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. When PWM input goes high the LS gate starts to go low after a few ns. When this signal crosses through 1.7 V the logic to switch the HS gate on is activated. When PWM goes low the HS gate goes low. When the HS gate-to-source drive signal crosses through 1.7 V the logic to turn on the LS gate is activated. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC762CD also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

DEVICE TRUTH TABLE

DSBL#	SMOD	PWM	GH	GL
Open	X	X	L	L
L	X	X	L	L
H	L	L	L	H ($I_L > 0$), L ($I_L \leq 0$)
H	L	H	H	L
H	H	H	H	L
H	H	L	L	H

TRISTATE PWM VOLTAGE THRESHOLD DIAGRAM

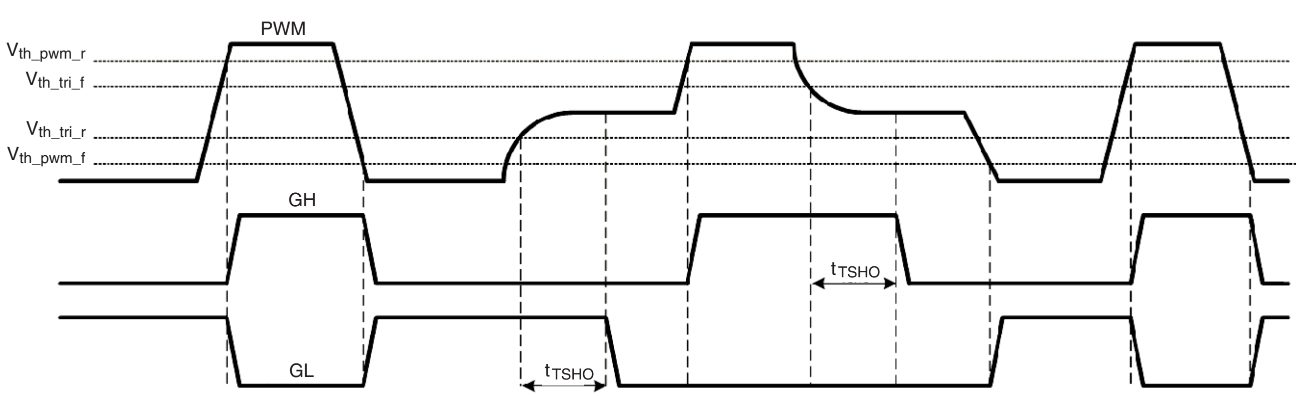


Figure 3

SMOD OPERATION DIAGRAM

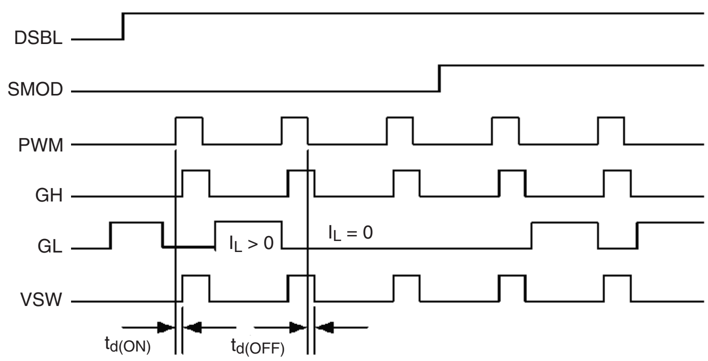


Figure 4

PIN CONFIGURATION

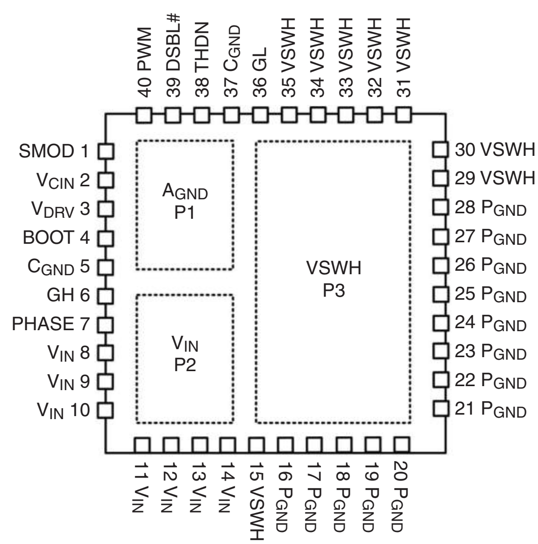
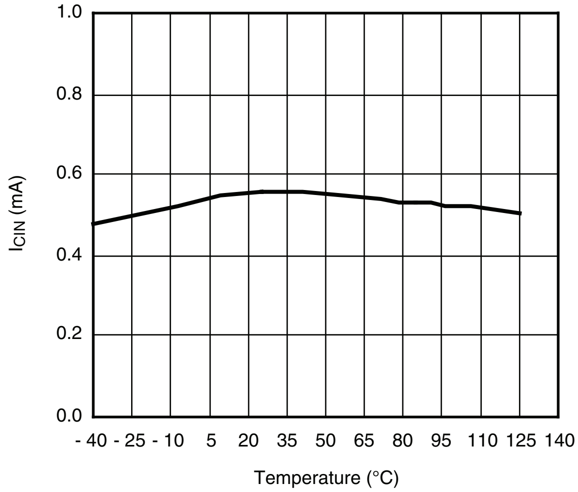


Figure 5 - PowerPAK MLP 6 x 6 40P Pin Out - Top View

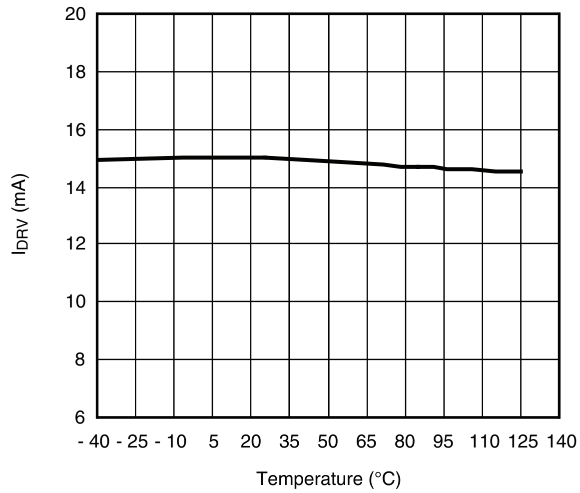
PIN DESCRIPTION

Pin Number	Symbol	Description
1	SMOD	Disable low side gate operation. Active low.
2	V_{CIN}	This will be the bias supply input for control IC (5 V).
3	V_{DRV}	IC bias supply and gate drive supply voltage (5 V).
4	BOOT	High side driver bootstrap voltage pin for external bootstrap capacitor.
5, 37, PAD1	C_{GND}	Control signal ground. It should be connected to P_{GND} externally. All pins internally connected.
6	GH	Gate signal output pin for high side MOSFET. Pin for monitoring.
7	PHASE	Return pin for the HS bootstrap capacitor. Connect a 0.1 µF ceramic capacitor from this pin to the boot pin (4).
8 to 14, PAD2	V_{IN}	Input voltage for power stage. It is the drain of the high-side MOSFET.
15, 29 to 35, PAD3	VSWH	It is the phase node between high side MOSFET source and low side MOSFET drain. It should be connected to an output inductor. All pins internally connected.
16 to 28	P_{GND}	Power ground.
36	GL	Gate signal output pin for low side MOSFET. Pin for monitoring.
38	THDN	Thermal shutdown open drain output. Use a 10K pull up resistor to V_{CIN}.
39	DSBL#	Disable pin. Active low.
40	PWM	PWM input logic signal. Compatible with Tristate controller function.

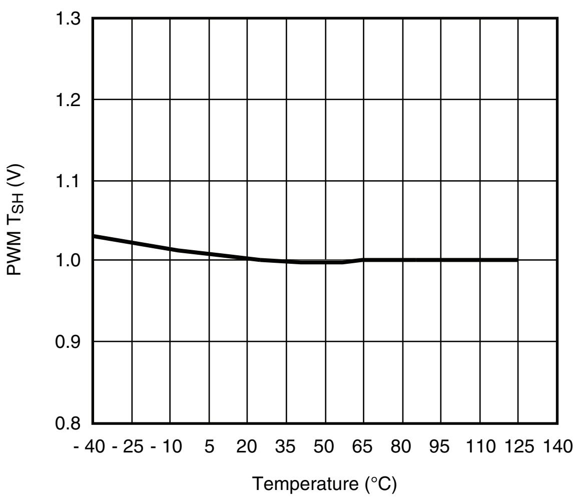
ELECTRICAL CHARACTERISTICS



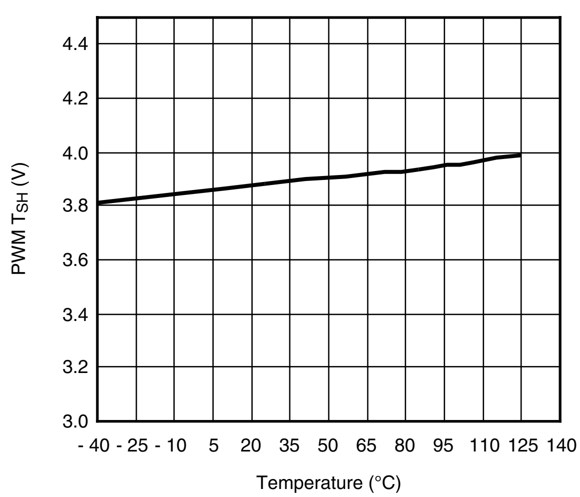
I_{CIN} (mA) vs. Temperature at Frequency = 300 kHz
D = 10 %, V_{CIN} = V_{DRV} = 5 V



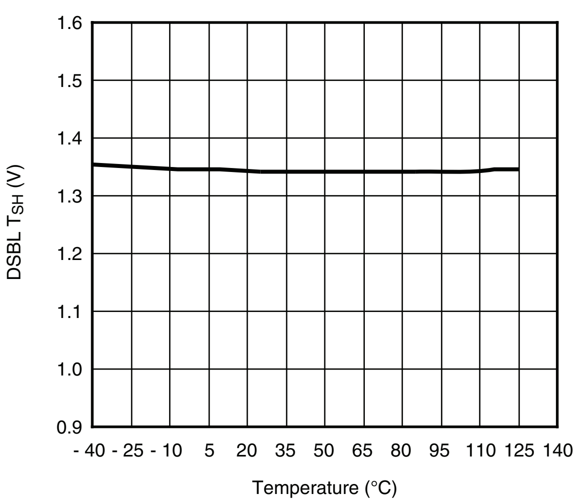
I_{DRV} (mA) vs. Temperature at Frequency = 300 kHz
D = 10 %, V_{CIN} = V_{DRV} = 5 V



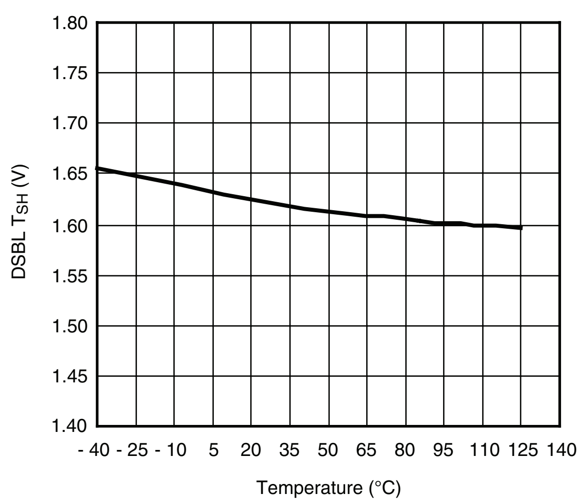
PWM Falling Threshold (V) vs. Temperature (°C)
V_{CIN} = V_{DRV} = 5 V



PWM Rising Threshold (V) vs. Temperature (°C)
V_{CIN} = V_{DRV} = 5 V

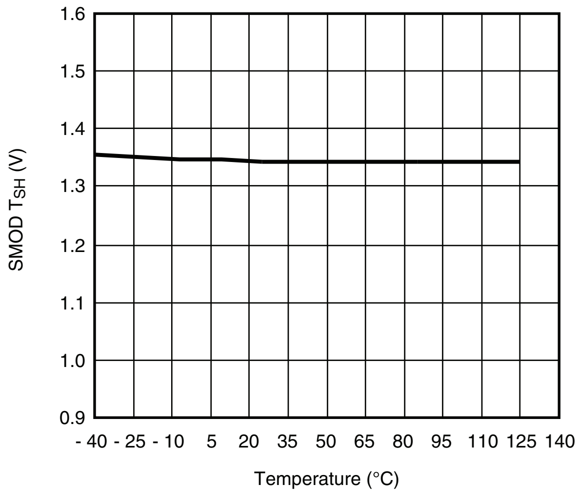


DSBL Falling Threshold (V) vs. Temperature (°C)
V_{CIN} = V_{DRV} = 5 V

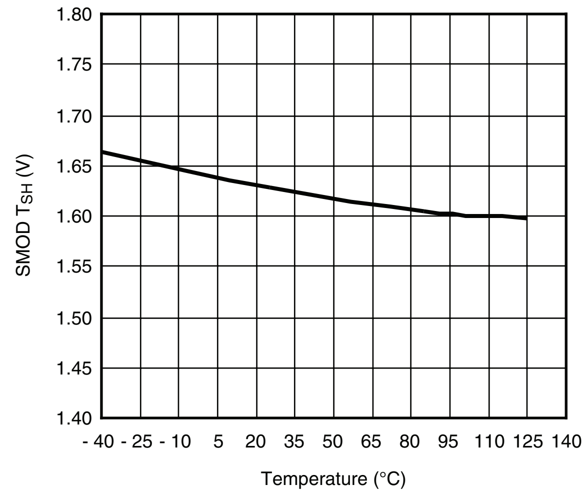


DSBL Rising Threshold (V) vs. Temperature (°C)
V_{CIN} = V_{DRV} = 5 V

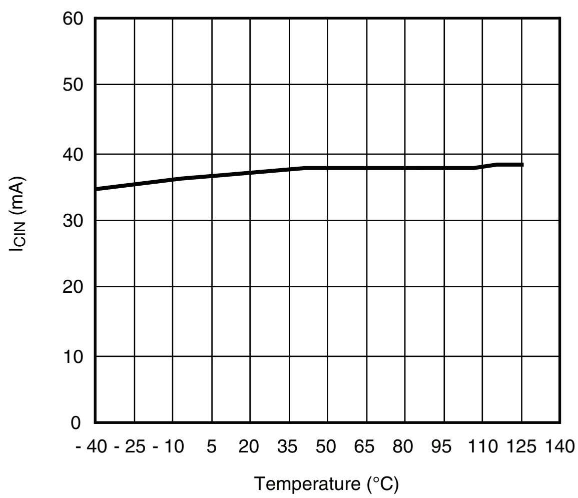
ELECTRICAL CHARACTERISTICS



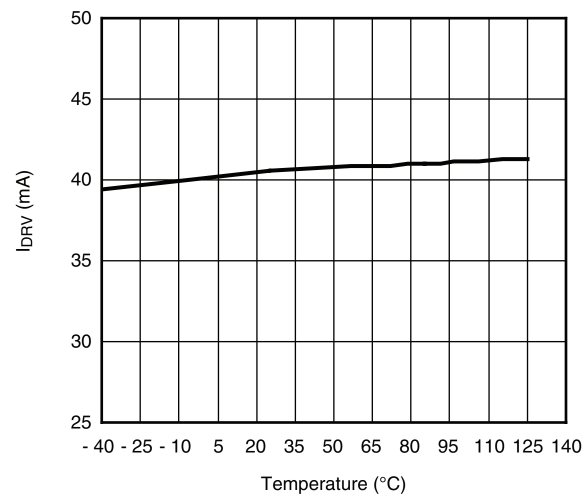
SMOD Falling Threshold (V) vs. Temperature (°C)
$V_{CIN} = V_{DRV} = 5$ V



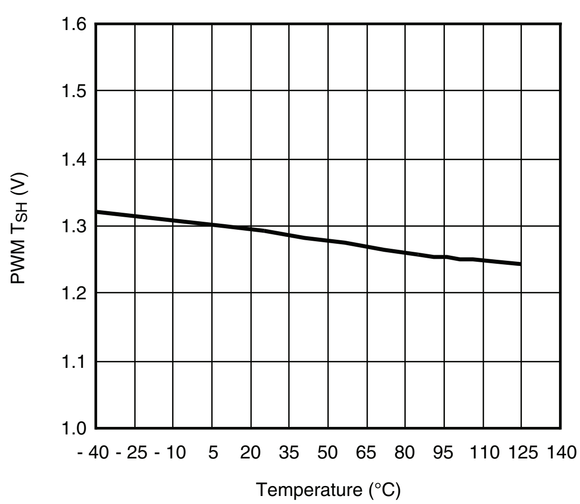
SMOD Rising Threshold (V) vs. Temperature (°C)
$V_{CIN} = V_{DRV} = 5$ V



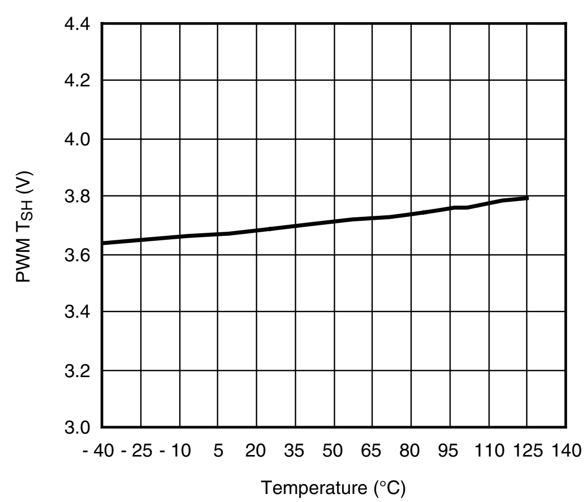
$I_{CIN} + I_{DRV}$ (mA) vs. Temperature at Frequency = 1 MHz
D = 10 %, $V_{CIN} = V_{DRV} = 5$ V



I_{DRV} (mA) vs. Temperature at Frequency = 1 MHz
D = 10 %, $V_{CIN} = V_{DRV} = 5$ V

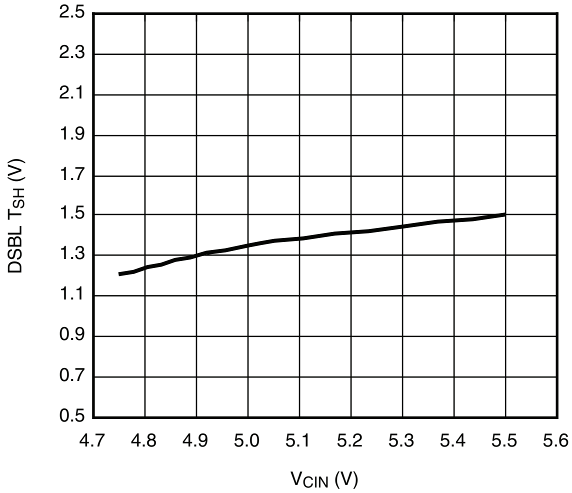


PWM Falling Tristate (V) vs. Temperature (°C)
$V_{CIN} = V_{DRV} = 5$ V

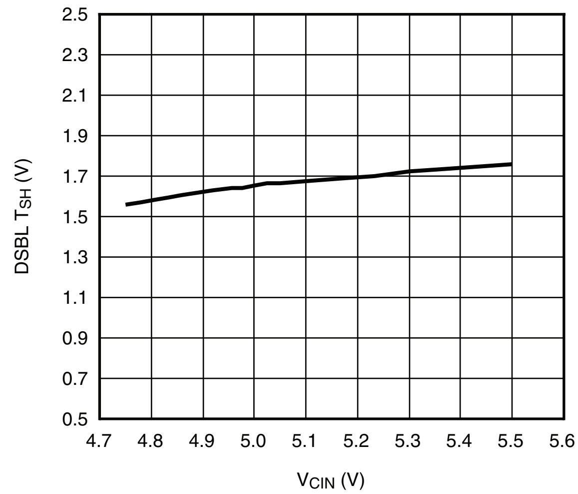


PWM Rising Tristate Threshold (V) vs. Temperature (°C)
$V_{CIN} = V_{DRV} = 5$ V

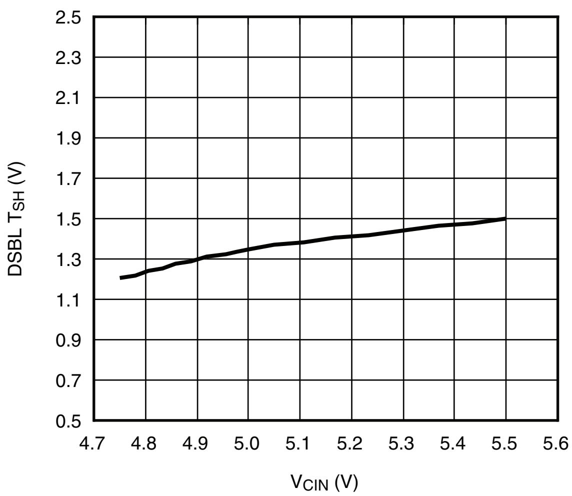
ELECTRICAL CHARACTERISTICS



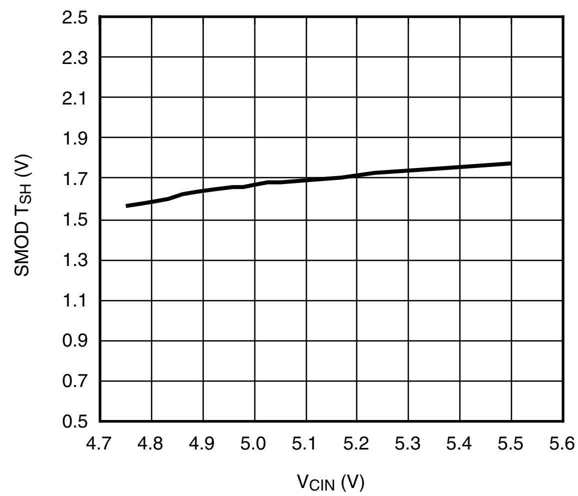
DSBL Falling Threshold vs. V_{CIN}



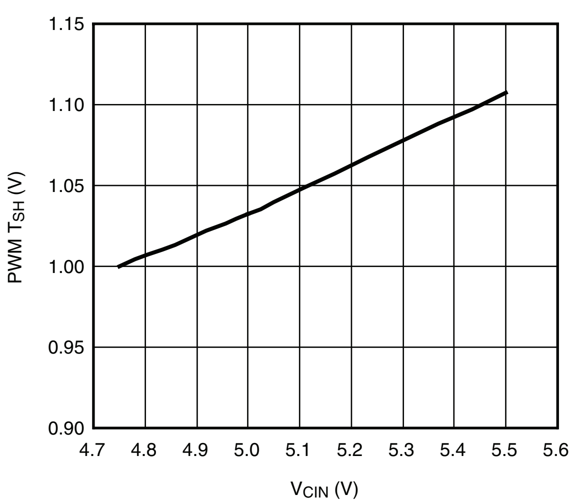
DSBL Rising Threshold vs. V_{CIN}



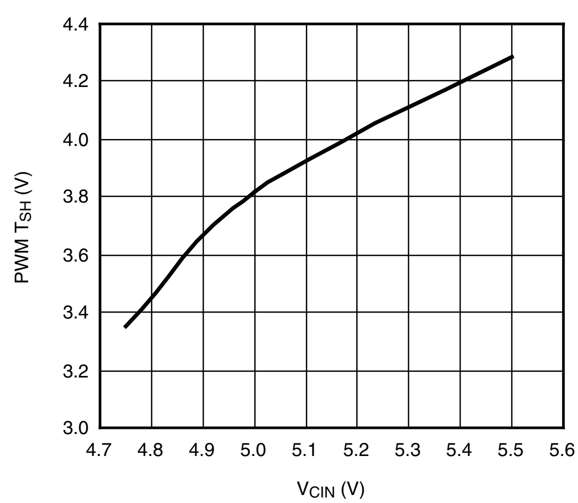
SMOD Falling Threshold vs. V_{CIN}



SMOD Rising Threshold vs. V_{CIN}

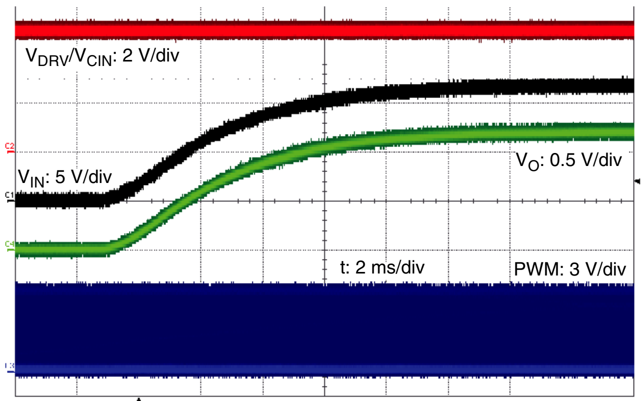


PWM Falling Threshold vs. V_{CIN}

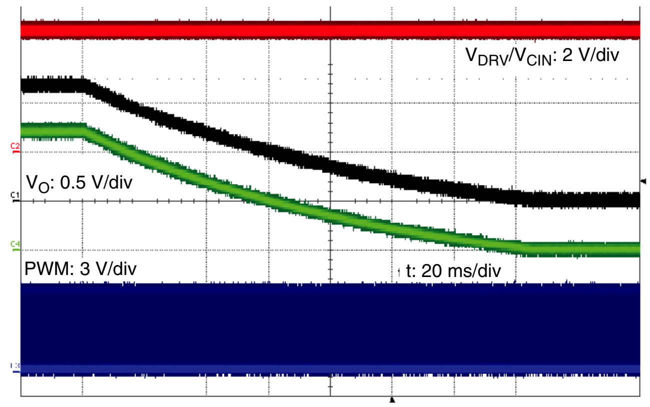


PWM Rising Threshold vs. V_{CIN}

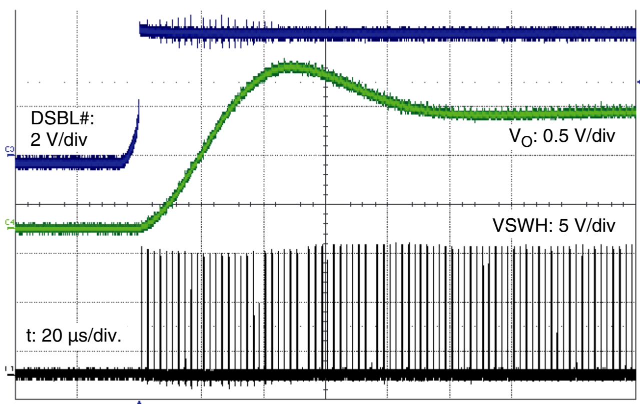
ELECTRICAL CHARACTERISTICS



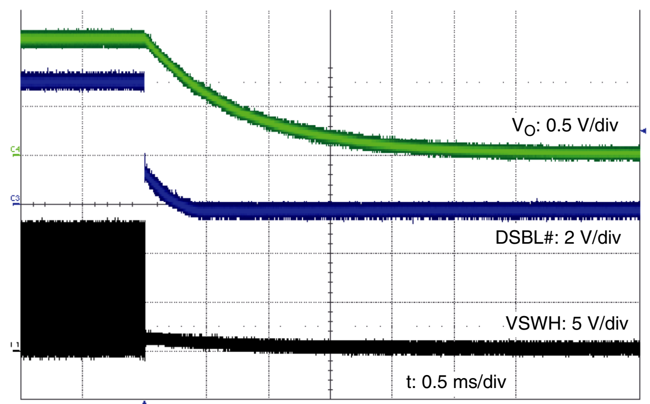
Startup with V_{IN} ramping up
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz



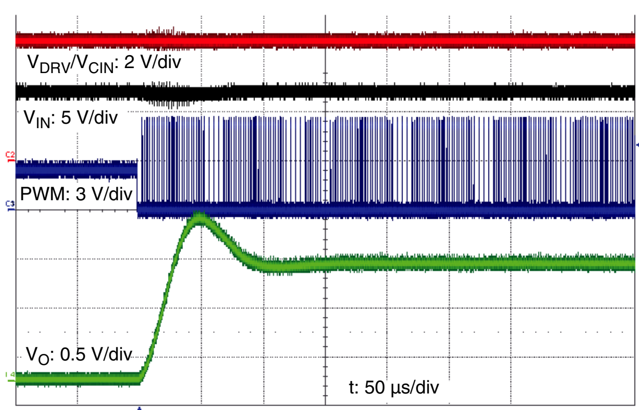
Power Off with V_{IN} ramping down
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz



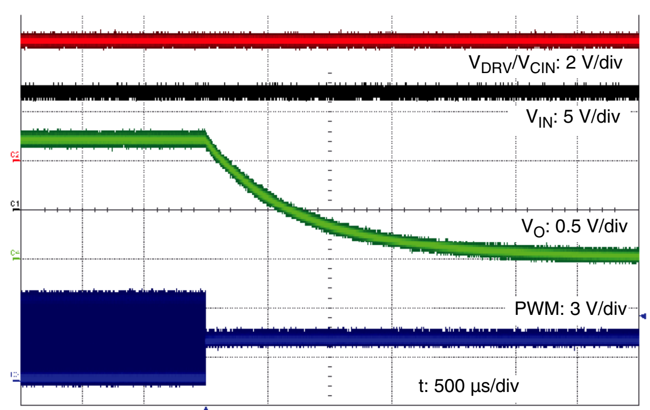
Enable with V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz



Disable with V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz

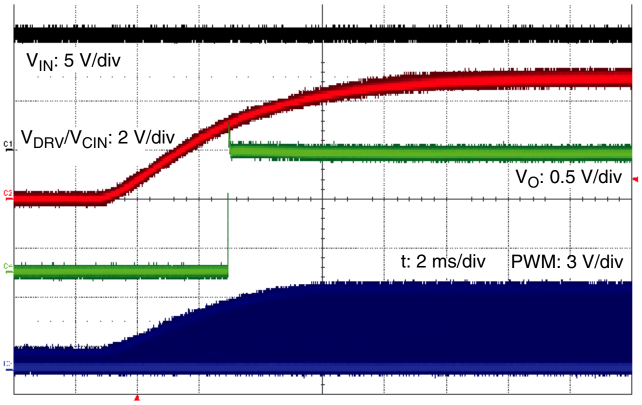


PWM Start with V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz

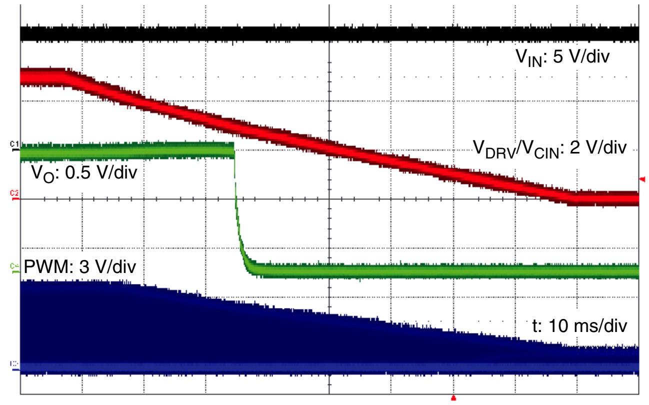


PWM Turn-off with V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz

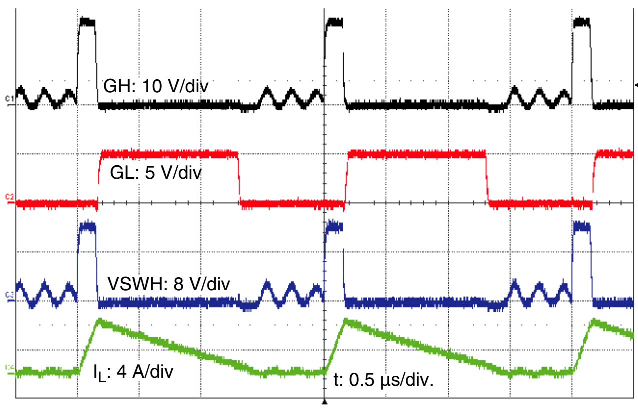
ELECTRICAL CHARACTERISTICS



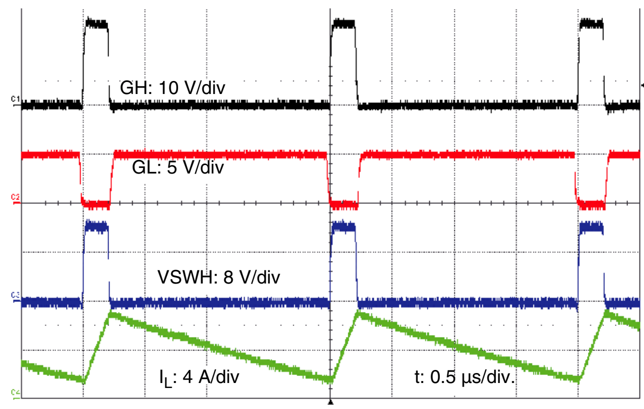
Startup with V_{DRV}/V_{CIN} ramping up
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz



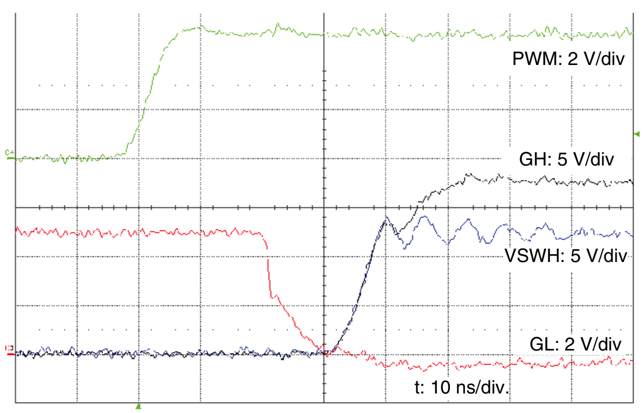
Power Off with V_{DRV}/V_{CIN} ramping down
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz



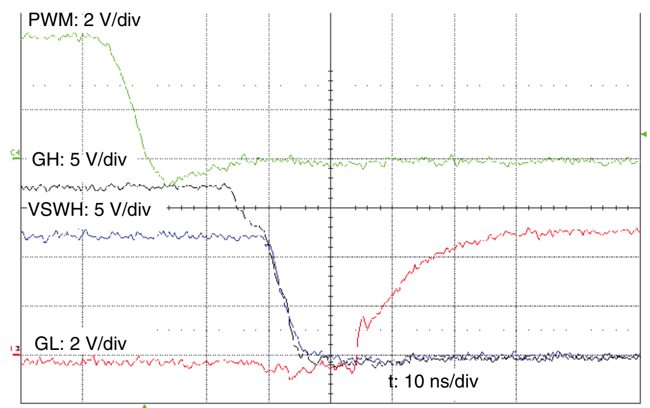
Switching Waveforms with SMOD enabled
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz, I_{OUT} = 1.5 A



Switching Waveforms with SMOD disabled
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz, I_{OUT} = 4 A

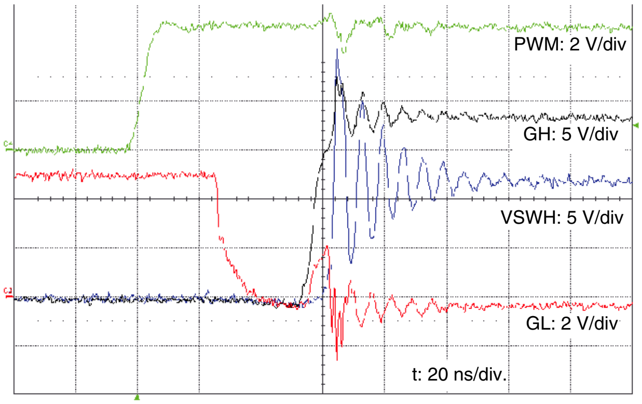


Switching Waveforms at PWM rising edge
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz, I_{OUT} = 0 A

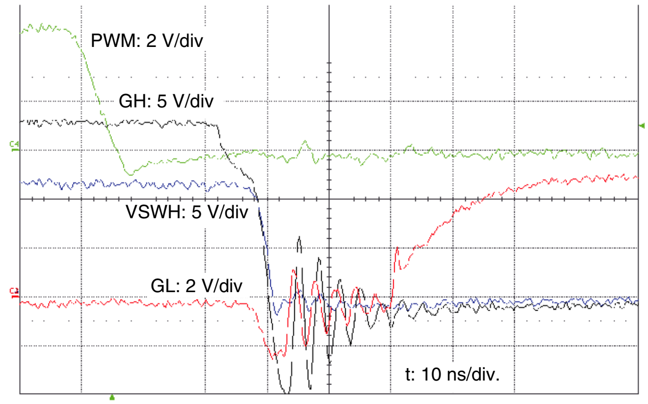


Switching Waveforms at PWM falling edge
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz, I_{OUT} = 0 A

ELECTRICAL CHARACTERISTICS

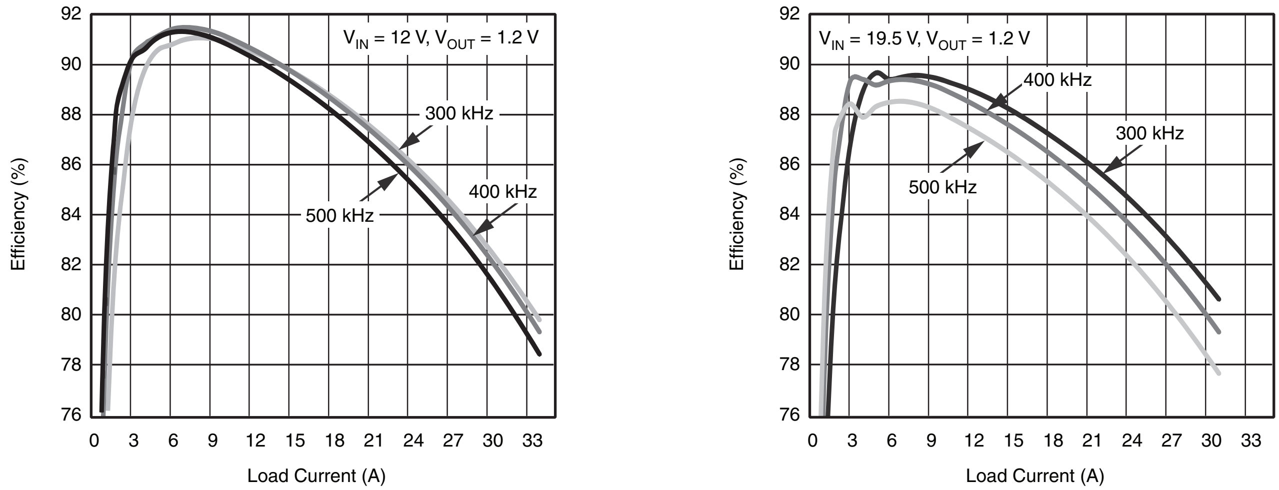


Switching Waveforms at PWM rising edge
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz, I_{OUT} = 30 A



Switching Waveforms at PWM falling edge
V_{IN} = 12 V, V_{OUT} = 1.2 V, F_S = 500 kHz, I_{OUT} = 30 A

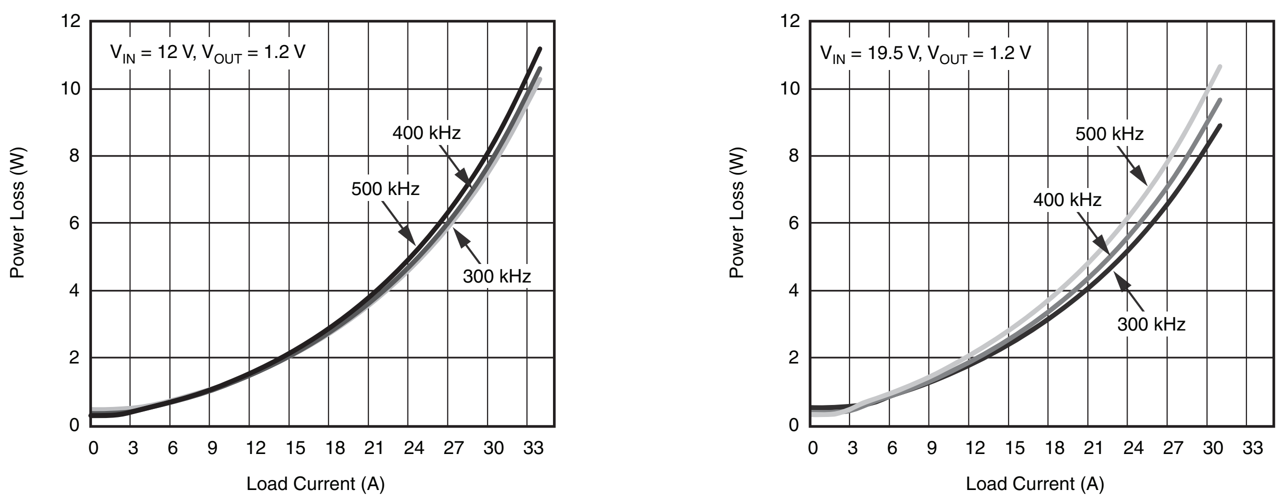
TYPICAL SYSTEM EFFICIENCY WITH SIC762CD



V_{IN} = 12 V and 19.5 V, V_{OUT} = 1.2 V, V_{DRV} = V_{CIN} = 5 V; No Air Flow
IHLP5050FDERR33M01 Inductor
L = 330 nH, DER = 0.83 mΩ

Figure 6 - System Efficiency with SiC762

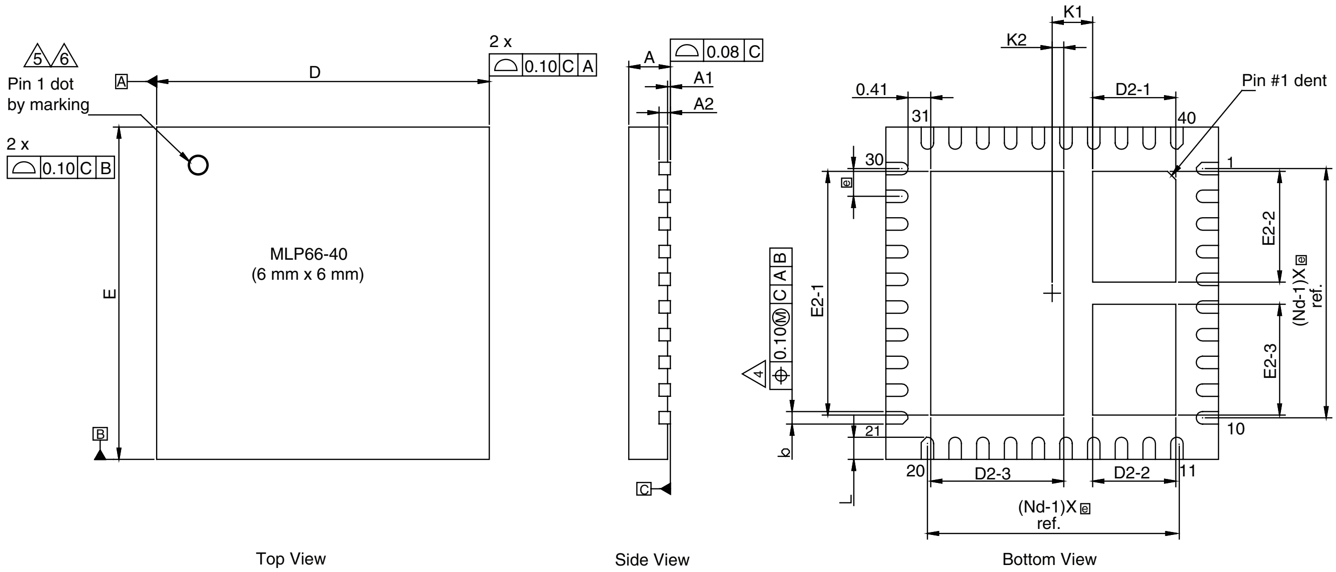
TYPICAL SYSTEM POWER LOSS WITH SIC762CD



V_{IN} = 12 V and 19.5 V, V_{OUT} = 1.2 V, V_{DRV} = V_{CIN} = 5 V; No Air Flow
IHLP5050FDERR33M01 Inductor
L = 330 nH, DER = 0.83 mΩ

Figure 7 - System Power Loss with SiC762

PACKAGE DIMENSIONS



DIM	MILLIMETERS			INCHES		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A(8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b(4)	0.20	0.25	0.30	0.078	0.098	0.011
D	6.00 BSC			0.236 BSC		
e	0.50 BSC			0.019 BSC		
E	6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N(3)	40			40		
Nd(3)	10			10		
Ne(3)	10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1	0.73 BSC			0.028 BSC		
K2	0.21 BSC			0.008 BSC		

Notes:
1. Use millimeters as the primary measurement.
2. Dimensioning and tolerances conform to ASME Y14.5M-1994.
3. N is the number of terminals.
   Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction .

4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body .
6. Exact shape and size of this feature is optional.
7. Package warpage max. 0.08 mm.
8. Applied only for terminals.

Figure 8 - PowerPAK MLP 66-40

LAND PATTERN DIMENSIONS

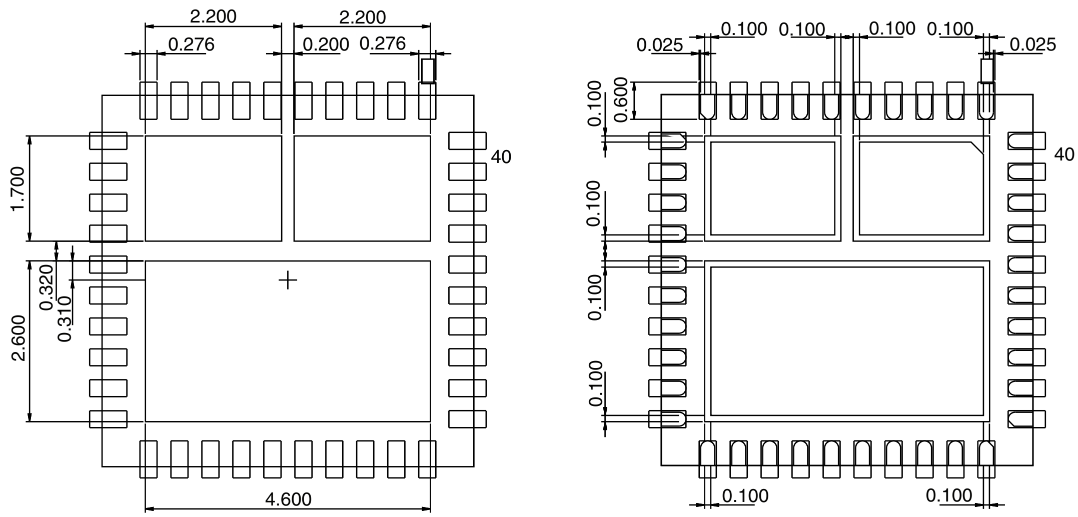
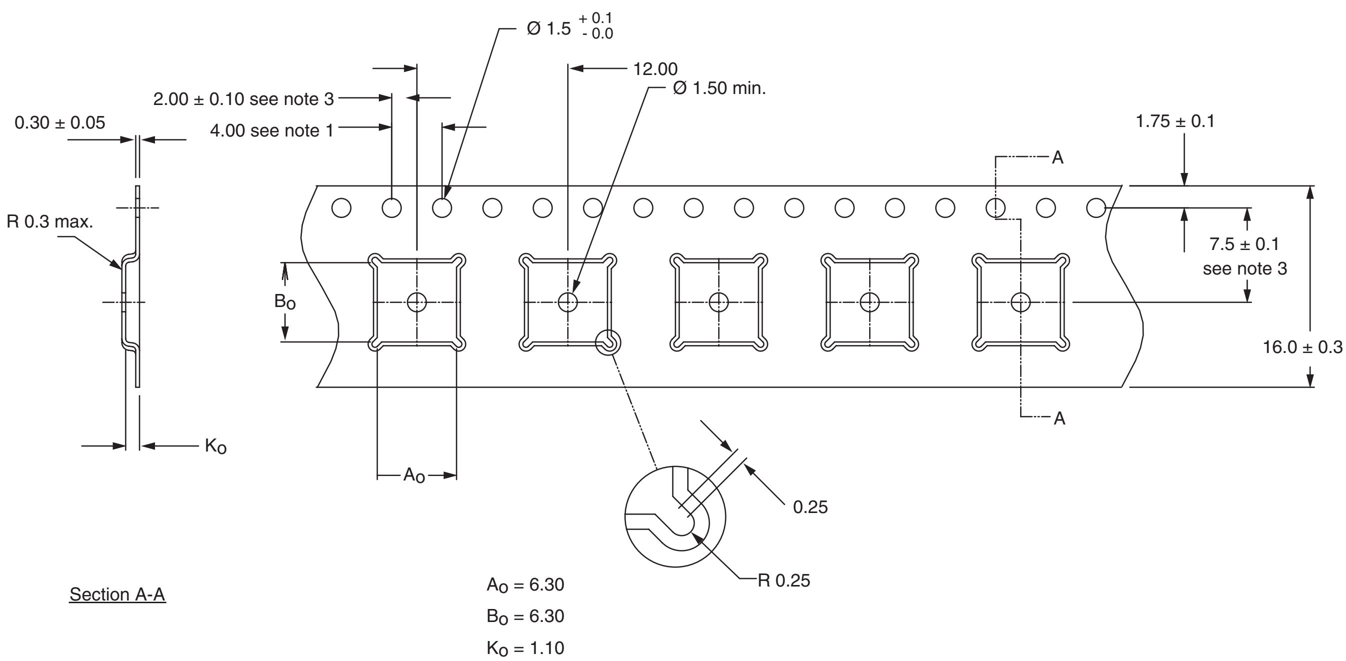


Figure 9 - PowerPAK MLP 66-40

TAPE AND REEL CARRIER TAPE DIMENSIONS

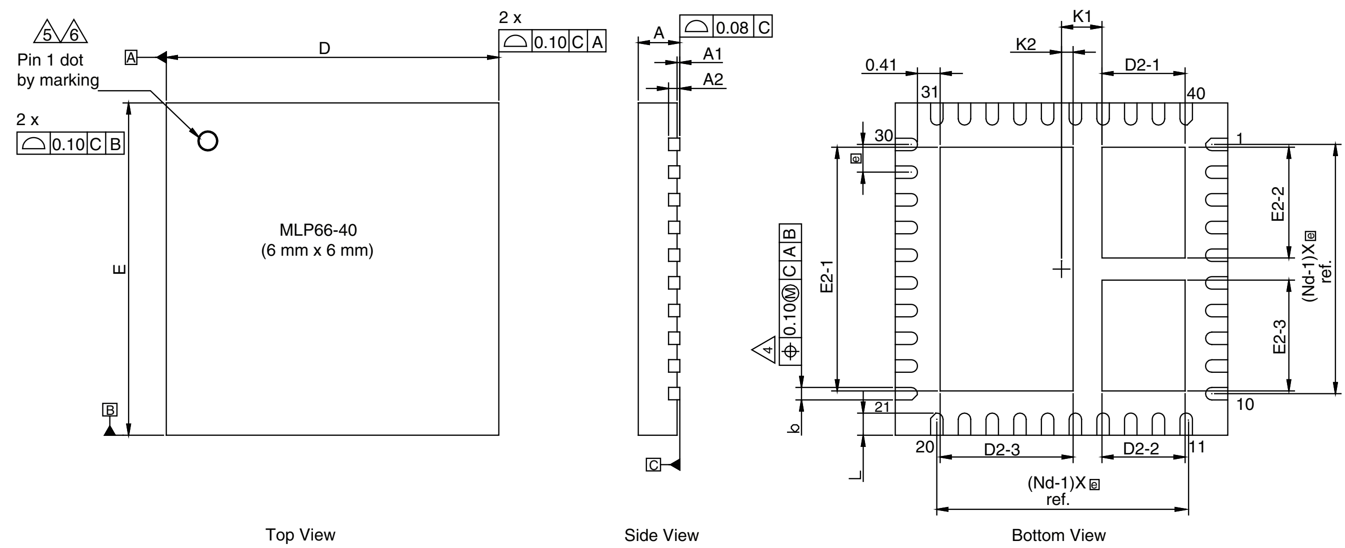


Notes:
1. 10 sprocket hole pitch cumulative tolerance ± 0.2.
2. Camber in compliance with EIA 481.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Figure 10 - PowerPAK MLP 66-40

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?65727.

PowerPAK® MLP66-40 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b (4)	0.20	0.25	0.30	0.078	0.098	0.011
D	6.00 BSC			0.236 BSC		
e	0.50 BSC			0.019 BSC		
E	6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)	40			40		
Nd (3)	10			10		
Ne (3)	10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1	0.73 BSC			0.028 BSC		
K2	0.21 BSC			0.008 BSC		
ECN: T14-0826-Rev. B, 12-Jan-15 DWG: 5986						

Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals. Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

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