DrMOS Integrated Power Stage

DESCRIPTION

The SiC770 is an integrated power stage solution optimized for synchronous buck applications to offer high current, high efficiency and high power density performance. Packaged in Vishay's proprietary 6 mm x 6 mm MLP package, SiC770 enables voltage regulator design to deliver in excess of 40 A per phase current.

The internal power MOSFETs utilizes Vishay's state-of-the-art TrenchFET Gen IV technology that delivers industry bench-mark performance to significantly reduce switching and conduction losses.

The SiC770 incorporates an advanced MOSFET gate driver IC that features high current driving capability, adaptive dead-time control, and integrated bootstrap Schottky diode, a thermal warning (THWn) alerts the system of excessive junction temperature. This driver is also compatible with wide range of PWM controllers with the support of tri-state PWM, 5 V PWM logic, and skip mode (ZCD) for improve light load efficiency.

FEATURES

- Industry benchmark MOSFET with integrated Schottky diode
- Delivers in excess of 40 A continuous current
- 91 % peak efficiency
- High frequency operation up to 1 MHz
- Power MOSFETs optimized for 19 V input stage
- 5 V PWM logic with tri-state and hold-off
- Automatic skip mode operation (ZCD) for light load efficiency
- Built-in bootstrap Schottky diode
- Thermal monitor flag
- V_{CIN} under voltage lockout
- Compliant with Intel DrMOS 4.0 specification
- Thermally enhanced PowerPAK® MLP6x6-40L package
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous buck converters
- Muliti-phase VRDs for CPU, GPU and memory
- DC/DC POL modules

TYPICAL APPLICATION DIAGRAM

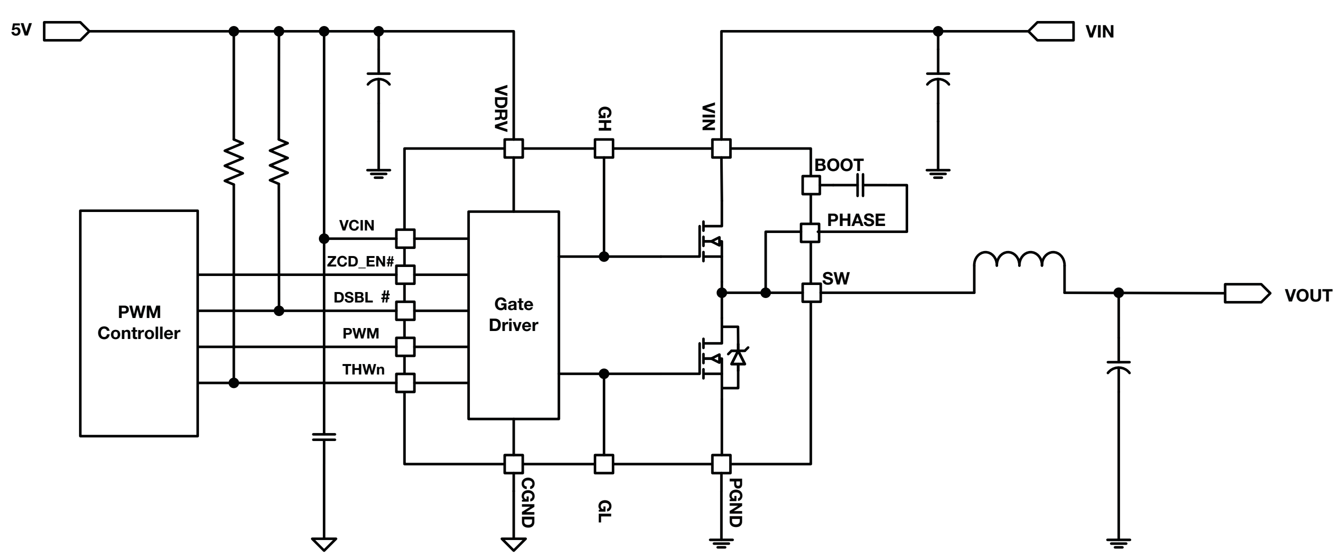


Fig. 1 - SiC770 Typical Application Diagram

PINOUT CONFIGURATION

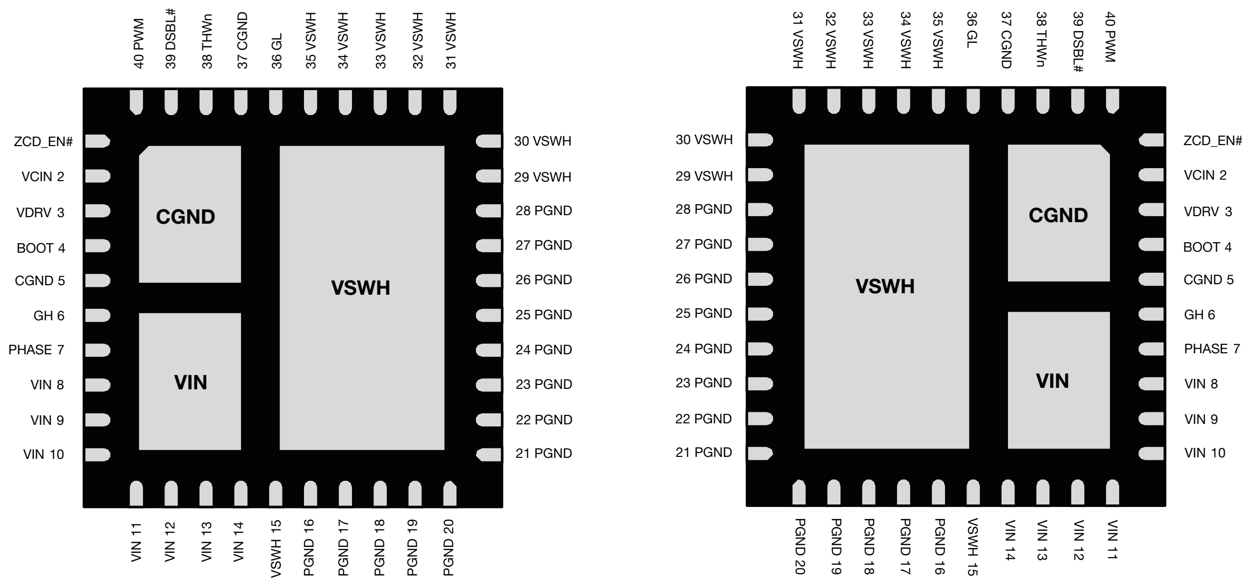


Fig. 2 - SiC770 Pin Configuration

PIN DESCRIPTION		
PIN#	**NAME**	**FUNCTION**
1	ZCD_EN#	LS FET turn-off logic; active low
2	V_{CIN}	Supply voltage for internal logic circuitry
3	V_{DRV}	Supply voltage for internal gate driver
4	BOOT	High side driver bootstrap voltage
5, 37, P1	C_{GND}	Analog ground for the driver IC
6	GH	High side gate signal
7	PHASE	Return path of HS gate driver
8 to 14, P2	V_{IN}	Power stage input voltage. Drain of high side MOSFET
15, 29 to 35, P3	V_{SWH}	Phase node of the power stage
16 to 28	P_{GND}	Power ground
36	GL	Low side gate signal
38	THWn	Thermal warning open drain output
39	DSBL#	Disable pin; active low
40	PWM	PWM input logic

ORDERING INFORMATION		
PART NUMBER	**PACKAGE**	**MARKING CODE**
SiC770CD-T1-GE3	PowerPAK MLP66-40L	SiC770CD
SiC770DB	Reference Board	

ABSOLUTE MAXIMUM RATINGS			
ELECTRICAL PARAMETER	**SYMBOL**	**LIMITS**	**UNIT**
Input Voltage	V_{IN}	- 0.3 to 30	V
Control Input Voltage	V_{CIN}	- 0.3 to 7	V
Drive Input Voltage	V_{DRV}	- 0.3 to 7	V
Switch Node (DC)	V_{SW}	- 0.3 to 30	V
Switch Node (AC) [1]		- 8 to 35	V
Boot Voltage (DC Voltage)	V_{BS}	- 0.3 to 32	V
Boot to Switching Node (DC Voltage)	VBS_SW	- 0.3 to 7	V
All Logic Inputs and Outputs (PWM, DSBL, SMOD, and THDN)		- 0.3 to V_{CIN} + 0.3	V
Max. Operating Junction Temperature	T_J	150	°C
Ambient Temperature	T_A	- 40 to 125	°C
Storage Temperature		- 65 to 150	°C

Notes

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) The specification values indicated “AC” is VSW to PGND - 8 V (< 20 ns, 10 µJ), minimum and 35 V (< 50 ns), maximum.

RECOMMENDED OPERATING RANGE				
ELECTRICAL	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Input Voltage (V_{IN})	4.5		24	V
Drive Input Voltage (V_{DRV})	4.5	5	5.5	V
Control Input Voltage (V_{CIN})	4.5	5	5.5	V
Switching Node (LX, DC Voltage)			27	V
BOOT-SW	4	4.5	5.5	V
THERMAL RESISTANCE				
Thermal Resistance from Junction to Case (to P3 PAD “VSWH”)		2.5		°C/W
Thermal Resistance from Junction to PCB		5		°C/W

ELECTRICAL SPECIFICATIONS (DSBL# = 5 V, SMOD = 5 V, V_{IN} = 19 V, V_{DRV} and V_{CIN} = 5 V, T_A = 25 °C)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS SPECIFIED**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
POWER SUPPLIES						
Control Logic Input Current	I_{VCIN}	$V_{DSBL\#}$ = 0 V, no switching		21		µA
		$V_{DSBL\#}$ = 5 V, no switching		350		
		$V_{DSBL\#}$ = 5 V, f_S = 300 kHz, D = 0.1		500		
Drive Input Current (Dynamic)	I_{VDRV}	f_S = 300 kHz, D = 0.1		14		mA
		f_S = 1 MHz, D = 0.1		40		
BOOTSTRAP SUPPLY						
Bootstrap Switch Forward Voltage	V_F	V_{CIN} = 5 V, forward bias current 2 mA		0.6		V
PWM CONTROL INPUT						
Rising Threshold	PWM_{TH_R}		3.5	3.9	4.2	V
Falling Threshold	$PWMT_{H\_F}$		0.8	1.0	1.2	V
Tri-state Voltage	V_{TRI}	PWM pin floating		2.3		V
Tri-state Rising Threshold	$V_{TRI\_TH\_R}$		0.9	1.3	1.8	V
Tri-state Falling Threshold	$V_{TRI\_TH\_F}$		3.4	3.7	4.0	V
Tri-state Rising Threshold Hysteresis	$V_{TRI\_HYS\_R}$			280		mV
Tri-state Falling Threshold Hysteresis	$V_{TRI\_HYS\_F}$			180		mV
PWM Input Current	I_{PWM}	V_{PWM} = 5 V		250		µA
		V_{PWM} = 0 V		- 250		
TIMING SPECIFICATIONS						
Tri-state to GH/GL Rising Propagation Delay	$T_{PD\_R\_Tri}$	No load, see fig. 4		20		ns
Tri-state Hold-Off Time	T_{TSHO}			150		ns
GH - Turn Off Propagation Delay	$T_{PD\_OFF\_GH}$			20		ns
GH - Turn ON Propagation Delay (Dead Time Rising)	$T_{PD\_ON\_GH}$			15		ns
GL - Turn Off Propagation Delay	$T_{PD\_OFF\_GL}$			20		ns
GL - Turn ON Propagation Delay (Dead Time Falling)	$T_{PD\_ON\_GL}$			20		ns
DSBL# Hi to GH/GL Rising Propagation Delay	$T_{PD\_R\_DSBL}$			500		ns
DSBL# Lo to GH/GL Falling Propagation Delay	$T_{PD\_F\_DSBL}$			200		ns
DSBL# , ZCD_EN# INPUT						
DSBL# Logic Input Voltage	V_{DSBL}	Enable	2			V
		Disenable			0.8	
ZCD_EN# Logic Input Voltage	V_{SMOD}	High State	2			V
		Low State			0.8	
PROTECTION						
Under Voltage Lockout	V_{UVLO}	Rising, On Threshold		3.3	3.9	V
		Falling, Off Threshold	2.3	2.95		
Under Voltage Lockout Hysteresis				400		mV
THWn Flag Set[(2)]		(2)		160		°C
THWn Flag Clear[(2)]				135		°C
THWn Flag Hysteresis[(2)]				25		°C
THWn Output Low				0.02		V

Notes
(1) Typical limits are established by characterization and are not production tested.
(2) Guaranteed by design.
(3) Min. and max. parameters are not 100 % production tested.

DETAILED OPERATIONAL DESCRIPTION

PWM Input with Tri-State Function

The PWM input receives the PWM control signal from the VR controller IC. The PWM input is designed to be compatible with standard controllers using two state logic (H and L) and advanced controllers that incorporate tri-state logic (H, L, and tri-state) on the PWM output. For two state logic, the PWM input operates as follows. When PWM is driven above $V_{th\_pwm\_r}$ the low side is turned OFF and the high side is turned ON. When PWM input is driven below $V_{th\_pwm\_f}$ the high side turns off and the low side turns on. For tri-state logic, the PWM input operates as above for driving the MOSFETs. However, there is an third state that is entered into as the PWM output of tri-state compatible controller enters its high impedance state during shut-down. The high impedance state of the controller's PWM output allows the SiC770 to pull the PWM input into the tri-state region (see the tri-state Voltage Threshold diagram below). If the PWM input stays in this region for the tri-state hold-off period, t_{TSHO}, both high side and low side MOSFETs are turned off. This function allows the VR phase to be disabled without negative output voltage swing caused by inductor ringing and saves a schottky diode clamp. The PWM and tri-state regions are separated by hysteresis to prevent false triggering. The SiC770CD incorporates PWM voltage thresholds that are compatible with 5 V logic.

Disable (DSBL#)

In the low state, the DSBL# pin shuts down the driver IC and disables both high-side and low-side MOSFET. In this state, the standby current is minimized. If DSBL# is left unconnected an internal pull-down resistor will pull the pin down to CGND and shut down the IC.

Diode Emulation Mode (ZCD_EN#) Skip

When ZCD_EN# pin is low the diode emulation mode is enabled. This is a non-synchronous conversion mode that improves light load efficiency by reducing switching losses. Conducted losses that occur in synchronous buck regulators when inductor current is negative are also reduced. Circuitry in the gate drive IC detects the inductor valley current when inductor current crosses zero and automatically stops switching the low side MOSFET. See ZCD_EN# operation diagram for additional details. This function can be also be used for a pre-biased output voltage. If ZCD_EN# is left un-connected, an internal pull up resistor will pull the pin up to V_{CIN} (logic high) to disable the ZCD_EN# function.

Thermal Shutdown Warning (THWn)

The THWn pin is an open drain signal that flags the presence of excessive junction temperature. Connect a maximum of 20 kΩ to pull this pin up to V_{CIN}. An internal temperature sensor detects the junction temperature. The temperature threshold is 160 °C. When this junction temperature is exceeded the THWn flag is set. When the junction temperature drops below 135 °C the device will clear the THWn signal. The SiC770 does not stop operation when the flag is set. The decision to shutdown must be made by an external thermal control function.

Voltage Input (V_{IN})

This is the power input to the drain of the high-side Power MOSFET. This pin is connected to the high power intermediate BUS rail.

Switch Node (V_{SWH} and PHASE)

The switch node V_{SWH} is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter. The PHASE pin is internally connected to the switch node V_{SWH}. This pin is to be used exclusively as the return pin for the BOOT capacitor. A 20 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET in the event that V_{CIN} goes to zero while V_{IN} is still applied.

Ground connections (C_{GND} and P_{GND})

P_{GND} (power ground) should be externally connected to C_{GND} (control signal ground). The layout of the printed circuit board should be such that the inductance separating the C_{GND} and P_{GND} should be a minimum. Transient differences due to inductance effects between these two pins should not exceed 0.5 V.

Control and Drive Supply Voltage Input (V_{DRV}, V_{CIN})

V_{CIN} is the bias supply for the gate drive control IC. V_{DRV} is the bias supply for the gate drivers. It is recommended to separate these pins through a resistor. This creates a low pass filtering effect to avoid coupling of high frequency gated rive noise into the IC.

Bootstrap Circuit (BOOT)

The internal bootstrap switch and an external bootstrap capacitor form a charge pump that supplies voltage to the BOOT pin. An integrated bootstrap diode is incorporated so that only an external capacitor is necessary to complete the bootstrap circuit. Connect a boot strap capacitor with one leg tied to BOOT pin and the other tied to PHASE pin.

Shoot-Through Protection and Adaptive Dead Time (AST)

The SiC770 has an internal adaptive logic to avoid shoot through and optimize dead time. The shoot through protection ensures that both high-side and low-side MOSFET are not turned on the same time. The adaptive dead time control operates as follows. The HS and LS gate voltages are monitored to prevent the one turning on until the other's gate voltage is sufficiently low (1.0 V), that and built in delays ensure the one Power MOS is completely off, before the other can be turned on. This feature helps to adjust dead time as gate transitions change with respect to output current and temperature.

Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET gate low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The SiC770 also incorporates logic to clamp the gate drive signals to zero when the UVLO falling edge triggers the shutdown of the device. As an added precaution, a 20.2 kΩ resistor is connected between GH and PHASE to provide a discharge path for the HS MOSFET.

FUNCTIONAL BLOCK DIAGRAM

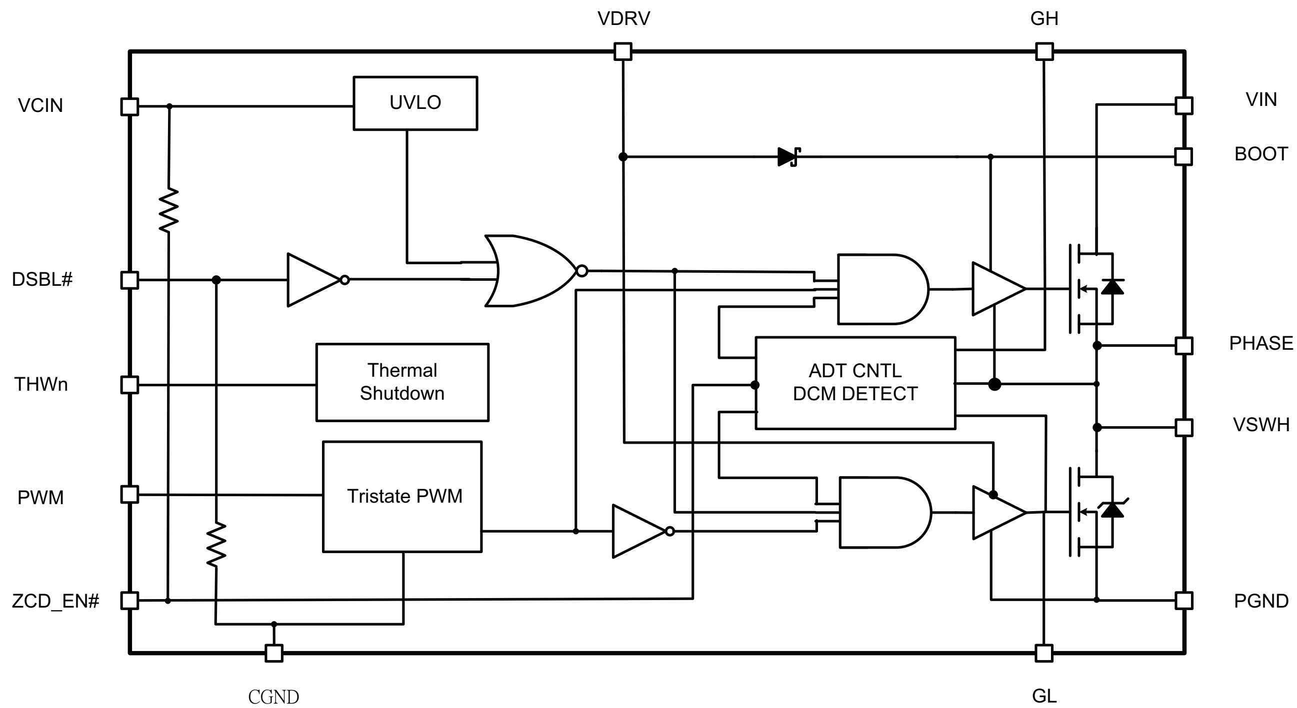


Fig. 3 - SiC770 Functional Block Diagram

DEVICE TRUTH TABLE				
DSBL#	SMOD	PWM	GH	GL
Open	X	X	L	L
L	X	X	L	L
H	L	L	L	H (IL > 0), L (IL ≤ 0)
H	L	H	H	L
H	H	H	H	L
H	H	L	L	H

PWM TIMING DIAGRAM

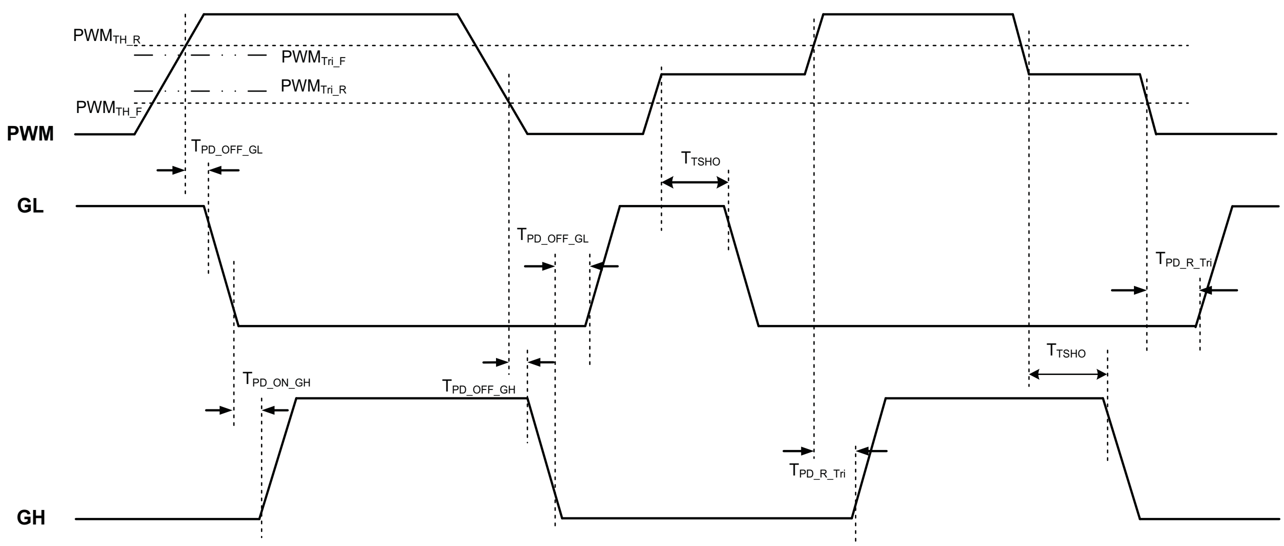


Fig. 4 - Definition of PWM Logic and Tri-State

PWM TIMING DIAGRAM

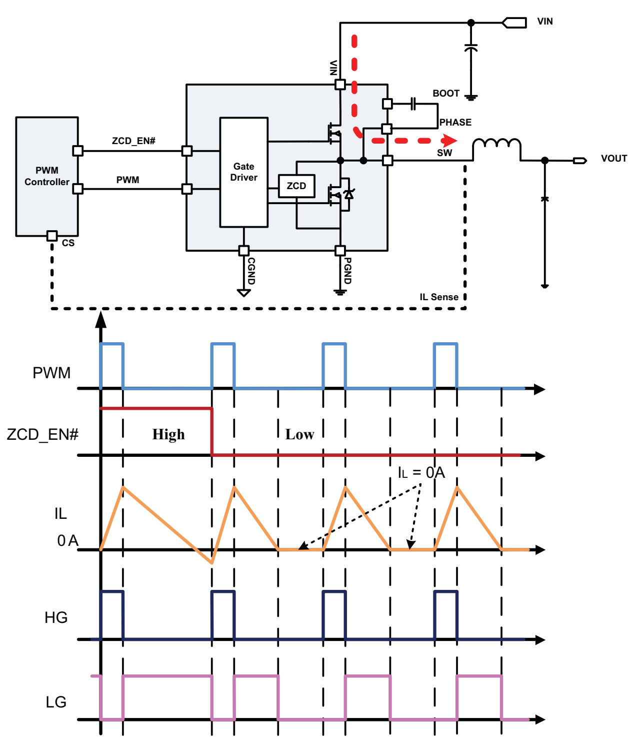


Fig. 5 - ZCD_EN# Operation Timing Diagram

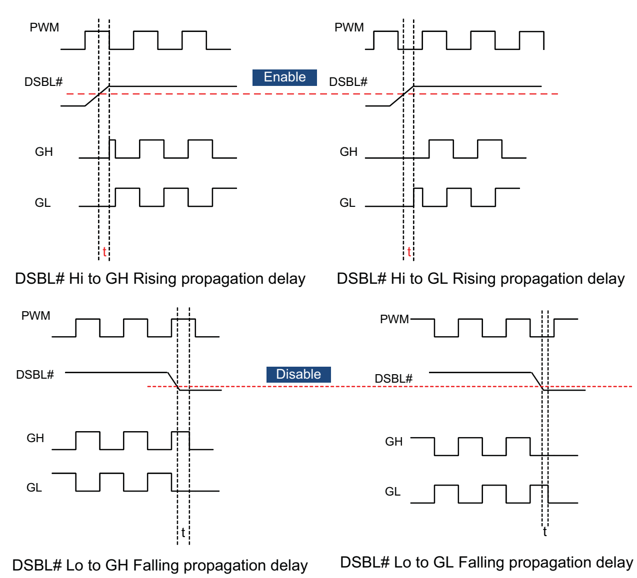
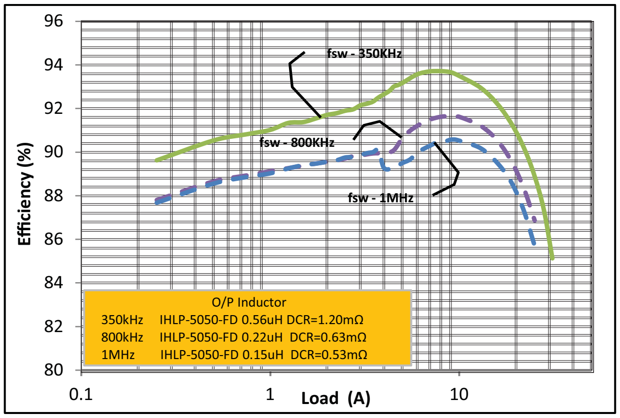
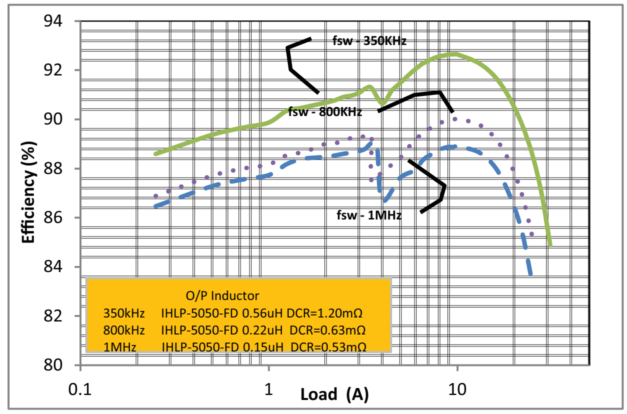


Fig. 6 - DSBL# Function Timing Diagram

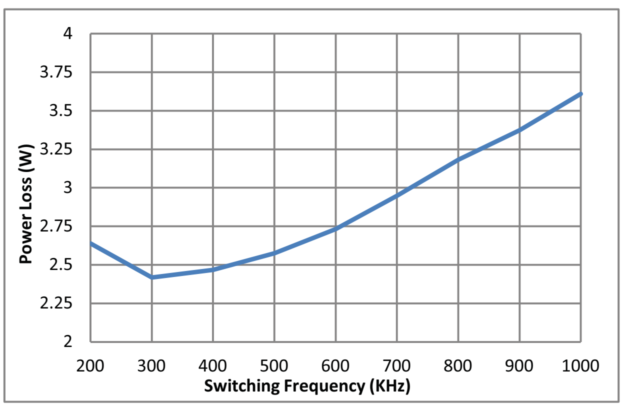
ELECTRICAL CHARACTERISTICS



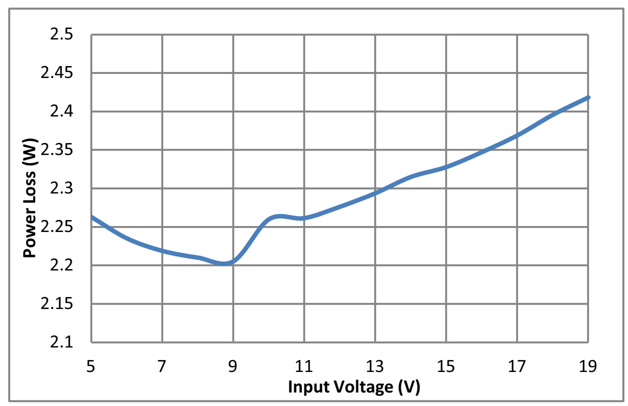
Efficiency Performance vs. f_{SW}
V_{IN} = 12 V, V_{OUT} = 1.8 V



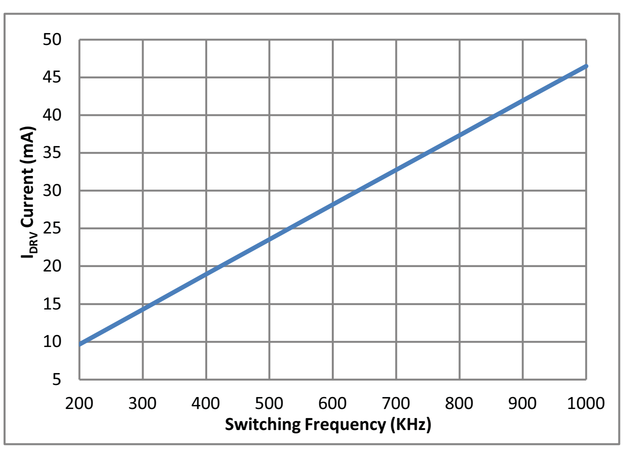
Efficiency Performance vs. f_{SW}
V_{IN} = 19 V, V_{OUT} = 1.8 V



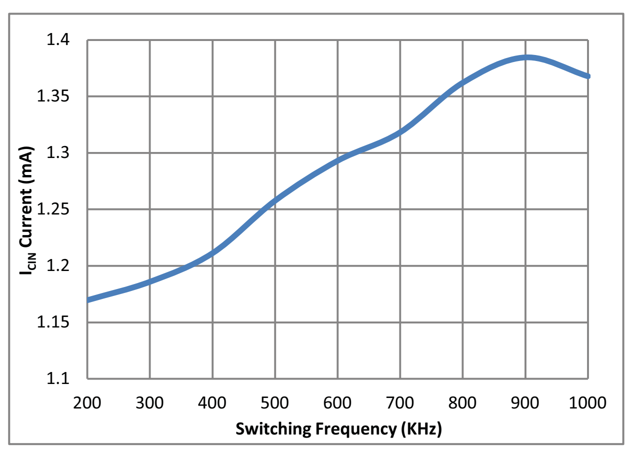
Power Loss vs. Switching Frequency
V_{IN} = 19 V, V_{OUT} = 1.8 V, I_{OUT} = 15 A, Rboot = 4.7 Ω,
Inductance = 0.47 µH



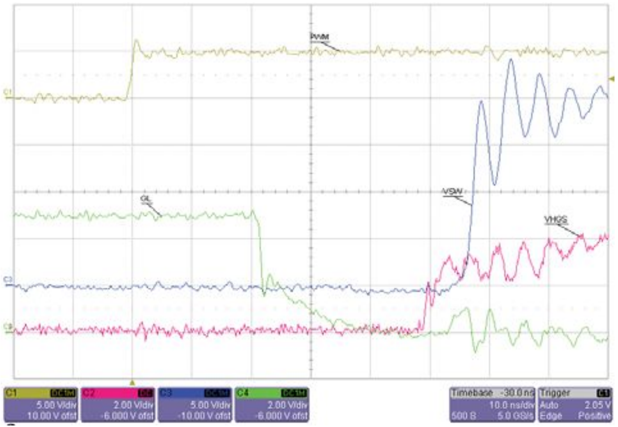
Power Loss vs. Input Voltage
V_{OUT} = 1.8 V, I_{OUT} = 15 A, f_{SW} = 300 kHz, Rboot = 4.7 Ω,
Inductance = 0.47 µH



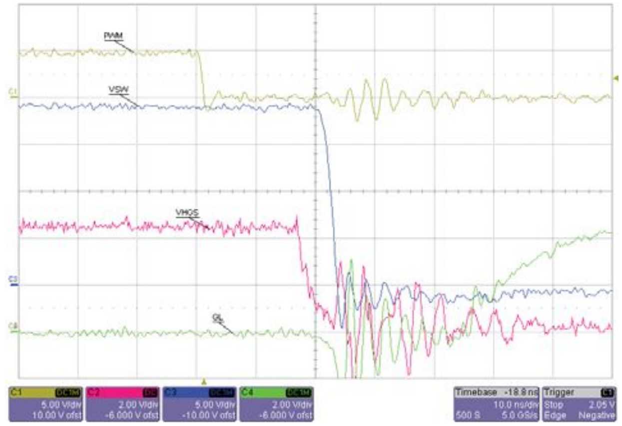
Driver Current vs. Switching Frequency
V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 20 A, V_{CIN} = V_{DRV} = 5 V



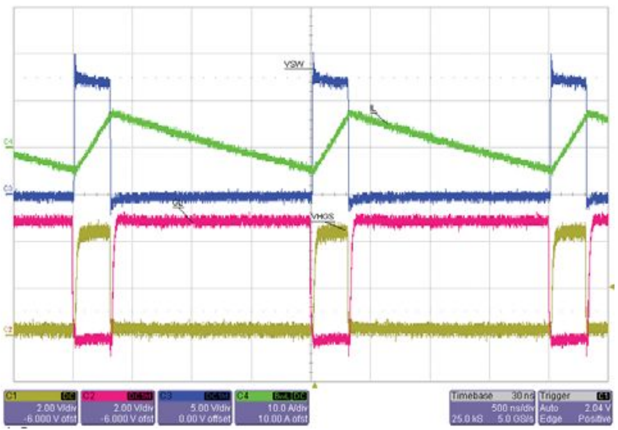
V_{CIN} Current vs. Switching Frequency
V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 20 A, V_{CIN} = V_{DRV} = 5 V



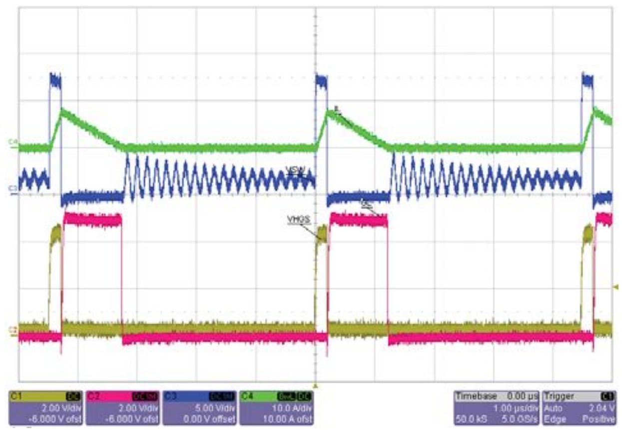
Switching Waveform at PWM Rising Edge
V_{IN} = 19 V, V_O = 1.8 V, I_O = 20 A, f_{SW} = 500 kHz



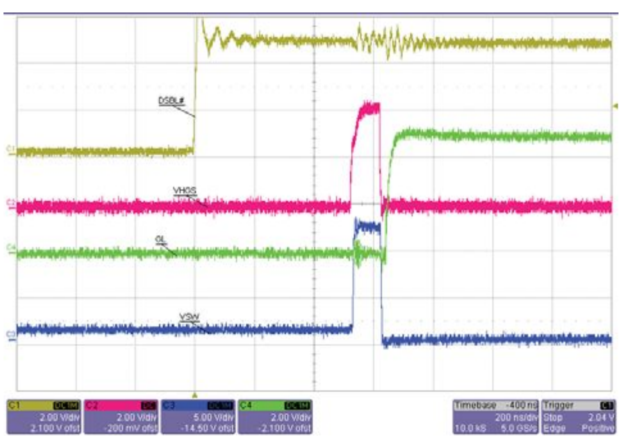
Switching Waveform at PWM Falling Edge
V_{IN} = 19 V, V_O = 1.8 V, I_O = 20 A, f_{SW} = 500 kHz



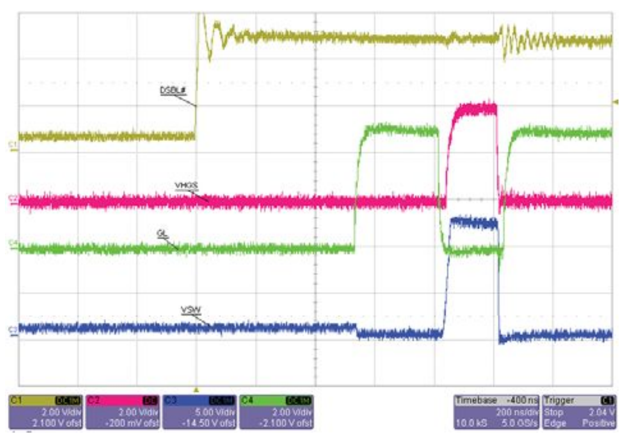
Switching Waveform at ZCD_EN# - High
V_{IN} = 12 V, V_O = 1.8 V, , I_L = 1 A, f_{SW} = 500 kHz



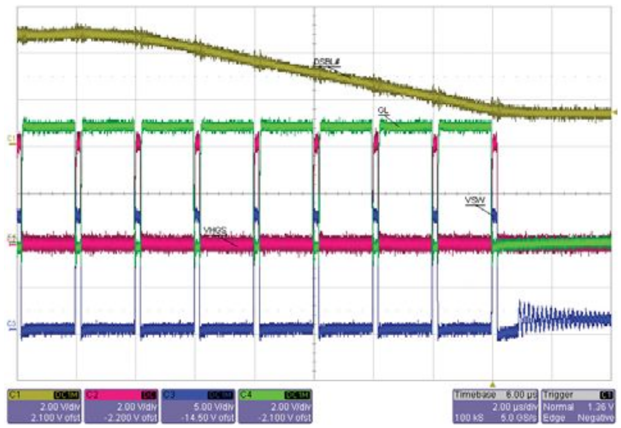
Switching Waveform at ZCD_EN# - Low
V_{IN} = 12 V, V_O = 1.8 V, , I_L = DCM, t_{on} = 200 ns



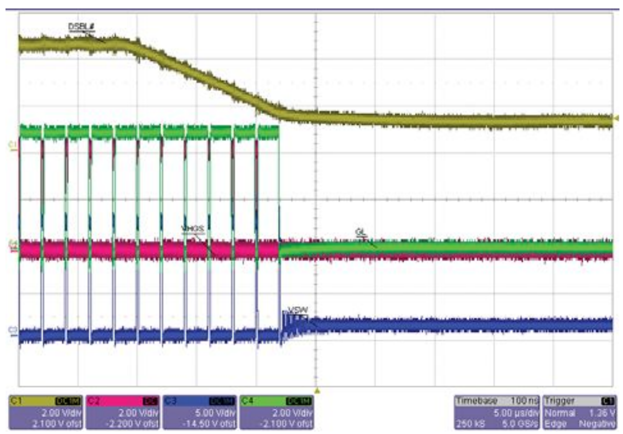
DSBL# Hi to GH Rising Propagation Delay
V_{IN} = 12 V, t_{on} = 200 ns, f_{SW} = 500 kHz, I_O = 0 A



DSBL# Hi to GL Rising Propagation Delay
V_{IN} = 12 V, t_{on} = 200 ns, f_{SW} = 500 kHz, I_O = 0 A

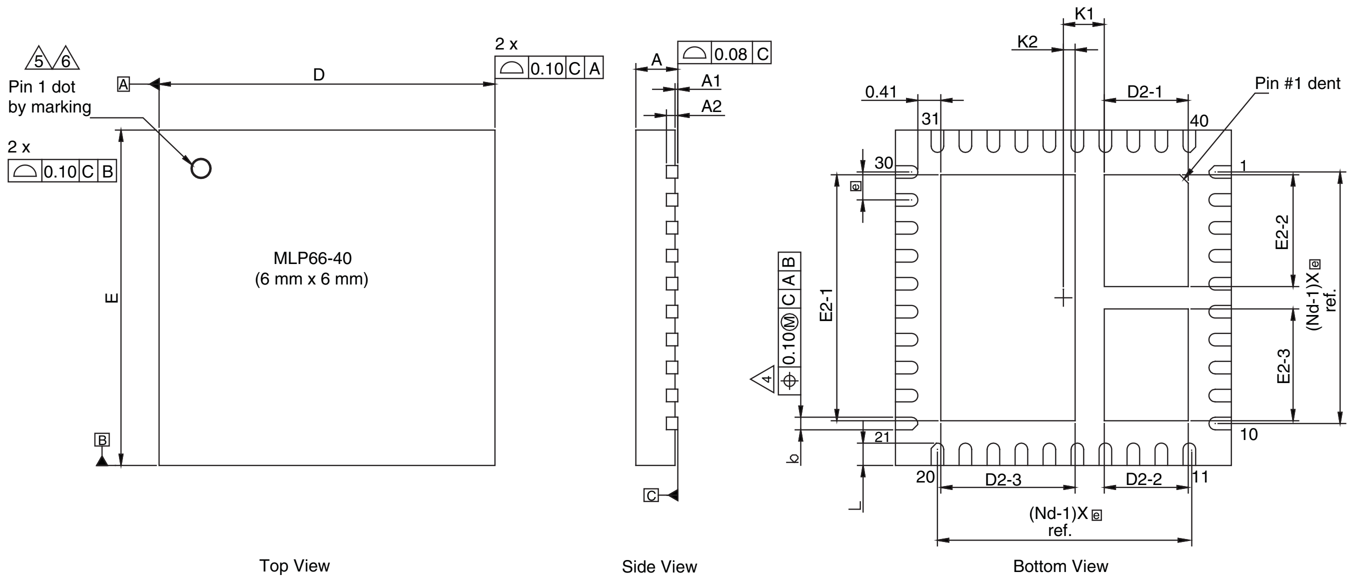


DSBL# Lo to GH Falling Propagation Delay



DSBL# Lo to GL Falling Propagation Delay

PACKAGE MECHANICAL DRAWING



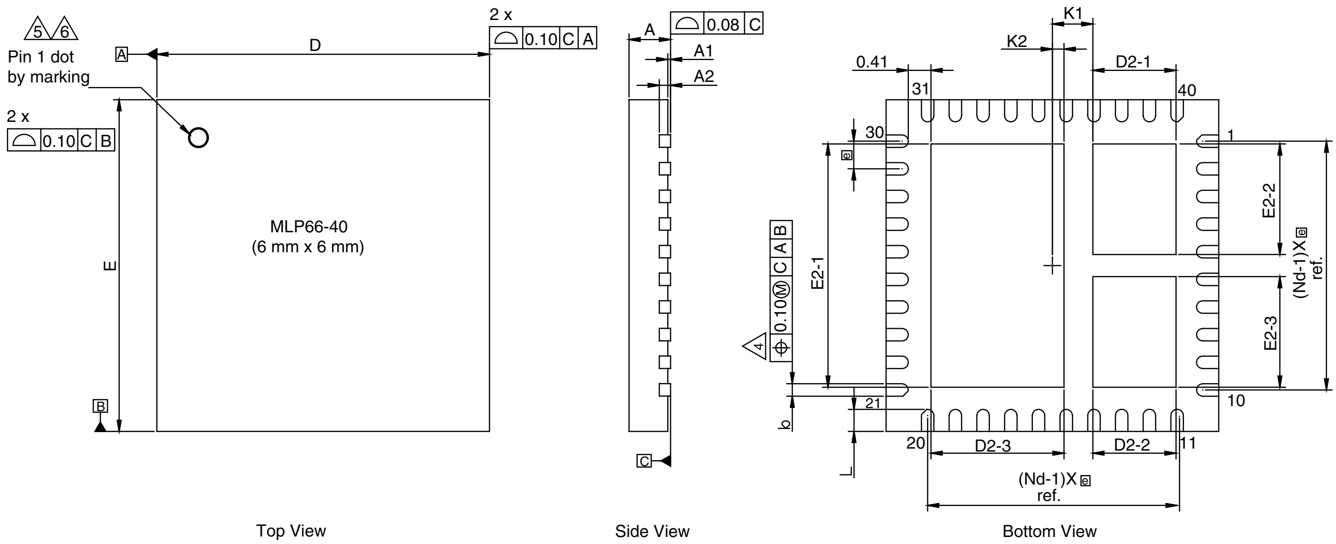
DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A (8)	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b (4)	0.20	0.25	0.30	0.078	0.098	0.011
D	6.00 BSC			0.236 BSC		
e	0.50 BSC			0.019 BSC		
E	6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N (3)	40			40		
Nd (3)	10			10		
Ne (3)	10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1	0.73 BSC			0.028 BSC		
K2	0.21 BSC			0.008 BSC		

Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals. Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62727.

PowerPAK® MLP66-40 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A [(8)]	0.70	0.75	0.80	0.027	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
A2	0.20 ref.			0.008 ref.		
b [(4)]	0.20	0.25	0.30	0.078	0.098	0.011
D	6.00 BSC			0.236 BSC		
e	0.50 BSC			0.019 BSC		
E	6.00 BSC			0.236 BSC		
L	0.35	0.40	0.45	0.013	0.015	0.017
N [(3)]	40			40		
Nd [(3)]	10			10		
Ne [(3)]	10			10		
D2-1	1.45	1.50	1.55	0.057	0.059	0.061
D2-2	1.45	1.50	1.55	0.057	0.059	0.061
D2-3	2.35	2.40	2.45	0.095	0.094	0.096
E2-1	4.35	4.40	4.45	0.171	0.173	0.175
E2-2	1.95	2.00	2.05	0.076	0.078	0.080
E2-3	1.95	2.00	2.05	0.076	0.078	0.080
K1	0.73 BSC			0.028 BSC		
K2	0.21 BSC			0.008 BSC		
ECN: T14-0826-Rev. B, 12-Jan-15 DWG: 5986						

Notes

1. Use millimeters as the primary measurement
2. Dimensioning and tolerances conform to ASME Y14.5M. - 1994
3. N is the number of terminals. Nd is the number of terminals in X-direction and Ne is the number of terminals in Y-direction
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
5. The pin #1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
6. Exact shape and size of this feature is optional
7. Package warpage max. 0.08 mm
8. Applied only for terminals

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