

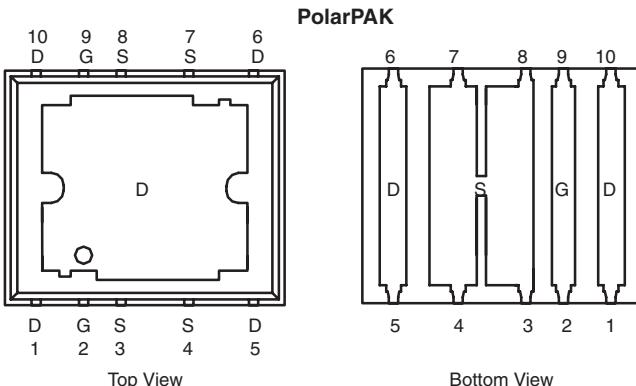
N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^a		Q _g (Typ.)
		Silicon Limit	Package Limit	
20	0.0034 at V _{GS} = 10 V	138	50	24 nC
	0.0055 at V _{GS} = 4.5 V	108	50	

Package Drawing

www.vishay.com/doc?73398



Top View

Bottom View

Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE822DF-T1-E3 (Lead (Pb)-free)

SiE822DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

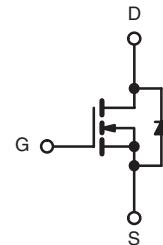
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{gd}/Q_{gs} Ratio Helps Prevent Shoot-Through
- 100 % R_g and UIS Tested
- Compliant to RoHS directive 2002/95/EC



APPLICATIONS

- VRM
- DC-DC Conversion
- Synchronous Rectification



N-Channel MOSFET

For Related Documents
www.vishay.com/pgg?74451

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	138 (Silicon Limit)	
		50 ^a (Package Limit)	
		50 ^a	
		31 ^{b, c}	
		24.8 ^{b, c}	
Pulsed Drain Current	I _{DM}	80	
Continuous Source-Drain Diode Current	I _S	50 ^a	
		4.3 ^{b, c}	
Single Pulse Avalanche Current	I _{AS}	30	
Avalanche Energy	E _{AS}	45	mJ
Maximum Power Dissipation	P _D	104	
		66	
		5.2 ^{b, c}	
		3.3 ^{b, c}	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

Notes:

- a. Package limited is 50 A.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See Solder Profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	R_{thJA}	20	24	°C/W
Maximum Junction-to-Case (Drain Top) ^a	R_{thJC} (Drain)	1	1.2	
Maximum Junction-to-Case (Source) ^{a, c}	R_{thJC} (Source)	2.8	3.4	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. Maximum under Steady State conditions is 68 °C/W.
- c. Measured at source pin (on the side of the package).

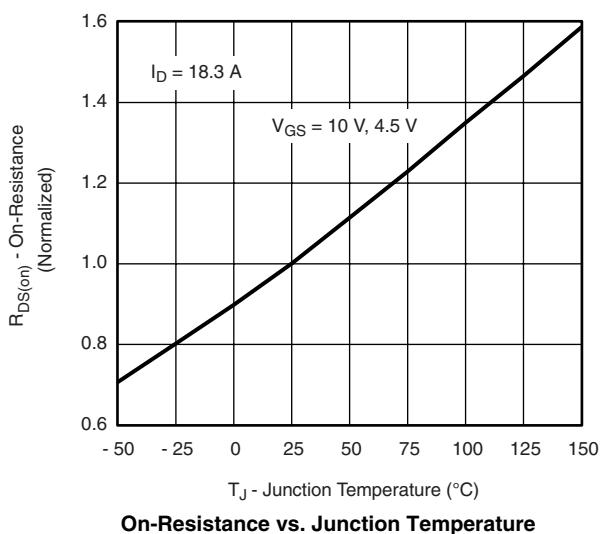
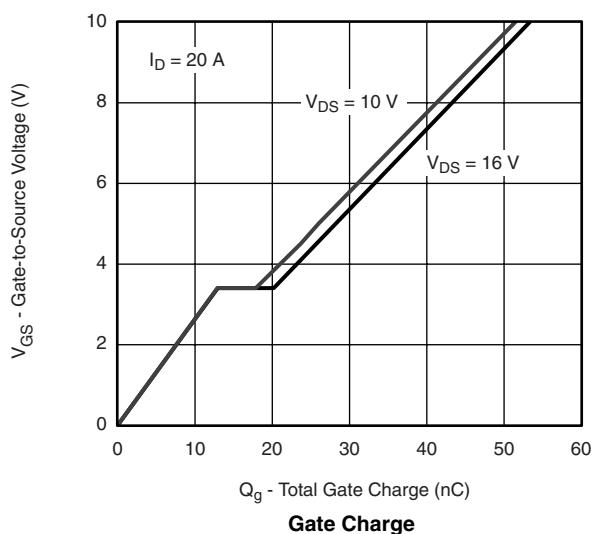
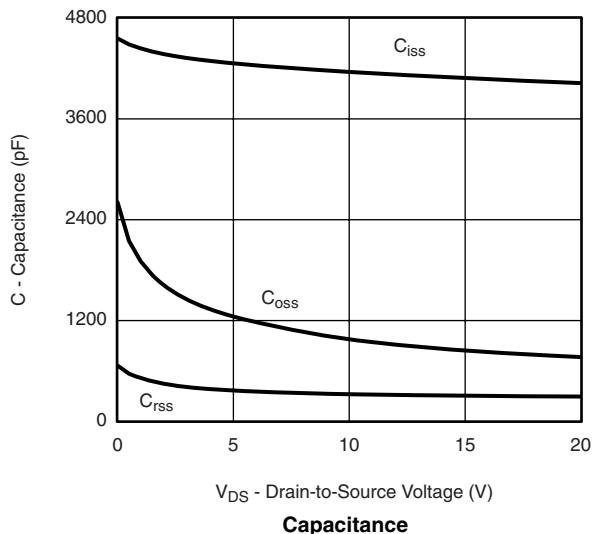
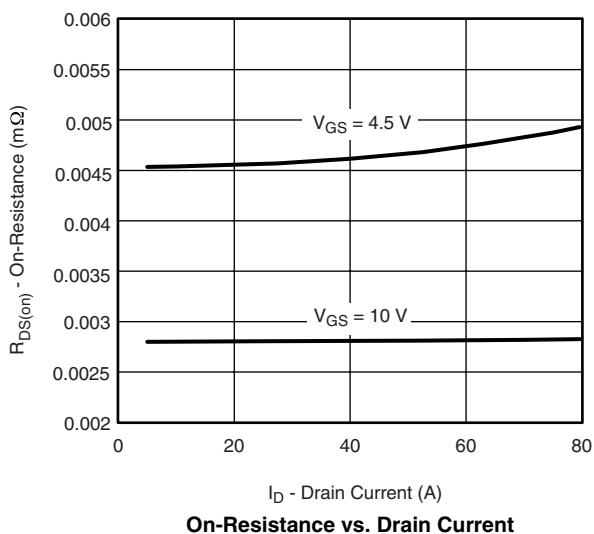
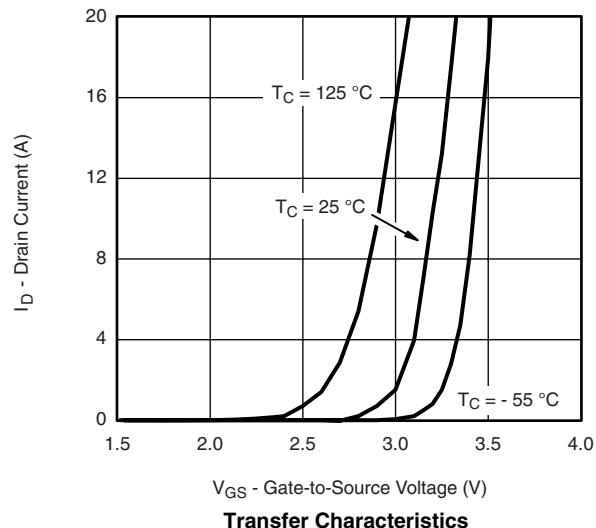
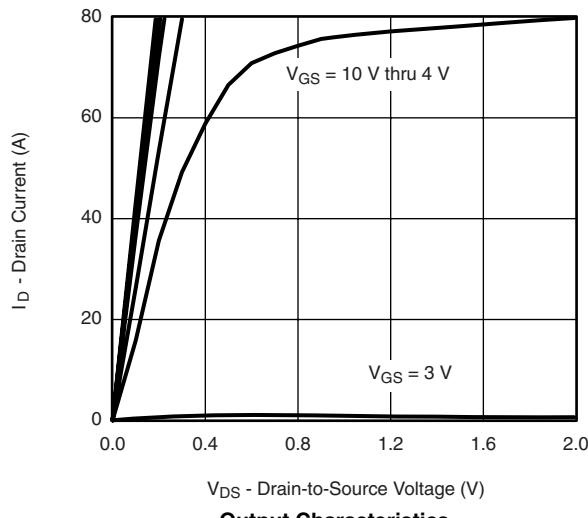
SPECIFICATIONS $T_J = 25^\circ\text{C}$, unless otherwise noted

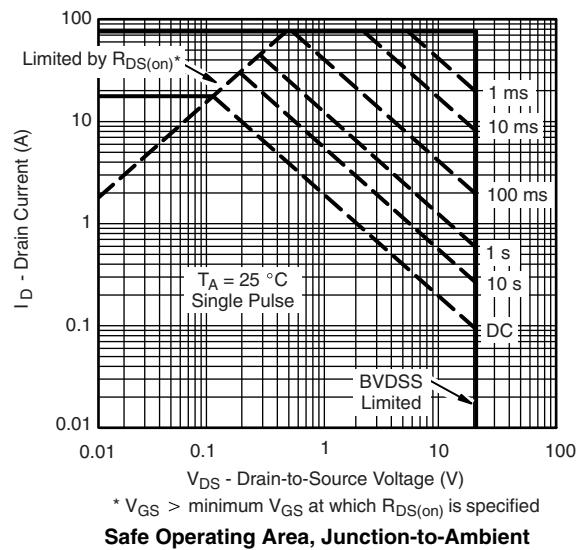
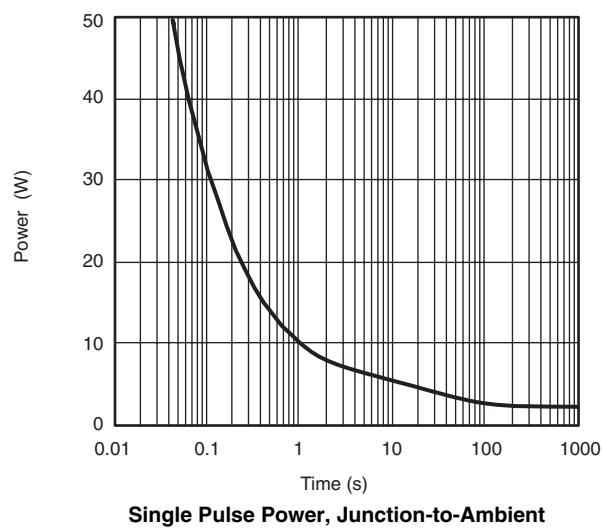
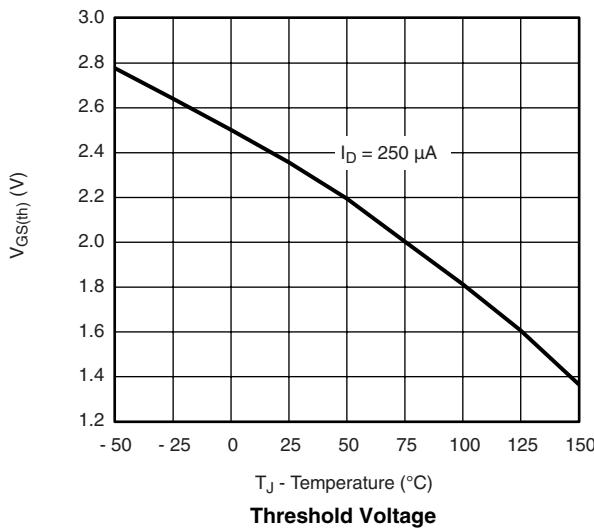
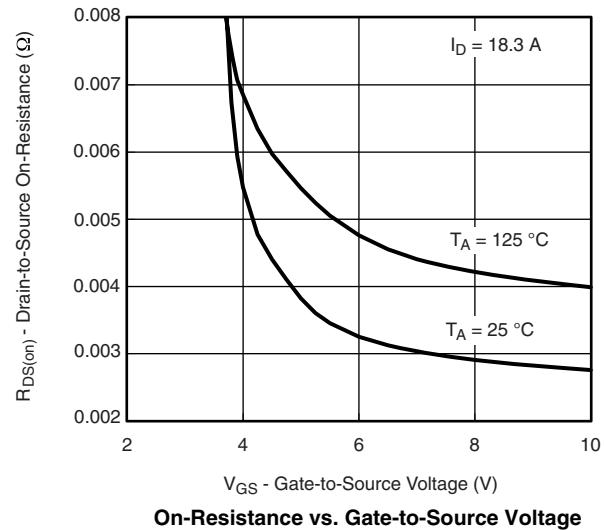
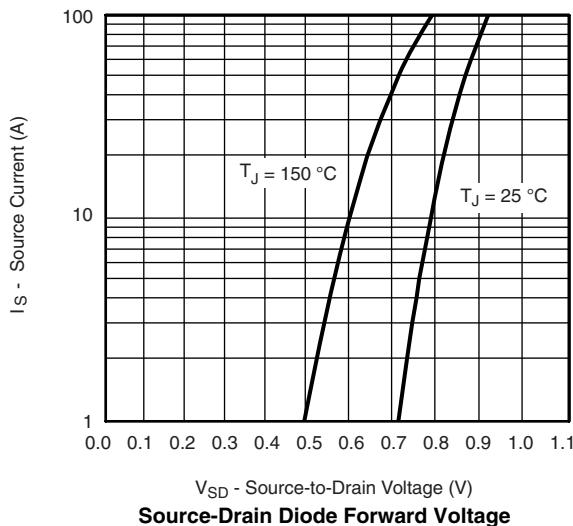
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250 \mu\text{A}$		24.1		mV/°C
$V_{GS(\text{th})}$ Temperature Coefficient	$\Delta V_{GS(\text{th})}/T_J$			- 7.1		
Gate-Source Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.5	2.3	3.0	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(\text{on})}$	$V_{DS} \geq 5 \text{ V}, V_{GS} = 10 \text{ V}$	25			A
Drain-Source On-State Resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}, I_D = 18.3 \text{ A}$		0.0028	0.0034	Ω
		$V_{GS} = 4.5 \text{ V}, I_D = 14.5 \text{ A}$		0.0045	0.0055	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 18.3 \text{ A}$		90		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		4200		pF
Output Capacitance	C_{oss}			1000		
Reverse Transfer Capacitance	C_{rss}			320		
Total Gate Charge	Q_g	$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		52	78	nC
Gate-Source Charge	Q_{gs}			24	36	
Gate-Drain Charge	Q_{gd}			13		
Gate Resistance	R_g			5		
Turn-On Delay Time	$t_{d(\text{on})}$	$V_{DD} = 10 \text{ V}, R_L = 1 \Omega$ $I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		1.0	1.5	Ω
Rise Time	t_r			50	75	ns
Turn-Off Delay Time	$t_{d(\text{off})}$			220	330	
Fall Time	t_f			35	55	
Turn-On Delay Time	$t_{d(\text{on})}$			20	30	
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(\text{off})}$			25	40	
Fall Time	t_f			35	55	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25^\circ\text{C}$			50	A
Pulse Diode Forward Current ^a	I_{SM}				80	
Body Diode Voltage	V_{SD}	$I_S = 10 \text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 10 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}, T_J = 25^\circ\text{C}$		40	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			36	60	nC
Reverse Recovery Fall Time	t_a			19		ns
Reverse Recovery Rise Time	t_b			21		

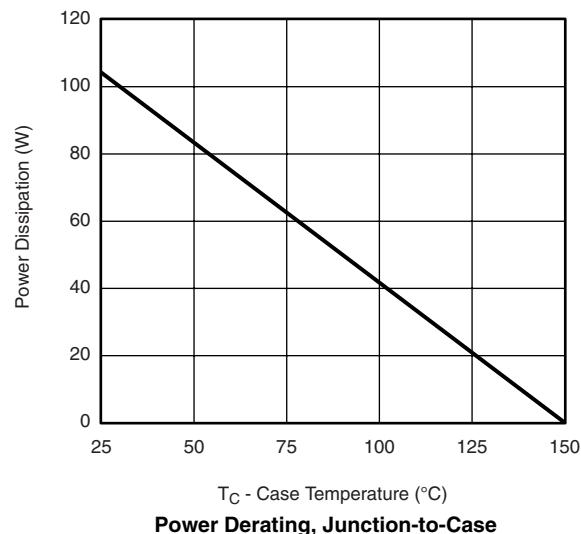
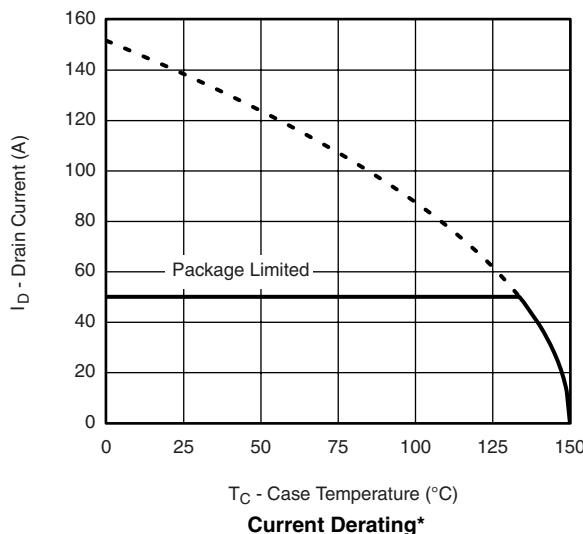
Notes:

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing.

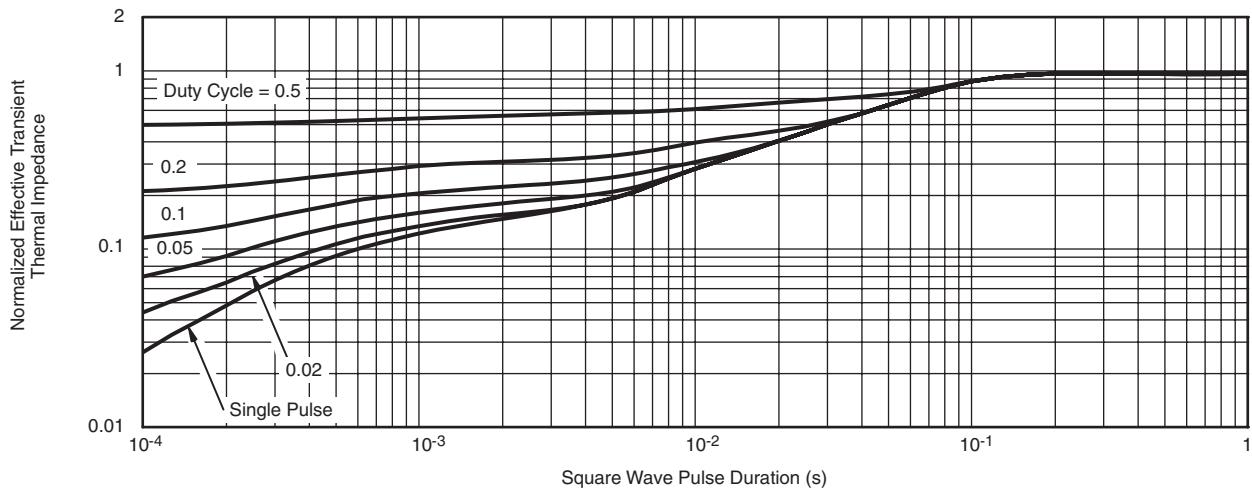
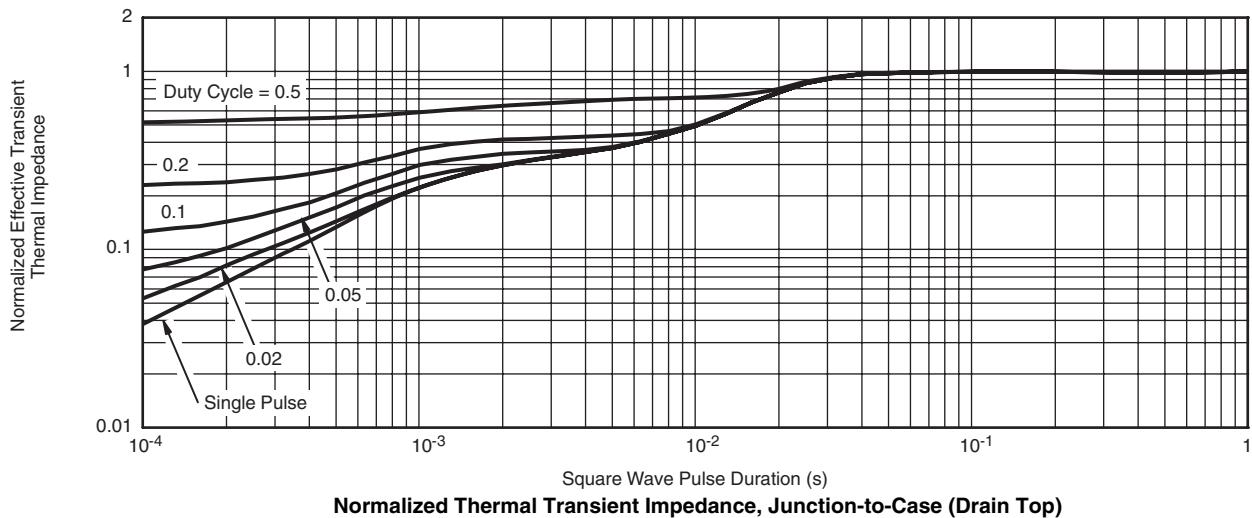
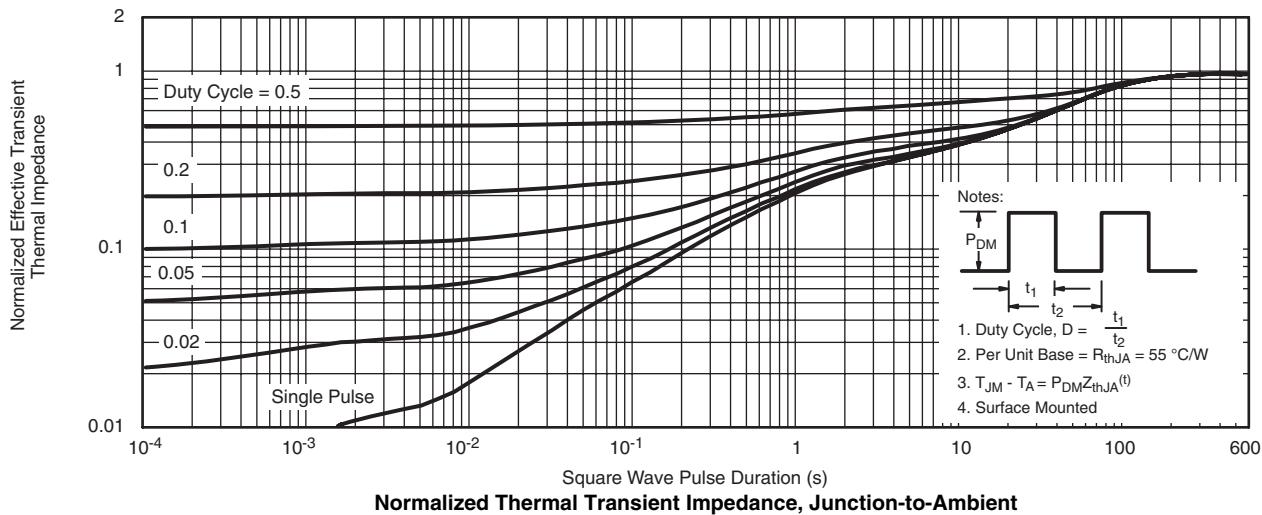
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


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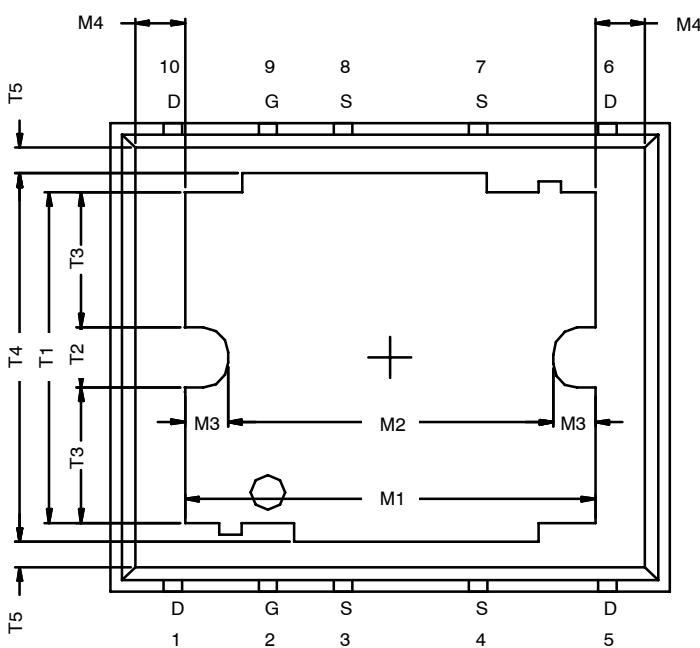
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

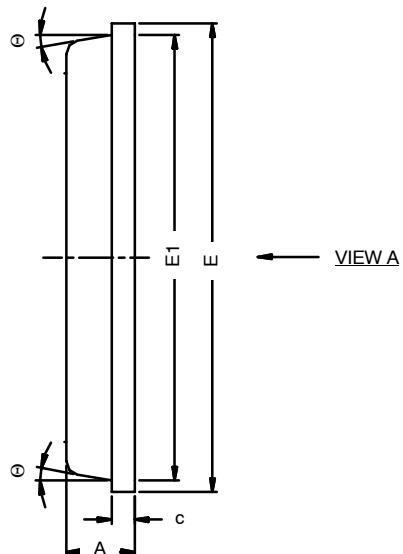
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PolarPAK™ (Option S)

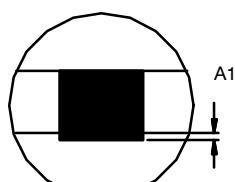
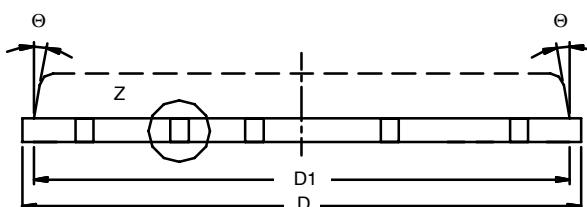


(Top View)

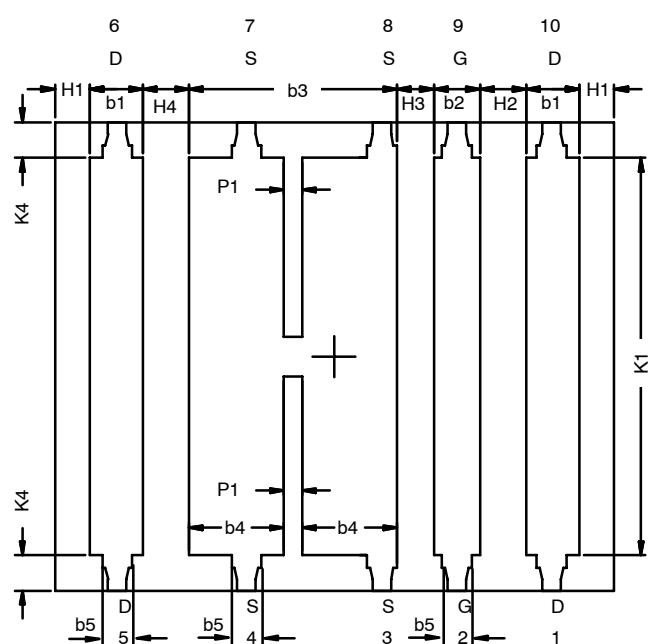
Product datasheet/information page contain links to applicable package drawing.



VIEW A



DETAIL Z



VIEW A

(Bottom View)

Package Information

Vishay Siliconix

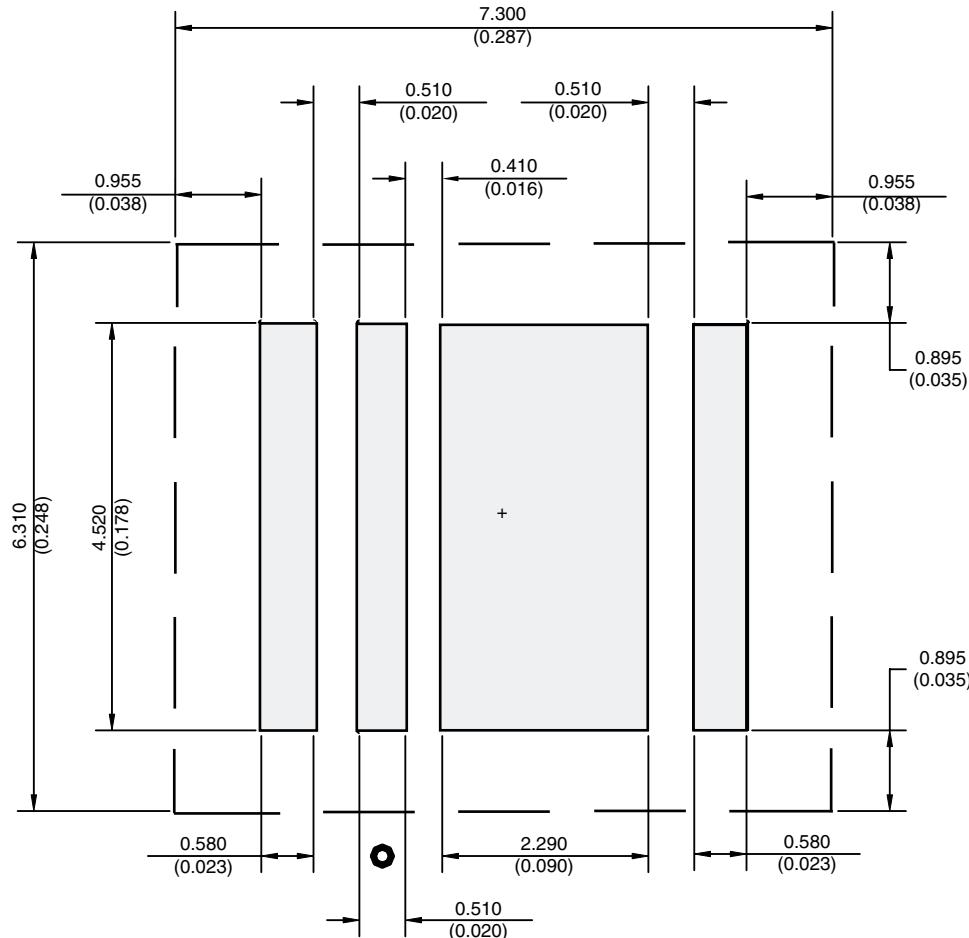


Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.75	0.80	0.85	0.030	0.031	0.033
A1	0.00	—	0.05	0.000	—	0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6.00	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23	—	—	0.009	—	—
H2	0.45	—	0.56	0.020	—	0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45	—	0.56	0.020	—	0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K4	0.24	—	—	0.009	—	—
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22	—	—	0.009	—	—
M4	0.05	—	—	0.002	—	—
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.150
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20	—	—	0.051	—	—
T4	3.90	—	—	0.154	—	—
T5	0	0.18	0.36	0.000	0.007	0.014
Θ	0°	10°	12°	0°	10°	12°

ECN: S-51049 Rev. B, 13-Jun-05
DWG: 5947

Note: Millimeters govern over inches

RECOMMENDED MINIMUM PADS FOR PolarPAK® Option L and S



Recommended Minimum for PolarPAK Option L and S

Dimensions in mm/(Inches)

No External Traces within Broken Lines

Dot indicates Gate Pin (Part Marking)



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[NTE2911](#) [US6M2GTR](#) [TK10A80W,S4X\(S](#) [SSM6P69NU,LF](#)