

RoHS

COMPLIANT

HALOGEN

FREE

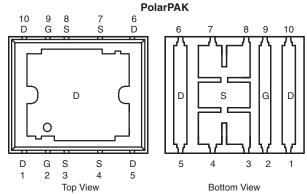


Vishay Siliconix

N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY						
		I _D (A)				
V _{DS} (V)	R _{DS(on)} (Ω)	Silicon Limit	Package Limit	Q _g (Typ.)		
60	$0.0061 \text{ at V}_{GS} = 10 \text{ V}$	110	60	51 nC		

Package Drawing: www.vishay.com/doc?72945



Top surface is connected to pins 1, 5, 6, and 10

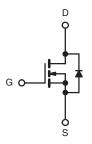
Ordering Information: SiE876DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK[®] Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size < 150 V
- Low Q_{ad}/Q_{as} Ratio Helps Prevent Shoot-Through
- 100 % R_q and UIS Tested
- Compliant to RoHS directive 2002/95/EC

APPLICATIONS

- Primary Side Switch
- · Half-Bridge



N-Channel MOSFET
For Related Documents:
www.vishay.com/ppg?64823

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V_{DS}	60	V	
Gate-Source Voltage		V_{GS}	± 20	V	
	T _C = 25 °C		110 (Silicon Limit)		
	10-23 0		60 ^a (Package Limit)		
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	I _D	60 ^a		
	T _A = 25 °C		22 ^{b, c}		
	T _A = 70 °C		17.9 ^{b, c}	Α	
Pulsed Drain Current		I _{DM}	60		
Continuous Source-Drain Diode Current	T _C = 25 °C		60 ^a		
Continuous Source-Diam Diode Current	T _A = 25 °C	I _S	4.3 ^{b, c}		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	50		
Single Pulse Avalanche Energy		E _{AS}	125	mJ	
	T _C = 25 °C		125		
Maximum Power Dissipation	T _C = 70 °C	P _D	80	w	
Maximum Power Dissipation	T _A = 25 °C	' D	5.2 ^{b, c}	VV	
	T _A = 70 °C		3.3 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Temperature) ^{d, e}		Ĭ	260		

Notes:

- a. Package limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. See Solder Profile (www.vishay.com/ppg?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

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THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, b}	t ≤ 10 s	R_{thJA}	20	24		
Maximum Junction-to-Case (Drain Top)	Steady State	R _{thJC} (Drain)	0.8	1	°C/W	
Maximum Junction-to-Case (Source)a, c	Oleady State	R _{thJC} (Source)	2.2	2.7		

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. Maximum under Steady State conditions is 68 °C/W.
- c. Measured at source pin (on the side of the package).

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V_{DS}	V _{GS} = 0 V, I _D = 250 μA	60			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1		70		\//0C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 9		mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	2.5		4.4	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Cata Valtana Duain Commant		V _{DS} = 60 V, V _{GS} = 0 V	1 10		1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V, T _J = 55 °C			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	25			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0050	0.0061	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		30		S	
Dynamic ^b			ı		I.		
Input Capacitance	C _{iss}			3100		pF	
Output Capacitance	C _{oss}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		480			
Reverse Transfer Capacitance	C _{rss}			180			
Total Gate Charge	Q_q			51	77	nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 19.8 \text{ A}$		19			
Gate-Drain Charge	Q_{gd}			15			
Gate Resistance	R_{g}	f = 1 MHz		1.1	2.2	Ω	
Turn-On Delay Time	t _{d(on)}			22	30		
Rise Time	t _r	V_{DD} = 30 V, R_L = 3 Ω		10	15	- ns	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		25	40		
Fall Time	t _f	-		10	15		
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			60	А	
Pulse Diode Forward Current ^a	I _{SM}	-			60		
Body Diode Voltage	V_{SD}	I _S = 10 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	- -		60	90	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	L = 10 A dl/dt = 100 A/va T 05 °C		135	205	nC	
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		42		ns	
Reverse Recovery Rise Time	t _b			18			

Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing.

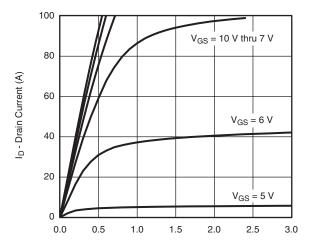
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





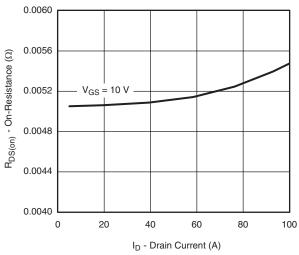
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

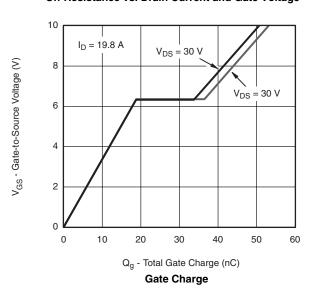


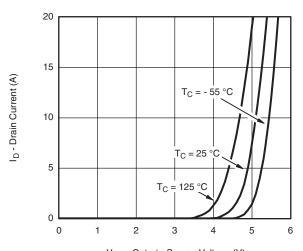
 V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics



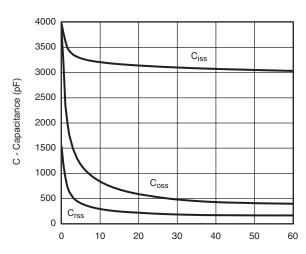
On-Resistance vs. Drain Current and Gate Voltage





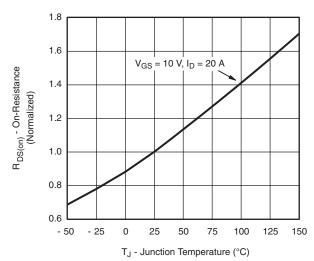
V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



V_{DS} - Drain-to-Source Voltage (V)

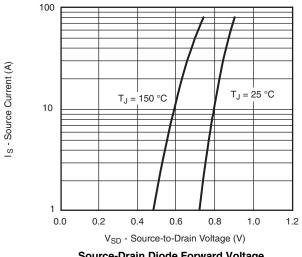
Capacitance

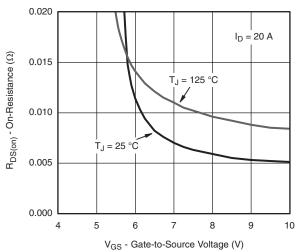


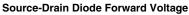
On-Resistance vs. Junction Temperature

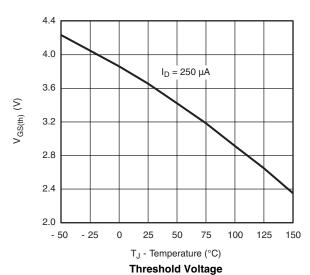
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

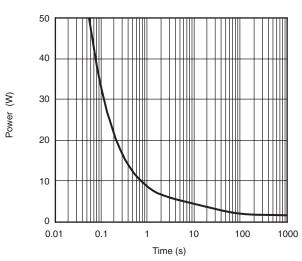




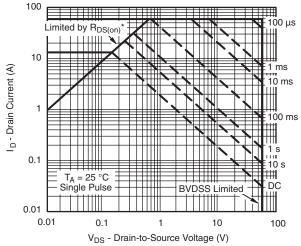




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



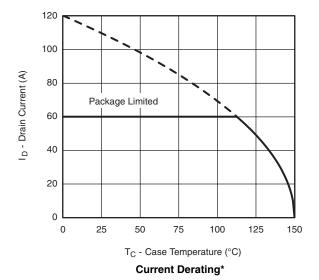
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

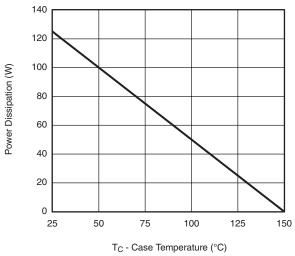
Safe Operating Area, Junction-to-Ambient



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





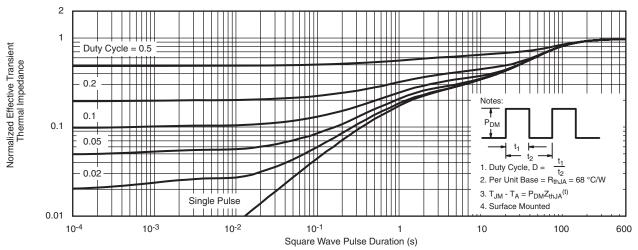
Power Derating, Junction-to-Case

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

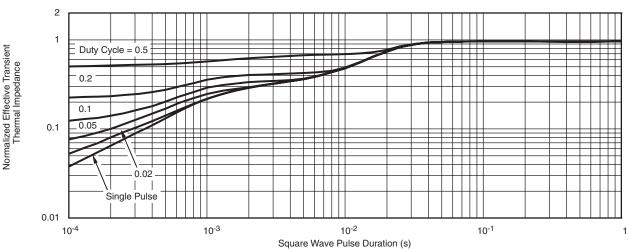
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case (Drain Top)

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