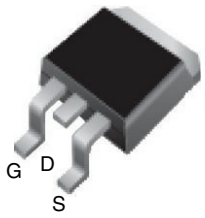
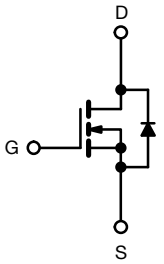
# E Series Power MOSFET

**D²PAK (TO-263)**




N-Channel MOSFET

## FEATURES

- Low figure-of-merit (FOM) $R_{on}$ x $Q_g$
- Low input capacitance ($C_{iss}$)
- Reduced switching and conduction losses
- Ultra low gate charge ($Q_g$)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

## APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) at $T_J$ max. | 850 | |
| $R_{DS(on)}$ typ. (Ω) at 25 °C | $V_{GS}$ = 10 V | 0.25 |
| $Q_g$ max. (nC) | 122 | |
| $Q_{gs}$ (nC) | 14 | |
| $Q_{gd}$ (nC) | 23 | |
| Configuration | Single | |

| ORDERING INFORMATION | |
|---|---|
| Package | D²PAK (TO-263) |
| Lead (Pb)-free and halogen-free | SiHB17N80E-GE3 |
| | SiHB17N80E-T1-GE3 |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-source voltage | | | $V_{DS}$ | 800 | V |
| Gate-source voltage | | | $V_{GS}$ | ± 30 | |
| Continuous drain current ($T_J$ = 150 °C) | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 15 | A |
| | | $T_C$ = 100 °C | | 10 | |
| Pulsed drain current [a] | | | $I_{DM}$ | 45 | |
| Linear derating factor | | | | 1.7 | W/°C |
| Single pulse avalanche energy [b] | | | $E_{AS}$ | 353 | mJ |
| Maximum power dissipation | | | $P_D$ | 208 | W |
| Operating junction and storage temperature range | | | $T_J$, $T_{stg}$ | -55 to +150 | °C |
| Drain-source voltage slope | $T_J$ = 125 °C | | dV/dt | 70 | V/ns |
| Reverse diode dV/dt [d] | | | | 5.1 | |
| Soldering recommendations (peak temperature) [c] | For 10 s | | | 300 | °C |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature
b. $V_{DD}$ = 140 V, starting $T_J$ = 25 °C, L = 28.2 mH, $R_g$ = 25 Ω, $I_{AS}$ = 5.0 A
c. 1.6 mm from case
d. $I_{SD} \leq I_D$, dI/dt = 100 A/µs, starting $T_J$ = 25 °C



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## THERMAL RESISTANCE RATINGS

| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
|---|---|---|---|---|
| Maximum junction-to-ambient | $R_{thJA}$ | - | 62 | °C/W |
| Maximum junction-to-case (drain) | $R_{thJC}$ | - | 0.6 | |

## SPECIFICATIONS ($T_J$ = 25 °C, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 800 | - | - | V |
| $V_{DS}$ temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | - | 1.08 | - | V/°C |
| Gate-source threshold Voltage (N) | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2.0 | - | 4.0 | V |
| Gate-source leakage | $I_{GSS}$ | $V_{GS}$ = ± 20 V | - | - | ± 100 | nA |
| | | $V_{GS}$ = ± 30 V | - | - | ± 1 | µA |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ = 800 V, $V_{GS}$ = 0 V | - | - | 1 | µA |
| | | $V_{DS}$ = 640 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 10 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V; $I_D$ = 8.5 A | - | 0.25 | 0.29 | Ω |
| Forward transconductance | $g_{fs}$ | $V_{DS}$ = 30 V, $I_D$ = 8.5 A | - | 8.7 | - | S |
| **Dynamic** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 100 V, f = 1 MHz | - | 2408 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 81 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 9 | - | |
| Effective output capacitance, energy related [a] | $C_{o(er)}$ | $V_{DS}$ = 0 V to 480 V, $V_{GS}$ = 0 V | - | 58 | - | |
| Effective output capacitance, time related [b] | $C_{o(tr)}$ | | - | 296 | - | |
| Total gate charge | $Q_g$ | $V_{GS}$ = 10 V; $I_D$ = 8.5 A, $V_{DS}$ = 480 V | - | 61 | 122 | nC |
| Gate-source charge | $Q_{gs}$ | | - | 14 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 23 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = 480 V, $I_D$ = 8.5 A, $V_{GS}$ = 10 V, $R_g$ = 9.1 Ω | - | 22 | 44 | ns |
| Rise time | $t_r$ | | - | 24 | 48 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 71 | 142 | |
| Fall time | $t_f$ | | - | 26 | 52 | |
| Gate input resistance | $R_g$ | f = 1 MHz, open drain | 0.3 | 0.7 | 1.4 | Ω |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous source-drain diode current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 15 | A |
| Pulsed diode forward current | $I_{SM}$ | | - | - | 45 | |
| Diode forward voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 8.5 A, $V_{GS}$ = 0 V | - | - | 1.2 | V |
| Reverse recovery time | $t_{rr}$ | $T_J$ = 25 °C, $I_F$ = $I_S$ = 8.5 A, di/dt = 100 A/µs, $V_R$ = 25 V | - | 416 | 832 | ns |
| Reverse recovery charge | $Q_{rr}$ | | - | 6.4 | 12.8 | µC |
| Reverse recovery current | $I_{RRM}$ | | - | 27 | - | A |

**Notes**

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DSS}$



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## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

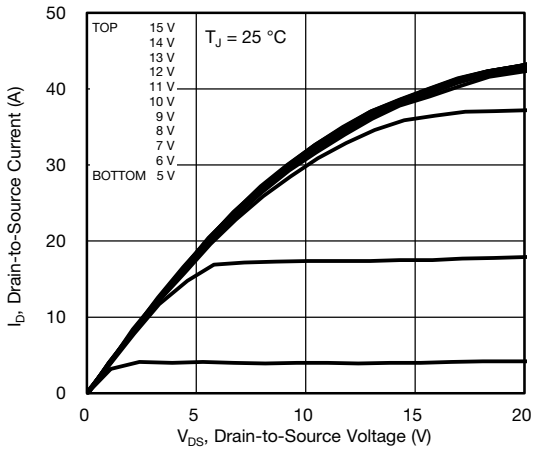


**Fig. 1 - Typical Output Characteristics**

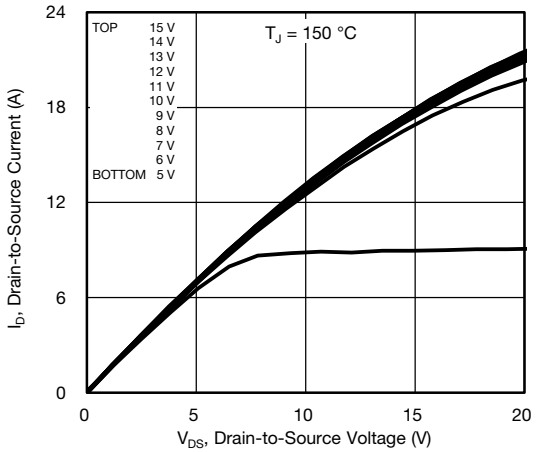


**Fig. 2 - Typical Output Characteristics**

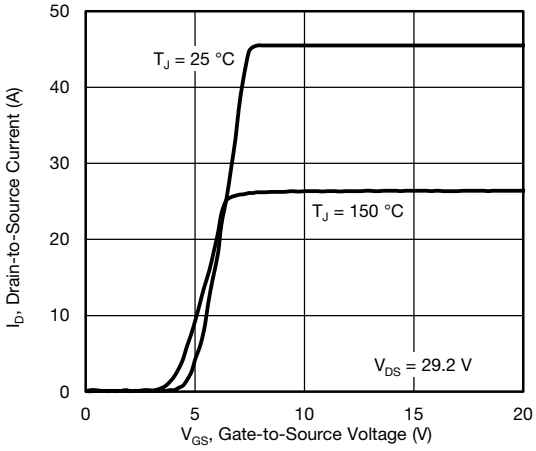


**Fig. 3 - Typical Transfer Characteristics**

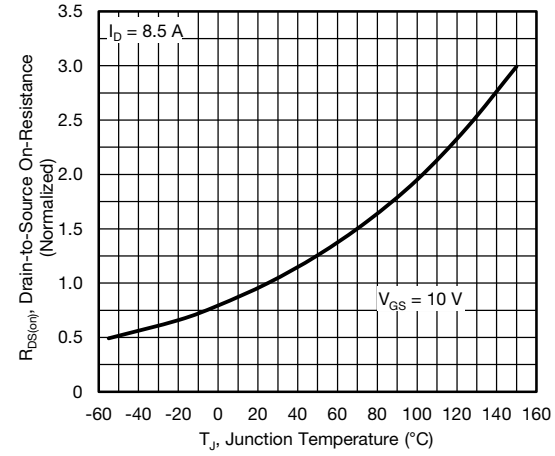


**Fig. 4 - Normalized On-Resistance vs. Temperature**

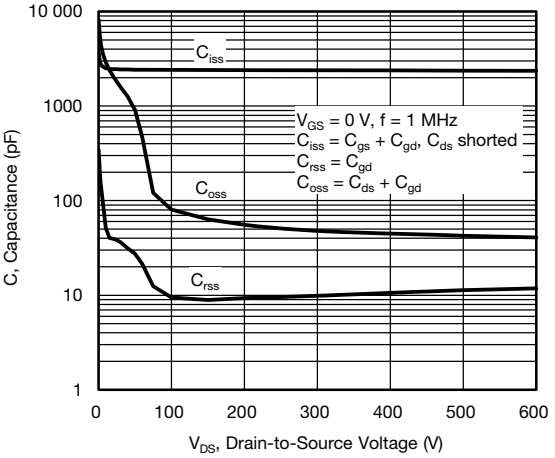


**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

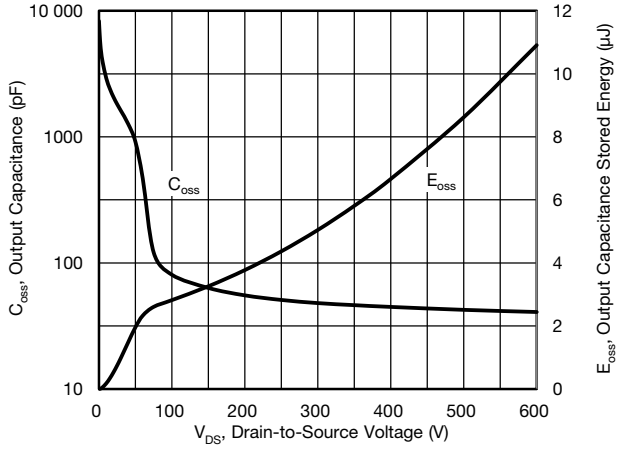


**Fig. 6 - $C_{oss}$ and $E_{oss}$ vs. $V_{DS}$**



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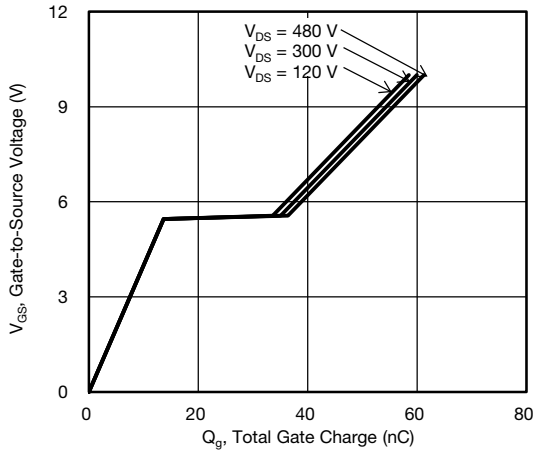


**Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage**

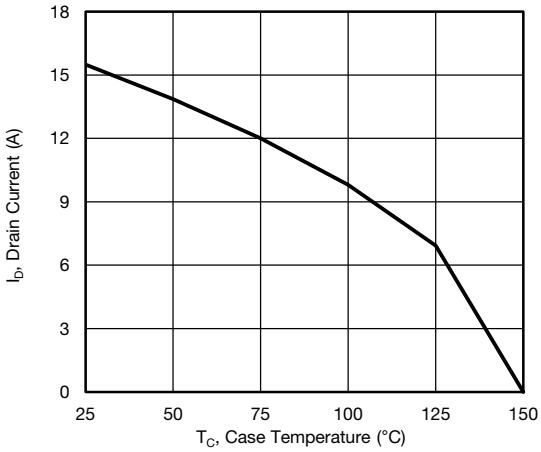


**Fig. 10 - Maximum Drain Current vs. Case Temperature**

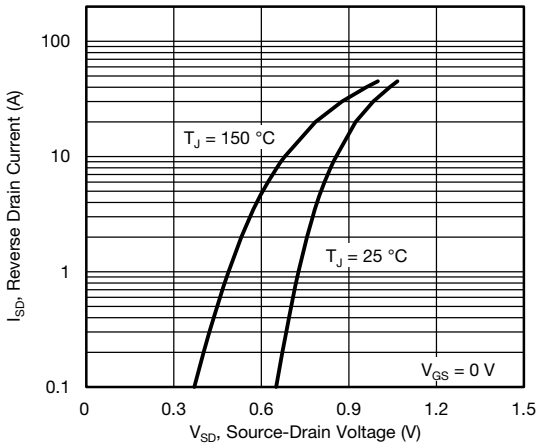


**Fig. 8 - Typical Source-Drain Diode Forward Voltage**

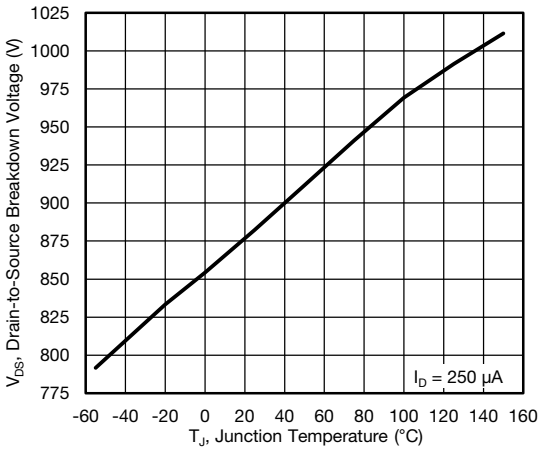


**Fig. 11 - Temperature vs. Drain-to-Source Voltage**

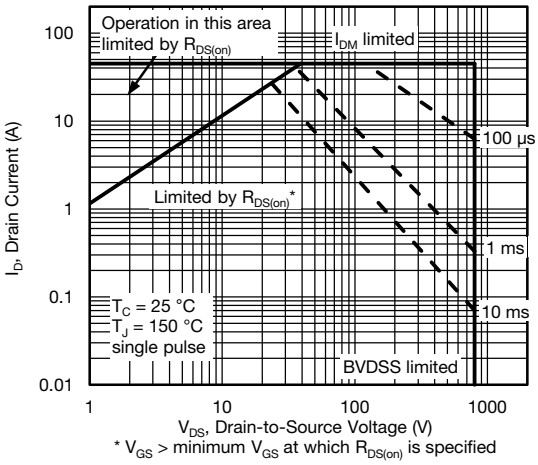


**Fig. 9 - Maximum Safe Operating Area**


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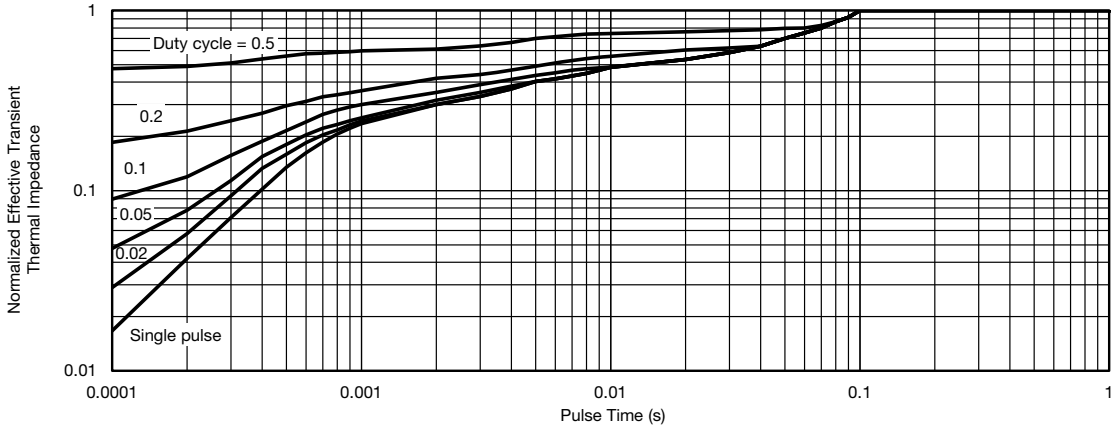


**Fig. 12 -Nor malized Thermal Transient Impedance, Junction-to-Case**

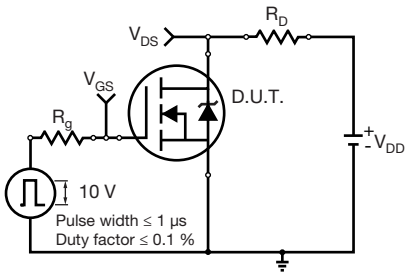


**Fig. 13 - Switching Time Test Circuit**

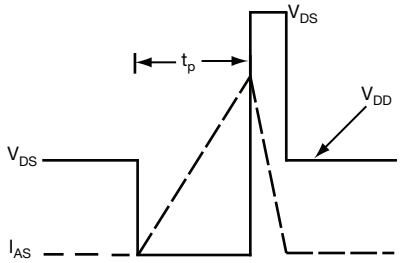


**Fig. 16 - Unclamped Inductive Waveforms**

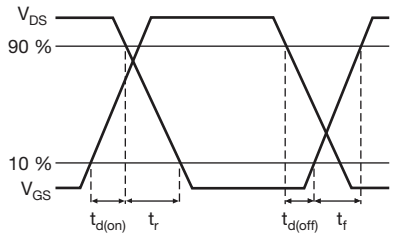


**Fig. 14 - Switching Time Waveforms**

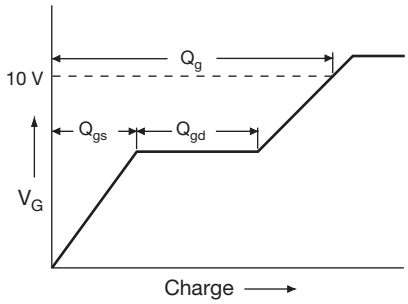


**Fig. 17 - Basic Gate Charge Waveform**

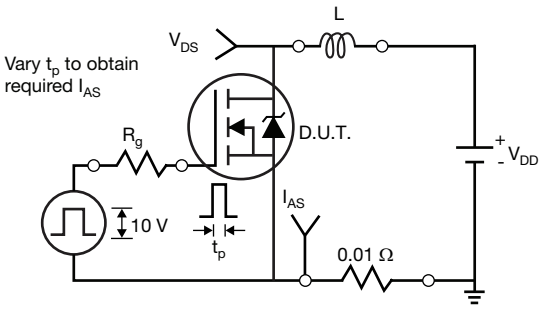


**Fig. 15 - Unclamped Inductive Test Circuit**

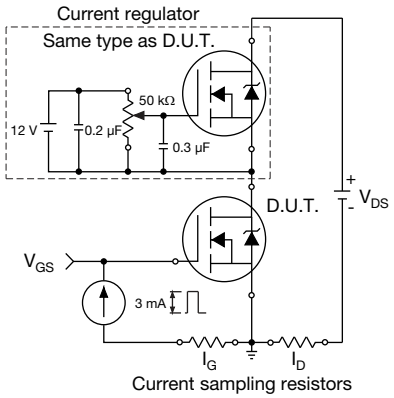


**Fig. 18 - Gate Charge Test Circuit**


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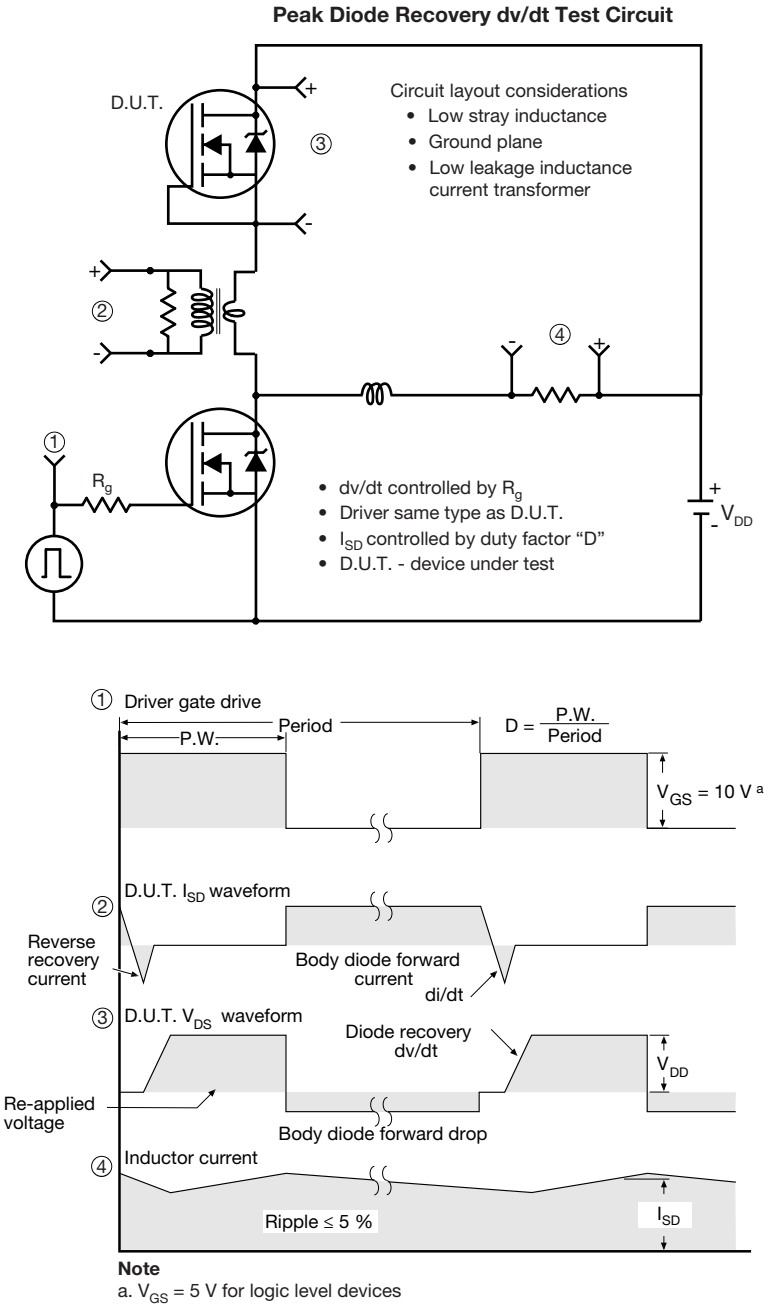


**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 19 - For N-Channel**



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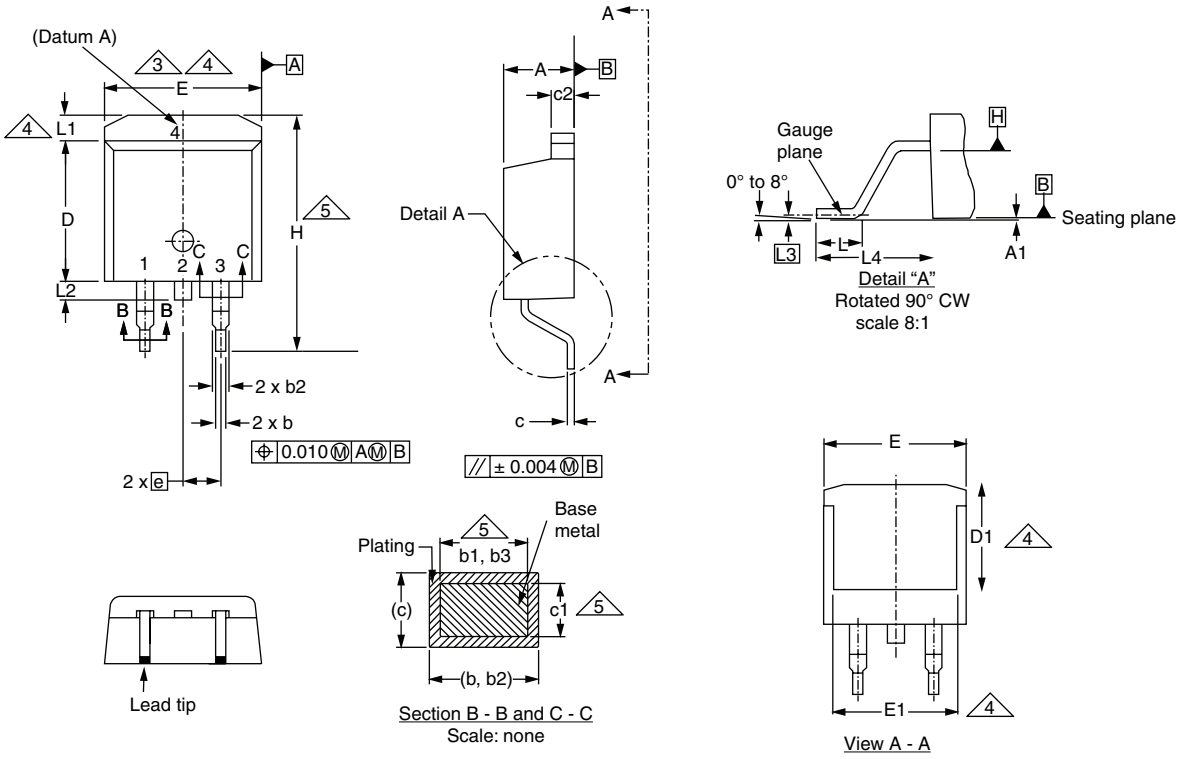
## TO-263AB (HIGH VOLTAGE)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

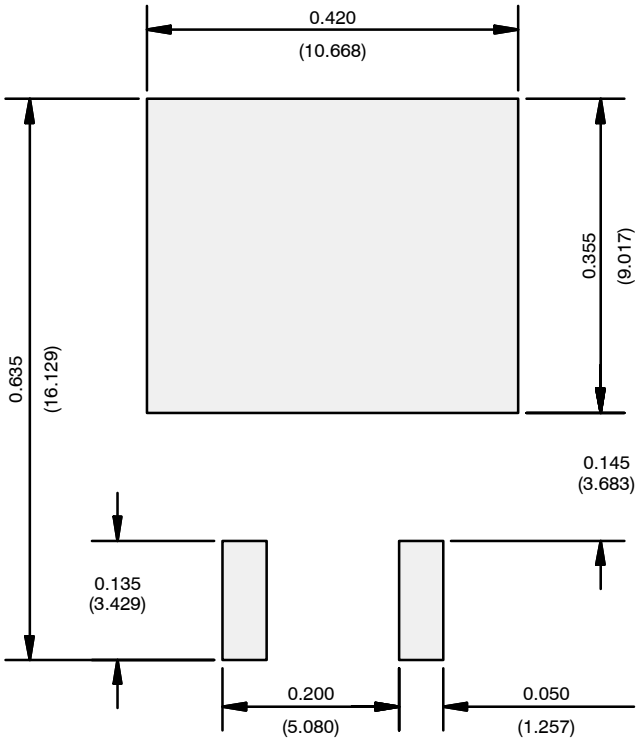
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

**Notes**

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

## RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead




Recommended Minimum Pads
Dimensions in Inches/(mm)

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