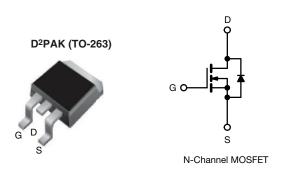
COMPLIANT

HALOGEN **FREE** 

## **E Series Power MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> (V) at T <sub>J</sub> max.	650				
R <sub>DS(on)</sub> typ. (Ω) at 25 °C	V <sub>GS</sub> = 10 V	0.156			
Q <sub>g</sub> max. (nC)	96				
Q <sub>gs</sub> (nC)	12				
Q <sub>gd</sub> (nC)	25				
Configuration	Single				



#### **FEATURES**

- Low figure-of-merit (FOM) Ron x Qa
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Ultra low gate charge (Q<sub>a</sub>)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

## **APPLICATIONS**

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

ORDERING INFORMATION			
Package	D <sup>2</sup> PAK (TO-263)		
Lead (Pb)-Free and Halogen-Free	SiHB22N60AE-GE3		

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			$V_{DS}$	600	V
Gate-Source Voltage			$V_{GS}$	± 30	7 v
Continuous Drain Current (T <sub>J</sub> = 150 °C)	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C T <sub>C</sub> = 100 °C	,	20	
	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 100 °C	I <sub>D</sub>	12	Α
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	49	
Linear Derating Factor				1.4	W/°C
Single Pulse Avalanche Energy b			E <sub>AS</sub>	204	mJ
Maximum Power Dissipation			P <sub>D</sub>	179	W
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Drain-Source Voltage Slope	$T_{J} = 1$	T <sub>J</sub> = 125 °C		70	1//20
Reverse Diode dV/dt <sup>d</sup>			dV/dt	31	- V/ns
Soldering Recommendations (Peak temperature	e) <sup>c</sup> For	For 10 s		300	°C

#### **Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b.  $V_{DD}$  = 140 V, starting  $T_J$  = 25 °C, L = 28.2 mH,  $R_q$  = 25  $\Omega$ ,  $I_{AS}$  = 3.8 A.
- c. 1.6 mm from case.
- d.  $I_{SD} \le I_D$ , dI/dt = 100 A/ $\mu$ s, starting  $T_J = 25$  °C.



# Vishay Siliconix

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	$R_{thJA}$	-	62	°C/W	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.7	C/VV	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static		-					
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> =	600	-	-	V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I <sub>D</sub> = 250 µA		-	0.72	-	V/°C
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2	-	4	V
Cata Carriaga Lagliaga		$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Gate-Source Leakage	$I_{GSS}$			-	-	± 1	μΑ
Zana Cata Valta da Busin Comunit		V <sub>DS</sub> =	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V		-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 480 \	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	10	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 11 A	-	0.156	0.180	Ω
Forward Transconductance	9 <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 11 A		-	4.8	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$ f = 1  MHz		-	1451	-	pF
Output Capacitance	C <sub>oss</sub>			-	73	-	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	5	-	
Effective Output Capacitance, Energy Related <sup>a</sup>	C <sub>o(er)</sub>	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V		-	50	-	
Effective Output Capacitance, Time Related <sup>b</sup>	C <sub>o(tr)</sub>			-	258	-	
Total Gate Charge	Qg		V <sub>GS</sub> = 10 V	-	48	96	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V		-	12	-	nC
Gate-Drain Charge	$Q_{gd}$	7			25	-	1
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 11 A,		-	19	38	- ns
Rise Time	t <sub>r</sub>			-	33	66	
Turn-Off Delay Time	t <sub>d(off)</sub>		$V_{DD} = 480 \text{ V}, T_{D} = 11 \text{ A},$ $V_{GS} = 10 \text{ V}, R_{g} = 9.1 \Omega$		45	90	
Fall Time	t <sub>f</sub>	1 3		-	21	42	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.3	0.6	1.2	Ω
<b>Drain-Source Body Diode Characteristic</b>	S						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	20	
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	49	A
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 11 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 11 A, dl/dt = 100 A/ $\mu$ s, V <sub>R</sub> = 25 V		-	319	638	ns
Reverse Recovery Charge	Q <sub>rr</sub>			-	4.9	9.8	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	28	-	A

### Notes

a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .

b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$ .



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

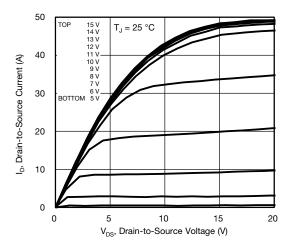


Fig. 1 - Typical Output Characteristics

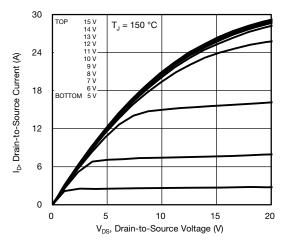


Fig. 2 - Typical Output Characteristics

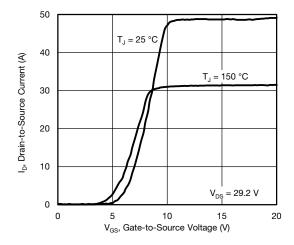


Fig. 3 - Typical Transfer Characteristics

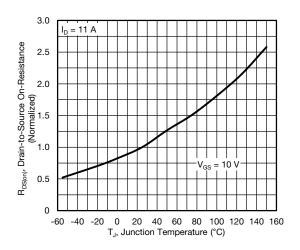


Fig. 4 - Normalized On-Resistance vs. Temperature

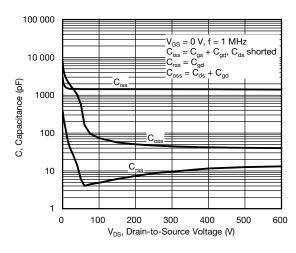


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

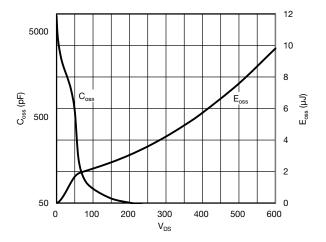


Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$ 



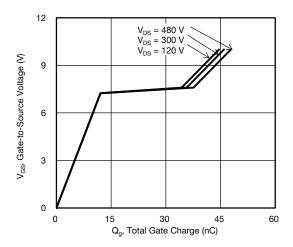


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

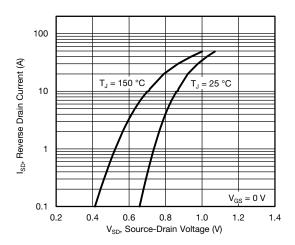


Fig. 8 - Typical Source-Drain Diode Forward Voltage

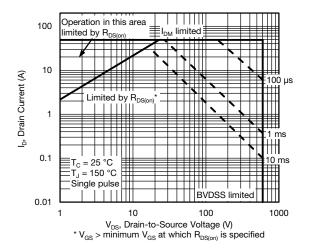


Fig. 9 - Maximum Safe Operating Area

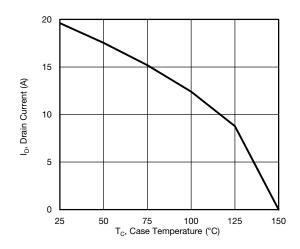


Fig. 10 - Maximum Drain Current vs. Case Temperature

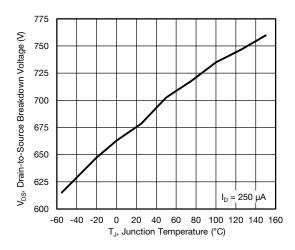


Fig. 11 - Temperature vs. Drain-to-Source Voltage



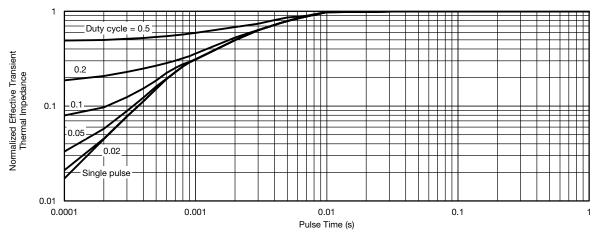


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

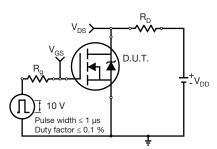


Fig. 13 - Switching Time Test Circuit

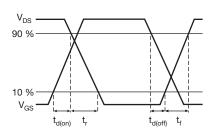


Fig. 14 - Switching Time Waveforms

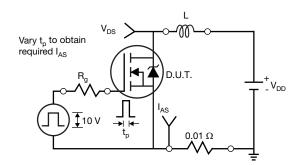


Fig. 15 - Unclamped Inductive Test Circuit

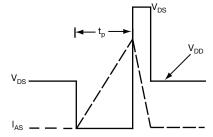


Fig. 16 - Unclamped Inductive Waveforms

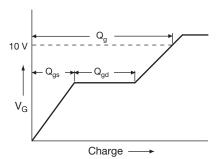


Fig. 17 - Basic Gate Charge Waveform

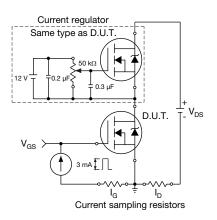
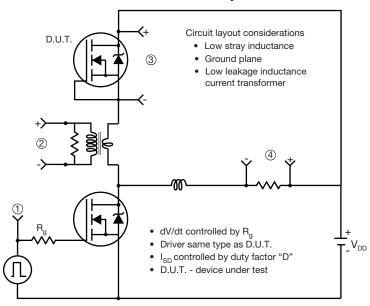


Fig. 18 - Gate Charge Test Circuit



### Peak Diode Recovery dV/dt Test Circuit



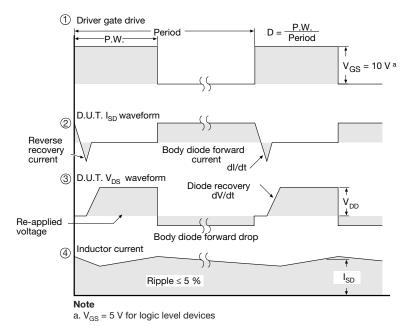


Fig. 19 - For N-Channel

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