

## EF Series Power MOSFET With Fast Body Diode

**D<sup>2</sup>PAK (TO-263)**


N-Channel MOSFET

### FEATURES

- A specific on resistance ( $m\Omega\text{-cm}^2$ ) reduction of 25 %
- Low figure-of-merit (FOM)  $R_{\text{on}} \times Q_g$
- Low input capacitance ( $C_{\text{iss}}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
 COMPLIANT  
 HALOGEN  
**FREE**

### PRODUCT SUMMARY

$V_{\text{DS}}$ (V) at $T_J$ max.	650	
$R_{\text{DS(on)}}$ typ. ( $\Omega$ ) at 25 °C	$V_{\text{GS}} = 10$ V	0.084
$Q_g$ max. (nC)	134	
$Q_{\text{gs}}$ (nC)	16	
$Q_{\text{gd}}$ (nC)	48	
Configuration	Single	

### APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### ORDERING INFORMATION

Package	D <sup>2</sup> PAK (TO-263)
Lead (Pb)-free and halogen-free	SiHB35N60EF-GE3

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)


PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{\text{DS}}$	600	V
Gate-source voltage	$V_{\text{GS}}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C)	$V_{\text{GS}}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current <sup>a</sup>	$I_{\text{DM}}$	80	
Linear derating factor		2.0	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{\text{AS}}$	298	mJ
Maximum power dissipation	$P_D$	250	W
Operating junction and storage temperature range	$T_J, T_{\text{stg}}$	-55 to +150	°C
Drain-source voltage slope	$dv/dt$	$T_J = 125$ °C	V/ns
Reverse diode $dv/dt$ <sup>d</sup>			
Soldering recommendations (peak temperature) <sup>c</sup>	For 10 s	260	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{\text{DD}} = 140$  V, starting  $T_J = 25$  °C,  $L = 28.2$  mH,  $R_g = 25$   $\Omega$ ,  $I_{\text{AS}} = 4.6$  A
- 1.6 mm from case
- $I_{\text{SD}} = 17$  A,  $di/dt = 300$  A/ $\mu$ s, starting  $T_J = 25$  °C



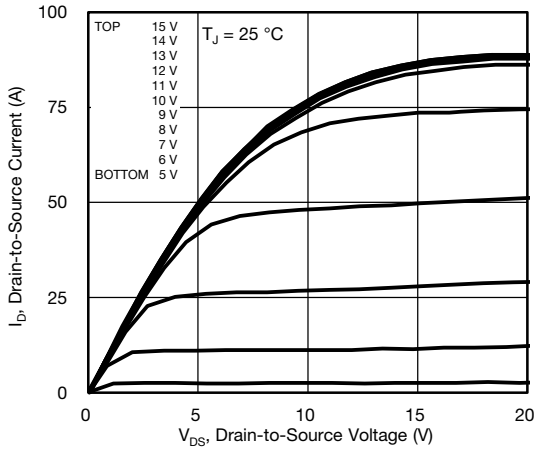
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R <sub>thJA</sub>	-	62	°C/W
Maximum junction-to-case (drain)	R <sub>thJC</sub>	-	0.5	

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		600	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 10 mA		-	0.66	-	V/°C
Gate-source threshold voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		2.0	-	4.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
		V <sub>GS</sub> = ± 30 V		-	-	± 1	μA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V		-	-	1	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C		-	-	500	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 17 A	-	0.084	0.097	Ω
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 17 A		-	8	-	S
<b>Dynamic</b>							
Input capacitance	C <sub>iSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V, f = 1 MHz		-	2568	-	pF
Output capacitance	C <sub>oss</sub>			-	113	-	
Reverse transfer capacitance	C <sub>rSS</sub>			-	7	-	
Effective output capacitance, energy related <sup>a</sup>	C <sub>o(er)</sub>			-	81	-	
Effective output capacitance, time related <sup>b</sup>	C <sub>o(tr)</sub>	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V		-	421	-	
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 17 A, V <sub>DS</sub> = 480 V	-	89	134	nC
Gate-source charge	Q <sub>gs</sub>			-	16	-	
Gate-drain charge	Q <sub>gd</sub>			-	48	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 17 A, V <sub>GS</sub> = 10 V, R <sub>g</sub> = 9.1 Ω		-	28	56	ns
Rise time	t <sub>r</sub>			-	85	170	
Turn-off delay time	t <sub>d(off)</sub>			-	96	192	
Fall time	t <sub>f</sub>			-	61	122	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.2	0.5	1.0	Ω
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	32	A
Pulsed diode forward current	I <sub>SM</sub>			-	-	80	
Diode forward voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 17 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> = 17 A, di/dt = 100 A/μs, V <sub>R</sub> = 400 V		-	150	300	ns
Reverse recovery charge	Q <sub>rr</sub>			-	1.1	2.2	μC
Reverse recovery current	I <sub>RRM</sub>			-	14	-	A

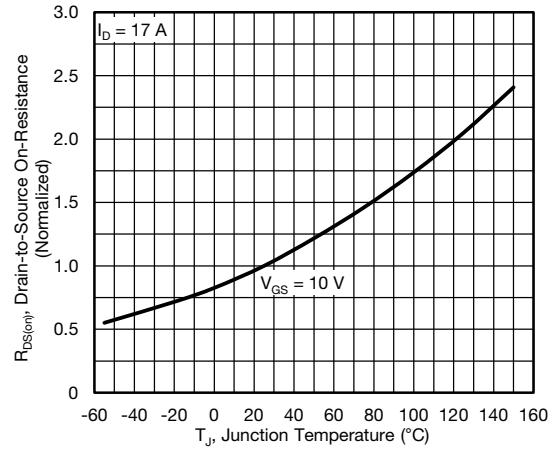
**Notes**

- a. C<sub>oss(er)</sub> is a fixed capacitance that gives the same energy as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>
- b. C<sub>oss(tr)</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DSS</sub>

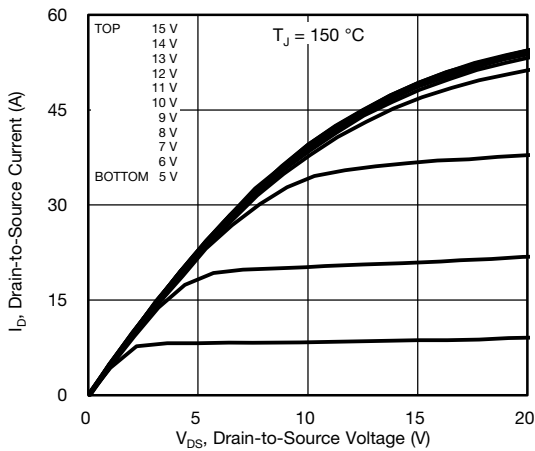
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



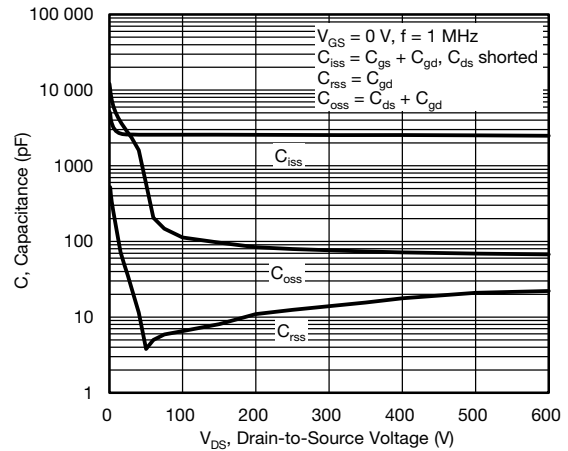
**Fig. 1 - Typical Output Characteristics**



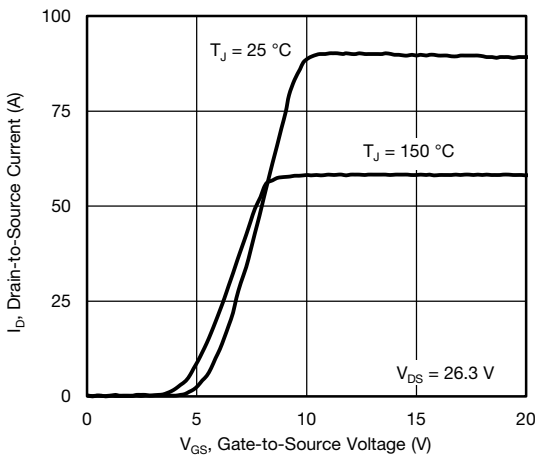
**Fig. 4 - Normalized On-Resistance vs. Temperature**



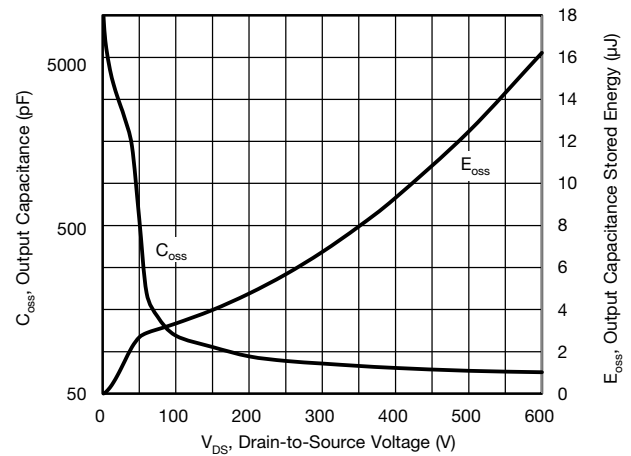
**Fig. 2 - Typical Output Characteristics**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 - C<sub>oss</sub> and E<sub>oss</sub> vs. V<sub>DS</sub>**

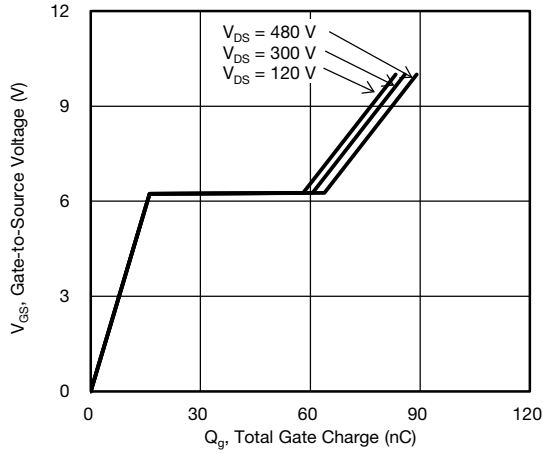


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

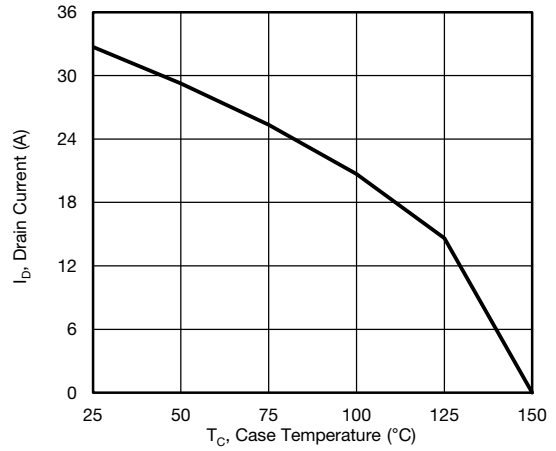


Fig. 10 - Maximum Drain Current vs. Case Temperature

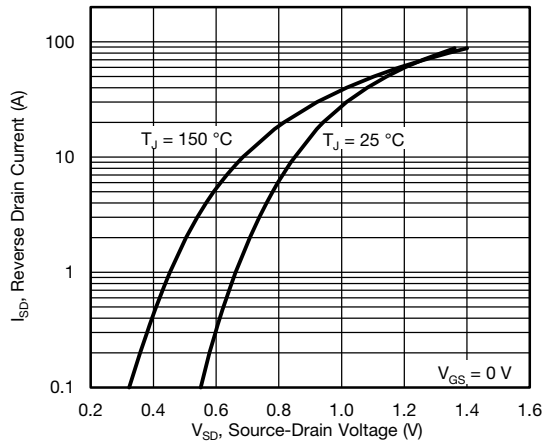


Fig. 8 - Typical Source-Drain Diode Forward Voltage

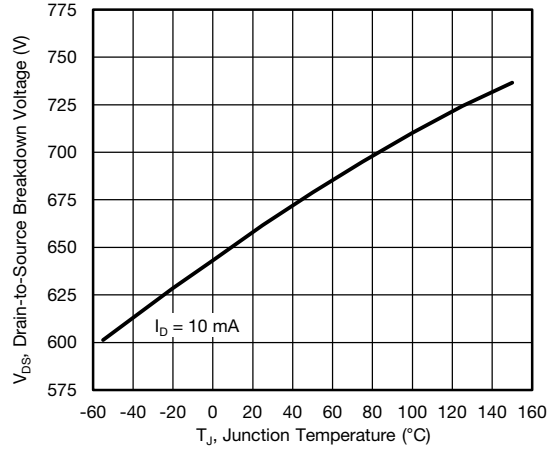


Fig. 11 - Temperature vs. Drain-to-Source Voltage

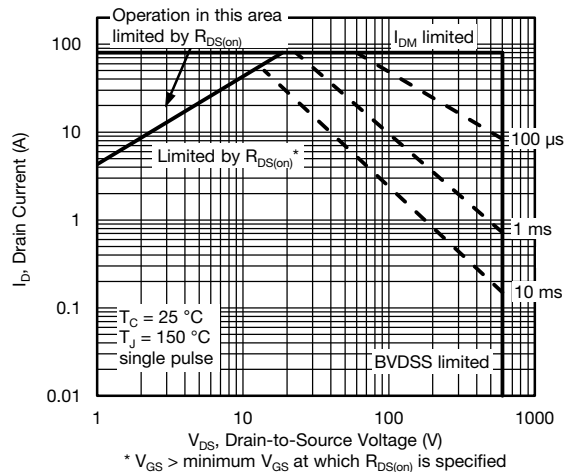


Fig. 9 - Maximum Safe Operating Area

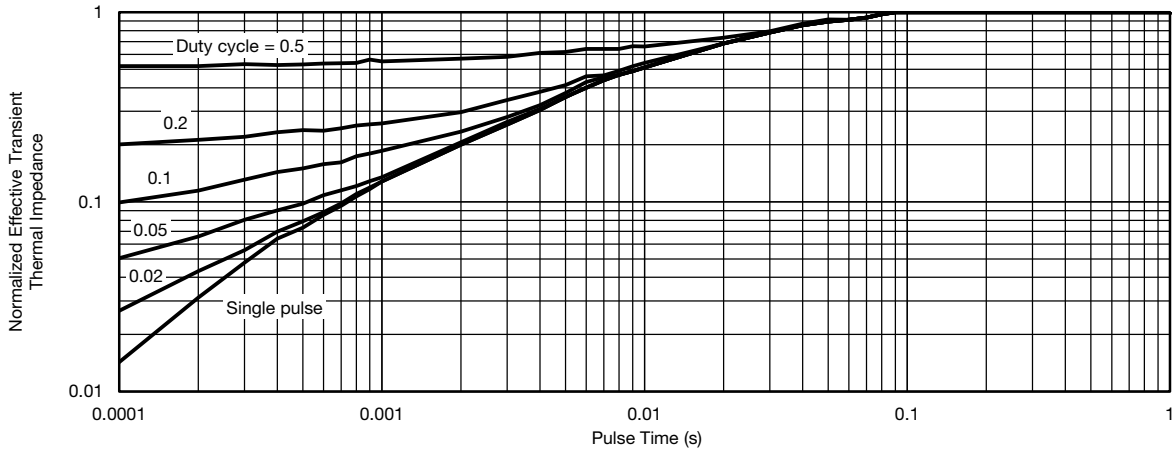


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case



Fig. 13 - Switching Time Test Circuit



Fig. 16 - Unclamped Inductive Waveforms

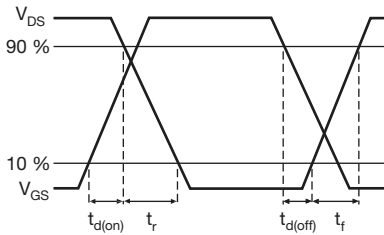


Fig. 14 - Switching Time Waveforms



Fig. 17 - Basic Gate Charge Waveform



Fig. 15 - Unclamped Inductive Test Circuit



Fig. 18 - Gate Charge Test Circuit



**Note**  
 a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 19 - For N-Channel**

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*Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?92108](http://www.vishay.com/ppg?92108).*

### TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08  
DWG: 5970

#### Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.



**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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