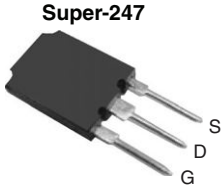
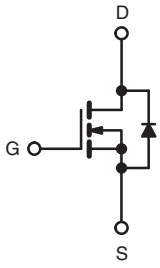
# Power MOSFET

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DS}$ (V) | 600 | |
| $R_{DS(on)}$ (Ω) | $V_{GS}$ = 10 V | 0.110 |
| $Q_g$ (Max.) (nC) | 330 | |
| $Q_{gs}$ (nC) | 84 | |
| $Q_{gd}$ (nC) | 150 | |
| Configuration | Single | |




Super-247




N-Channel MOSFET

## FEATURES

- Low Gate Charge $Q_g$ Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Enhanced Body Diode dV/dt Capability
- Compliant to RoHS Directive 2002/95/EC

Available

RoHS* COMPLIANT

## APPLICATIONS

- Hard Switching Primary or PFC Switch
- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Motor Drive

| ORDERING INFORMATION | |
|---|---|
| Package | Super-247 |
| Lead (Pb)-free | IRFPS40N60KPbF |
| | SiHFPS40N60K-E3 |
| SnPb | IRFPS40N60K |
| | SiHFPS40N60K |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|---|
| Drain-Source Voltage | | | $V_{DS}$ | 600 | V |
| Gate-Source Voltage | | | $V_{GS}$ | ± 30 | |
| Continuous Drain Current | $V_{GS}$ at 10 V | $T_C$ = 25 °C | $I_D$ | 40 | A |
| | | $T_C$ = 100 °C | | 24 | |
| Pulsed Drain Current[a] | | | $I_{DM}$ | 160 | |
| Linear Derating Factor | | | | 4.5 | W/°C |
| Single Pulse Avalanche Energy[b] | | | $E_{AS}$ | 600 | mJ |
| Repetitive Avalanche Current[a] | | | $I_{AR}$ | 40 | A |
| Repetitive Avalanche Energy[a] | | | $E_{AR}$ | 57 | mJ |
| Maximum Power Dissipation | $T_C$ = 25 °C | | $P_D$ | 570 | W |
| Peak Diode Recovery dV/dt[c] | | | dV/dt | 7.5 | V/ns |
| Operating Junction and Storage Temperature Range | | | $T_J$, $T_{stg}$ | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) | for 10 s | | | 300[d] | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting $T_J$ = 25 °C, L = 0.84 mH, $R_g$ = 25 Ω, $I_{AS}$ = 38 A, dV/dt = 5.5 V/ns (see fig. 12a).
c. $I_{SD} \leq$ 38 A, dI/dt ≤ 150 A/µs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

| THERMAL RESISTANCE RATINGS | | | | |
|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TYP.** | **MAX.** | **UNIT** |
| Maximum Junction-to-Ambient | $R_{thJA}$ | - | 40 | °C/W |
| Case-to-Sink, Flat, Greased Surface | $R_{thCS}$ | 0.24 | - | |
| Maximum Junction-to-Case (Drain) | $R_{thJC}$ | - | 0.22 | |

**SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| **Static** | | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | | 600 | - | - | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to 25 °C, $I_D$ = 1 mA | | - | 0.63 | - | V/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 3.0 | - | 5.0 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{GS}$ = ± 30 V | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 600 V, $V_{GS}$ = 0 V | | - | - | 50 | µA |
| | | $V_{DS}$ = 480 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 24 A[b] | - | 0.110 | 0.130 | Ω |
| Forward Transconductance | $g_{fs}$ | $V_{DS}$ = 50 V, $I_D$ = 24 A[b] | | 21 | - | - | S |
| **Dynamic** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 25 V, f = 1.0 MHz, see fig. 5 | | - | 7970 | - | pF |
| Output Capacitance | $C_{oss}$ | | | - | 750 | - | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 75 | - | |
| Output Capacitance | $C_{oss}$ | $V_{GS}$ = 0 V | $V_{DS}$ = 1.0 V , f = 1.0 MHz | - | 9440 | - | |
| | | | $V_{DS}$ = 480 V , f = 1.0 MHz | - | 200 | - | |
| Effective Output Capacitance | $C_{oss}$ eff. | | $V_{DS}$ = 0 V to 480 V[c] | - | 260 | - | |
| Total Gate Charge | $Q_g$ | $V_{GS}$ = 10 V | $I_D$ = 38 A, $V_{DS}$ = 480 V, see fig. 6 and 13[b] | - | - | 330 | nC |
| Gate-Source Charge | $Q_{gs}$ | | | - | - | 84 | |
| Gate-Drain Charge | $Q_{gd}$ | | | - | - | 150 | |
| Turn-On Delay Time | $t_{d(on)}$ | | $V_{DD}$ = 300 V, $I_D$ = 38 A, $R_G$ = 4.3 Ω, see fig. 10[b] | - | 47 | - | ns |
| Rise Time | $t_r$ | | | - | 110 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 97 | - | |
| Fall Time | $t_f$ | | | - | 60 | - | |
| **Drain-Source Body Diode Characteristics** | | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 40 | A |
| Pulsed Diode Forward Current[a] | $I_{SM}$ | | | - | - | 160 | |
| Body Diode Voltage | $V_{SD}$ | $T_J$ = 25 °C, $I_S$ = 38 A, $V_{GS}$ = 0 V[b] | | - | - | 1.5 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $T_J$ = 25 °C | $I_F$ = 38 A, dI/dt = 100 A/µs | - | 630 | 950 | ns |
| | | $T_J$ = 125 °C | | - | 730 | 1090 | |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | $T_J$ = 25 °C | | - | 14 | 20 | µC |
| | | $T_J$ = 125 °C | | - | 17 | 25 | |
| Body Diode Recovery Current | $I_{RRM}$ | $T_J$ = 25 °C | | - | 39 | 58 | A |
| Forward Turn-On Time | $t_{on}$ | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$) | | | | | |

**Notes**

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

c. $C_{oss}$ eff. is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 % to 80 % $V_{DS}$.

## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

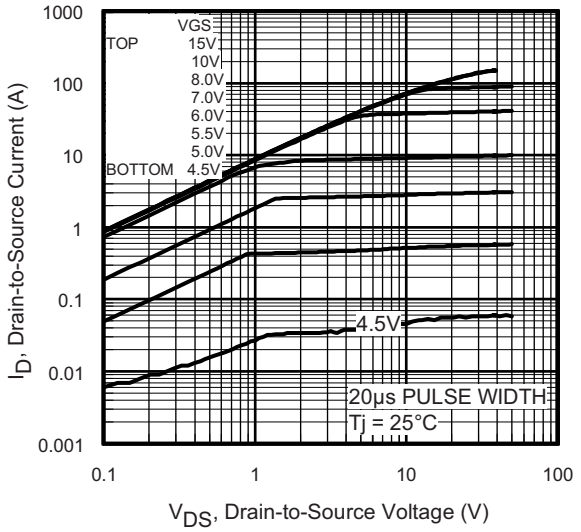



**Fig. 1 - Typical Output Characteristics**

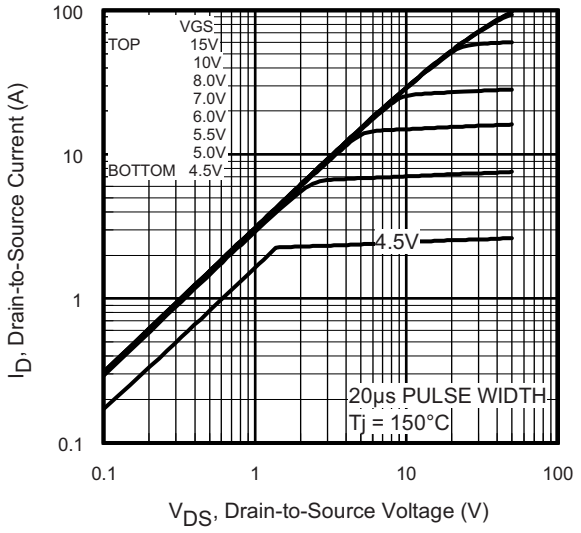



**Fig. 2 - Typical Output Characteristics**

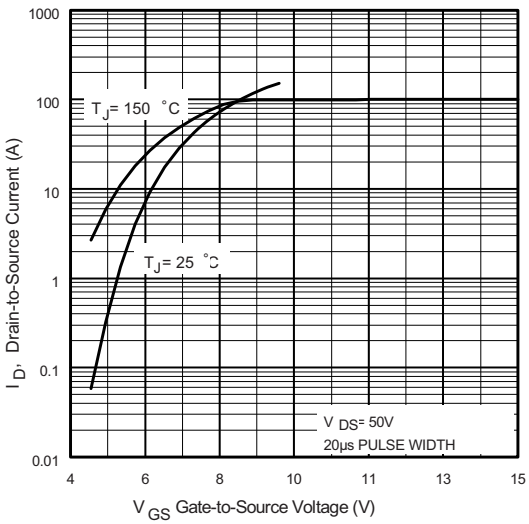



**Fig. 3 - Typical Transfer Characteristics**

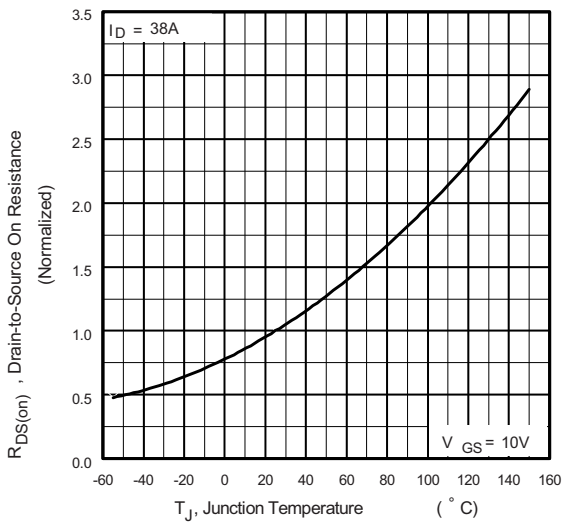



**Fig. 4 - Normalized On-Resistance vs. Temperature**

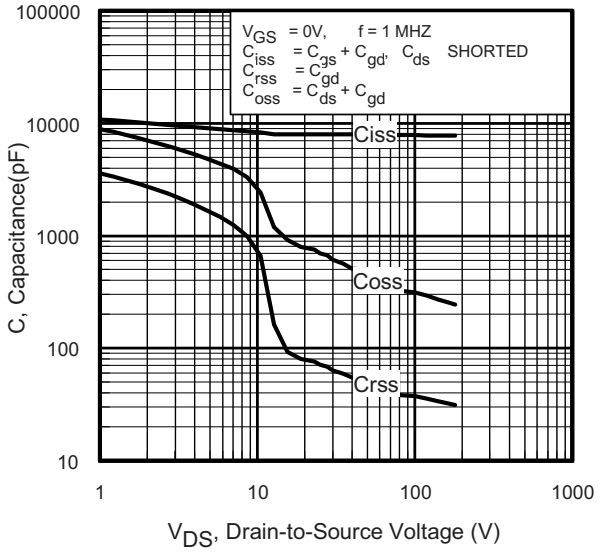



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

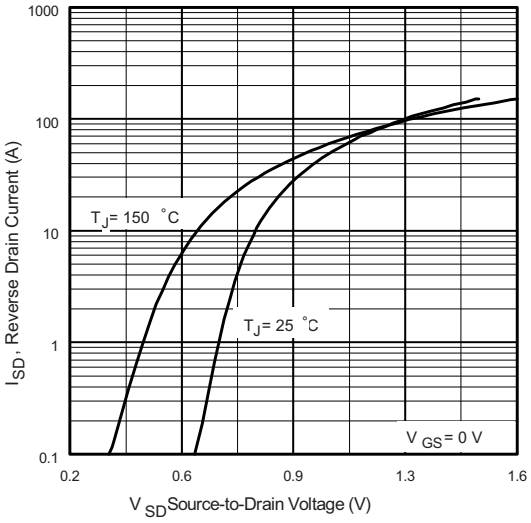



**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

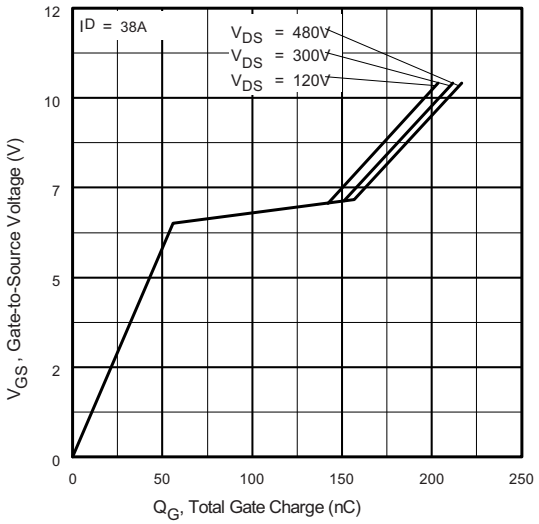



**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

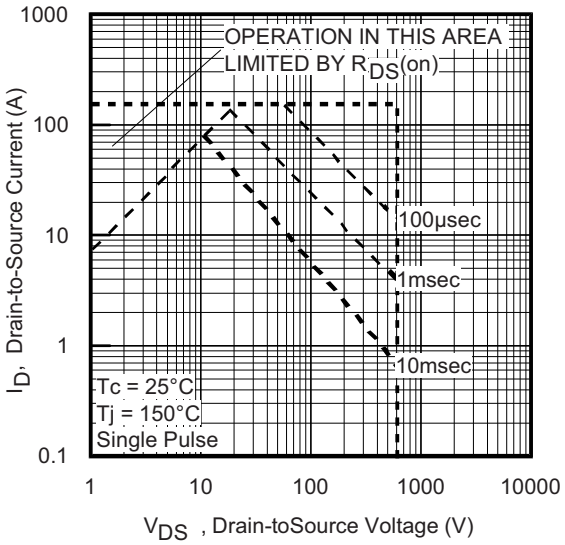



**Fig. 8 - Maximum Safe Operating Area**

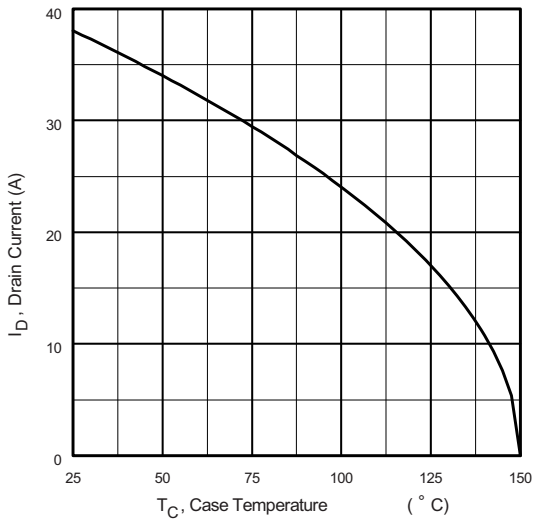



**Fig. 9 - Maximum Drain Current vs. Case Temperature**

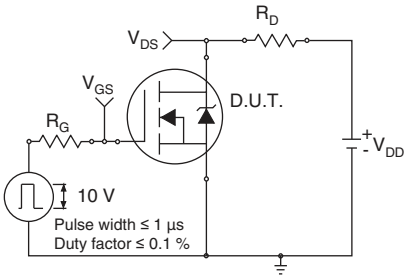



**Fig. 10a - Switching Time Test Circuit**

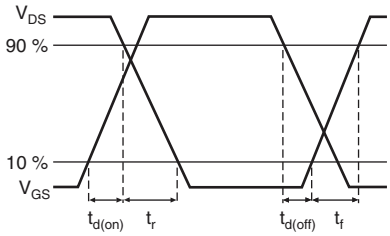



**Fig. 10b - Switching Time Waveforms**

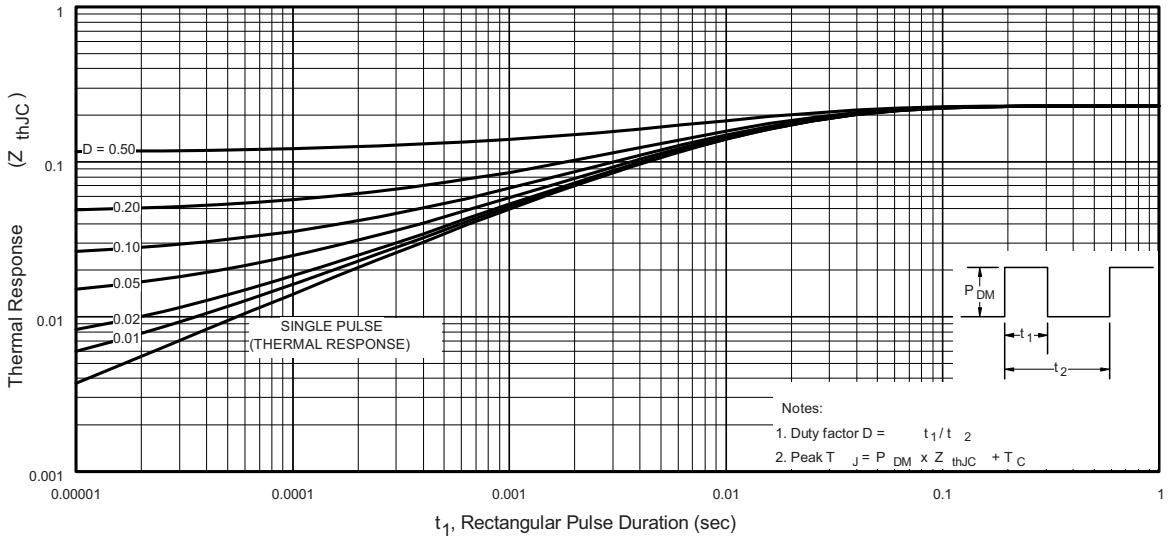



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

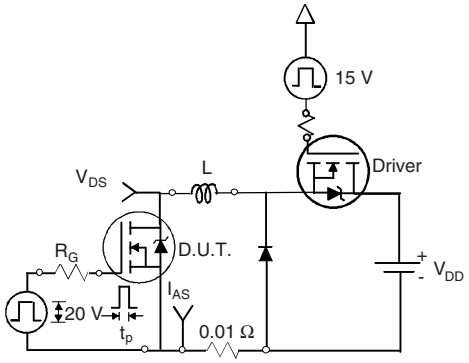



**Fig. 12a - Unclamped Inductive Test Circuit**

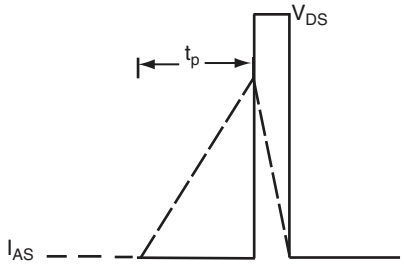



**Fig. 12b - Unclamped Inductive Waveforms**

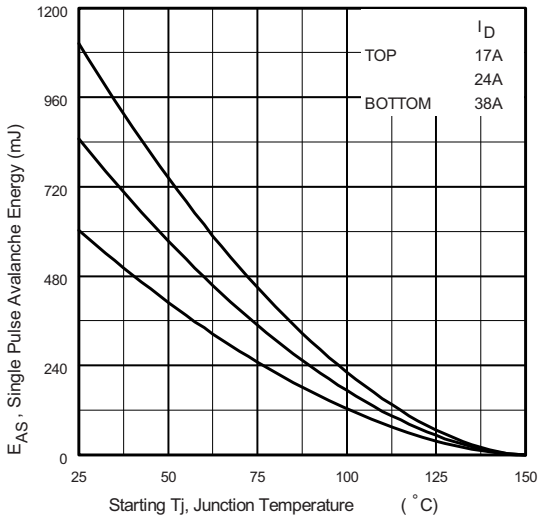



**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

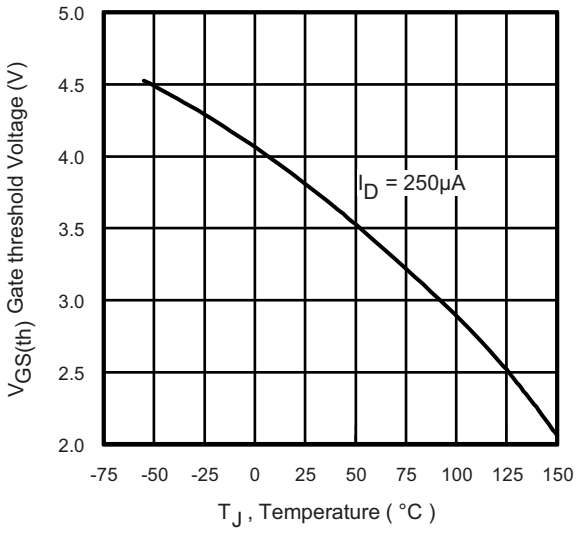



**Fig. 12d - Threshold Voltage vs. Temperature**

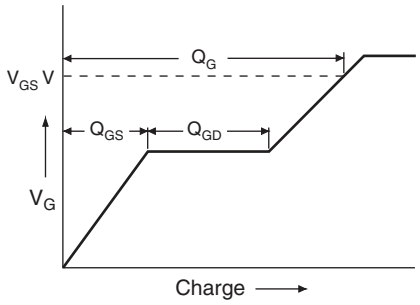



**Fig. 13a - Basic Gate Charge Waveform**

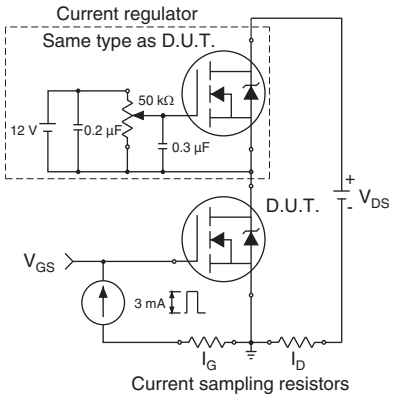
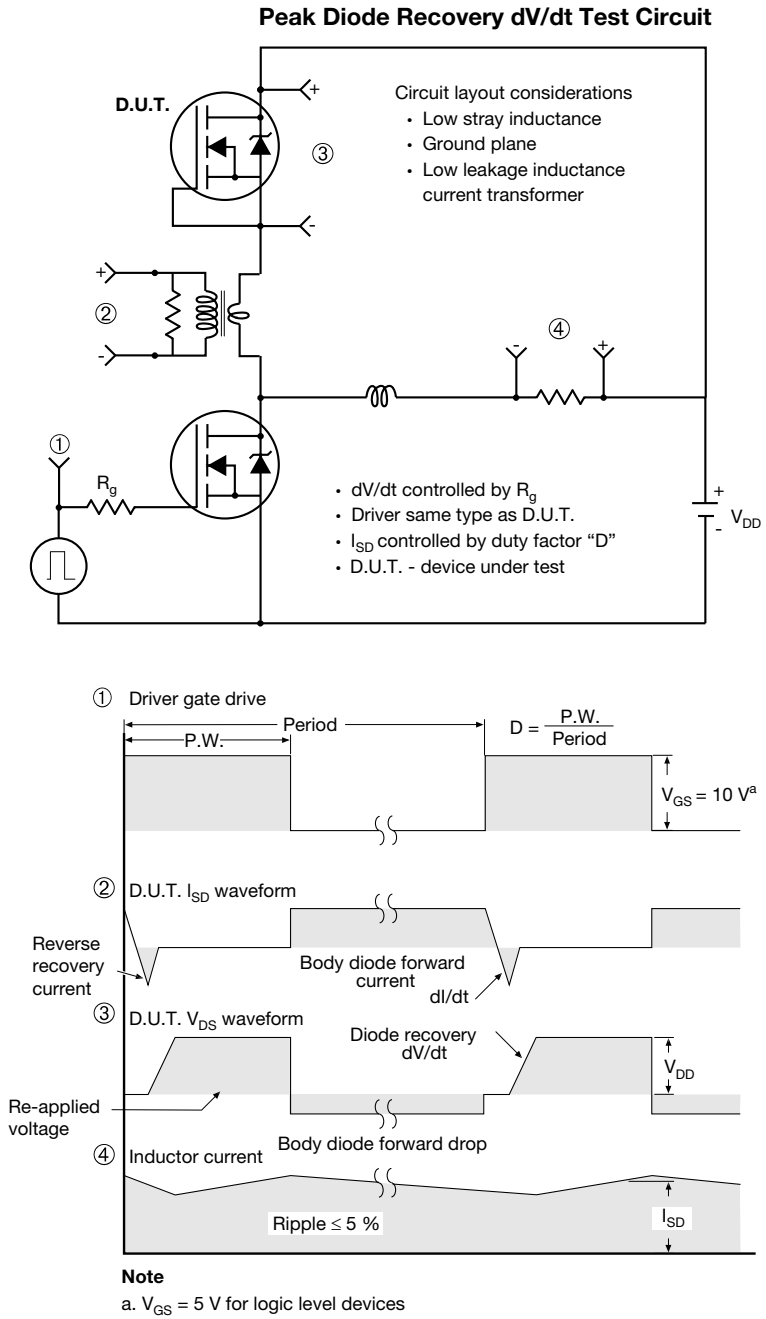



**Fig. 13b - Gate Charge Test Circuit**




**Note**

a. $V_{GS}$ = 5 V for logic level devices

**Fig. 14 - For N-Channel**

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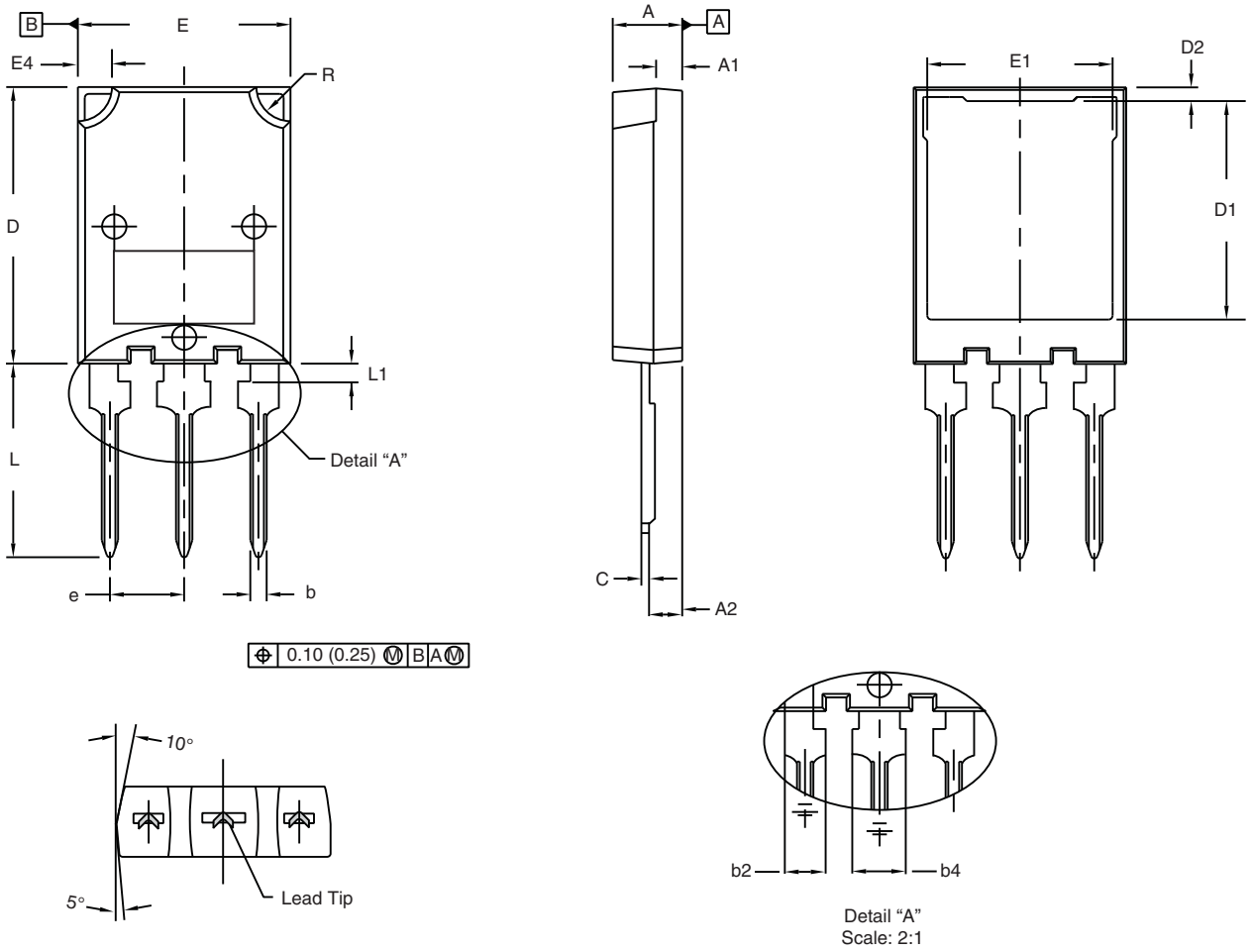
# TO-274AA (High Voltage)




| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| A | 4.70 | 5.30 | 0.185 | 0.209 |
| A1 | 1.50 | 2.50 | 0.059 | 0.098 |
| A2 | 2.25 | 2.65 | 0.089 | 0.104 |
| b | 1.30 | 1.60 | 0.051 | 0.063 |
| b2 | 1.80 | 2.20 | 0.071 | 0.087 |
| b4 | 3.00 | 3.25 | 0.118 | 0.128 |
| c (1) | 0.38 | 0.89 | 0.015 | 0.035 |
| D | 19.80 | 20.80 | 0.780 | 0.819 |

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM. | MIN. | MAX. | MIN. | MAX. |
| D1 | 15.50 | 16.10 | 0.610 | 0.634 |
| D2 | 0.70 | 1.30 | 0.028 | 0.051 |
| E | 15.10 | 16.10 | 0.594 | 0.634 |
| E1 | 13.30 | 13.90 | 0.524 | 0.547 |
| e | 5.45 BSC | | 0.215 BSC | |
| L | 13.70 | 14.70 | 0.539 | 0.579 |
| L1 | 1.00 | 1.60 | 0.039 | 0.063 |
| R | 2.00 | 3.00 | 0.079 | 0.118 |

ECN: X17-0056-Rev. B, 27-Mar-17
DWG: 5975

**Notes**

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA

(1) Dimension measured at tip of lead

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