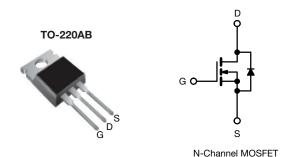
Vishay Siliconix

HALOGEN

FREE

E Series Power MOSFET



PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	650			
R _{DS(on)} typ. (Ω) at 25 °C	V _{GS} = 10 V	0.104		
Q _g max. (nC)	45			
Q _{gs} (nC)	10			
Q _{gd} (nC)	12			
Configuration	Single			

FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) Ron x Qg
- Low effective capacitance (Co(er))
- · Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- · Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free and halogen-free	SiHP120N60E-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-source voltage			V _{DS}	600		
Gate-source voltage			V_{GS}	± 30	V	
Continuous drain current (T _J = 150 °C)	V _{GS} at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	- I _D	25	1	
		T _C = 100 °C		16	Α	
Pulsed drain current ^a			I _{DM}	66		
Linear derating factor				1.4	W/°C	
Single pulse avalanche energy b			E _{AS}	88	mJ	
Maximum power dissipation			P_{D}	179	W	
Operating junction and storage temperature range			T _J , T _{stg}	-55 to +150	°C	
Drain-source voltage slope	T _J = 125 °C		dv/dt	70	1//20	
Reverse diode dv/dt d	se diode dv/dt ^d			50	V/ns	
Soldering recommendations (peak temperature) ^c	For	10 s		260	°C	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. V_{DD} = 120 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 2.5 A
- c. 1.6 mm from case
- d. $I_{SD} \le I_D$, di/dt = 100 A/ μ s, starting $T_J = 25$ °C



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W	
Maximum junction-to-case (drain)	R_{thJC}	-	0.7	C/VV	

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} =	600	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Reference to 25 °C, I _D = 1 mA		-	0.67	-	V/°C
Gate-source threshold voltage (N)	V _{GS(th)}	V _{DS} =	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		-	5.0	V
Cata acuraa laakaga	1	V _{GS} = ± 20 V		-	-	± 100	nA
Gate-source leakage	I_{GSS}	,	$V_{GS} = \pm 30 \text{ V}$		-	± 1	μΑ
Z		V _{DS} =	$V_{DS} = 600 \text{ V}, V_{GS} = 0 \text{ V}$		-	1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 480 V	, V _{GS} = 0 V, T _J = 125 °C	-	-	10	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 12 A	-	0.104	0.120	Ω
Forward transconductance ^a	9 _{fs}	V _{DS}	= 20 V, I _D = 12 A	-	6	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V,		-	1562	-	
Output capacitance	C _{oss}	Ţ,	$V_{DS} = 100 \text{ V},$		72	-	
Reverse transfer capacitance	C _{rss}	f = 1 MHz		-	6	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{DS} = 0 V to 480 V, V _{GS} = 0 V		-	56	-	pF
Effective output capacitance, time related ^b	C _{o(tr)}			-	357	-	
Total gate charge	Qg			-	30	45	
Gate-source charge	Q_{gs}	$V_{GS} = 10 \text{ V}$	$V_{GS} = 10 \text{ V}$ $I_D = 12 \text{ A}, V_{DS} = 480 \text{ V}$		10	-	nC
Gate-drain charge	Q_{gd}			-	12	-]
Turn-on delay time	t _{d(on)}	V _{DD} = 480 V, I _D = 12 A,		-	19	38	- ns
Rise time	t _r			-	65	130	
Turn-off delay time	t _{d(off)}	V _{GS} =	$V_{GS} = 10 \text{ V}, R_g = 9.1 \Omega$		31	62	
Fall time	t _f			-	33	66	
Gate input resistance	R_g	f = 1 MHz, open drain		0.3	0.65	1.3	Ω
Drain-Source Body Diode Characteristic	es						
Continuous source-drain diode current	I _S	showing the	MOSFET symbol showing the		-	25	
Pulsed diode forward current	I _{SM}	integral reverse p - n junction diode		-	-	66	A
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 12 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}		3 1 1 7 3 1 1 1 1 G		322	870	ns
Reverse recovery charge	Q _{rr}	$T_J = 25 ^{\circ}\text{C}$, $I_F = I_S = 12 \text{A}$, $di/dt = 100 \text{A/}\mu\text{s}$, $V_R = 400 \text{V}$		-	4.9	18.4	μC
Reverse recovery current	I _{RRM}			_	29	-	A

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
- b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

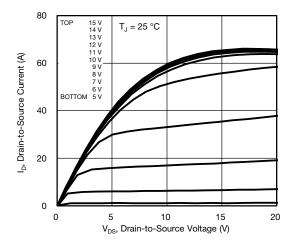


Fig. 1 - Typical Output Characteristics

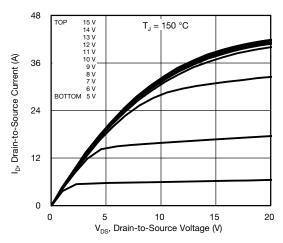


Fig. 2 - Typical Output Characteristics

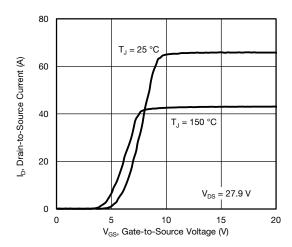


Fig. 3 - Typical Transfer Characteristics

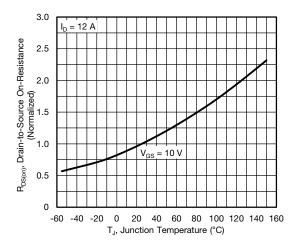


Fig. 4 - Normalized On-Resistance vs. Temperature

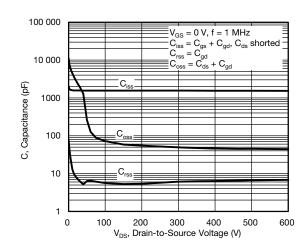


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

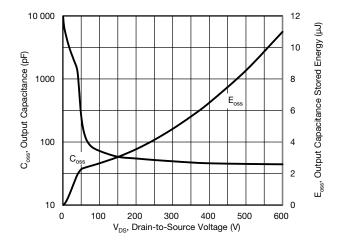


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}



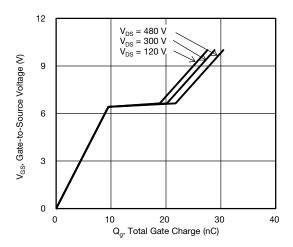


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

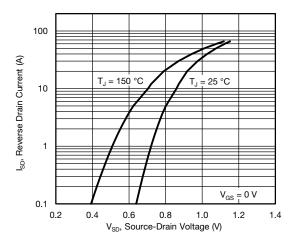


Fig. 8 - Typical Source-Drain Diode Forward Voltage

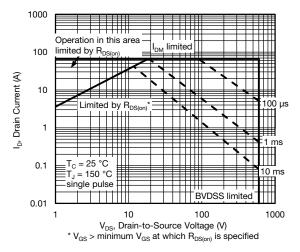


Fig. 9 - Maximum Safe Operating Area

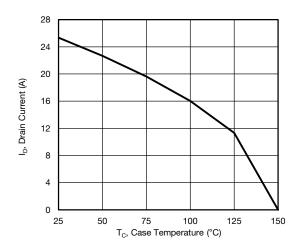


Fig. 10 - Maximum Drain Current vs. Case Temperature

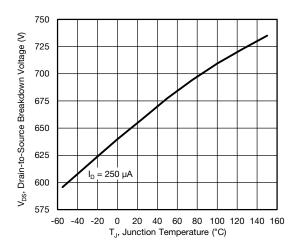


Fig. 11 - Temperature vs. Drain-to-Source Voltage



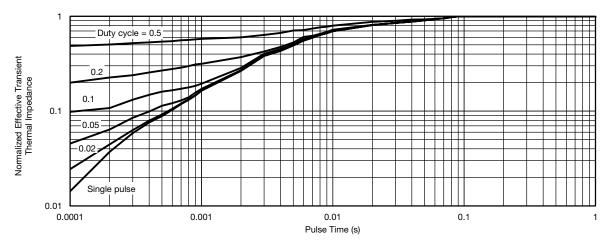


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

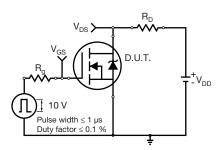


Fig. 13 - Switching Time Test Circuit

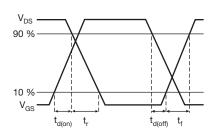


Fig. 14 - Switching Time Waveforms

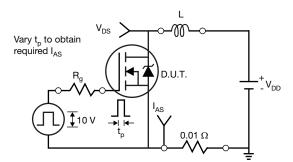


Fig. 15 - Unclamped Inductive Test Circuit

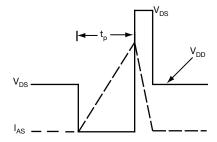


Fig. 16 - Unclamped Inductive Waveforms

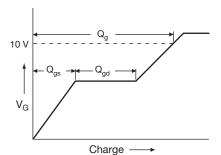


Fig. 17 - Basic Gate Charge Waveform

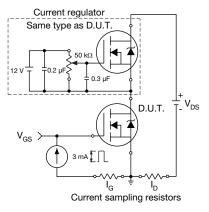
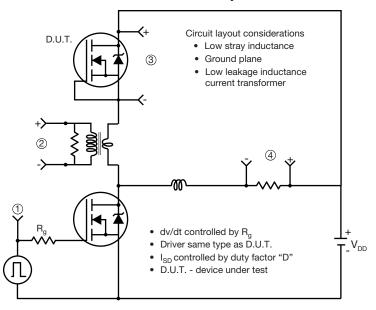


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



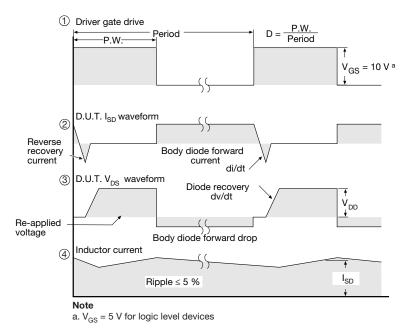


Fig. 19 - For N-Channel

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