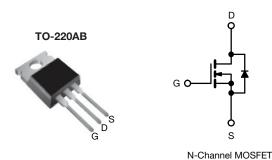
Vishay Siliconix

E Series Power MOSFET



PRODUCT SUMMA	RY	
V _{DS} (V) at T _J max.	550)
R _{DS(on)} max. at 25 °C (Ω)	V _{GS} = 10 V	0.243
Q _g max. (nC)	66	i
Q _{gs} (nC)	8	
Q _{gd} (nC)	14	
Configuration	Sing	le

FEATURES

- Low figure-of-merit (FOM) Ron x Qq
- Low input capacitance (Ciss)
- · Reduced switching and conduction losses
- Low gate charge (Qq)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



APPLICATIONS

- Computing
 - PC silver box / ATX power supplies
- Lighting
 - Two stage LED lighting
- Consumer electronics
- · Applications using hard switched topologies
 - Power factor correction (PFC)
 - Two switch forward converter
 - Flyback converter
- Switch mode power supplies (SMPS)

ORDERING INFORMATION	
Package	TO-220AB
Load (Dh) free and halogen free	SiHP15N50E-BE3
Lead (Pb)-free and halogen-free	SiHP15N50E-GE3

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	500	V		
Gate-Source Voltage			V_{GS}	± 30	V	
Continuous Drain Current /T = 150 °C\	V _{GS} at 10 V	T _C = 25 °C T _C = 100 °C	,	14.5		
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	T _C = 100 °C	I _D	9.2	Α	
Pulsed Drain Current ^a I _{DM} 28		28				
Linear Derating Factor				1.25	W/°C	
Single Pulse Avalanche Energy b			E _{AS}	136	mJ	
Maximum Power Dissipation		P _D	156	W		
Operating Junction and Storage Temperature Range	Э		T _J , T _{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	$V_{DS} = 0 V t$	o 80 % V _{DS}	dV/dt	70	1//20	
Reverse Diode dV/dt ^d			uv/at	27	- V/ns	
Soldering Recommendations (Peak Temperature) c for 10 s			300	°C		

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 3.1 A
- c. 1.6 mm from case
- d. $I_{SD} \le I_D$, $dI/dt = 100 \text{ A/}\mu\text{s}$, starting $T_J = 25 \,^{\circ}\text{C}$



Vishay Siliconix

THERMAL RESISTANCE RAT	INGS			
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	62	°C/W
Maximum junction-to-case (drain)	R _{thJC}	-	0.8	G/ VV

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static		_				•	L
Drain-source breakdown voltage	V _{DS}	V _{GS} =	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	Referenc	e to 25 °C, I _D = 1 mA	-	0.62	-	V/°C
Gate-source threshold Voltage (N)	V _{GS(th)}	V _{DS} =	V_{GS} , $I_{D} = 250 \mu A$	2.0	-	4.0	V
		V _{GS} = ± 20 V		-	-	± 100	nA
Gate-source leakage	I _{GSS}	1	$I_{GS} = \pm 30 \text{ V}$	-	-	± 1	μΑ
Zana anto coltano dunio accument		V _{DS} =	500 V, V _{GS} = 0 V	-	-	10	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 400 V	, V _{GS} = 0 V, T _J = 125 °C	-	-	25	μA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 7.5 A	-	0.243	0.280	Ω
Forward transconductance	9 _{fs}	V _{DS} =	= 30 V, I _D = 7.5 A	-	3.9	-	S
Dynamic					-		
Input capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$ $f = 1 \text{ MHz}$		-	1162	-	pF
Output capacitance	C _{oss}			-	51	-	
Reverse transfer capacitance	C _{rss}			-	7	-	
Effective output capacitance, energy related ^a	C _{o(er)}	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		-	55	-	
Effective output capacitance, time related ^b	C _{o(tr)}			-	164	-	
Total gate charge	Qg			-	33	66	
Gate-source charge	Q_{gs}	$V_{GS} = 10 \text{ V}$ $I_D = 7.5 \text{ A}, V_{DS} = 400 \text{ V}$		-	8	-	nC
Gate-drain charge	Q _{gd}	7		-	14	-	
Turn-on delay time	t _{d(on)}	V _{DD} = 400 V, I _D = 12 A,		-	15	30	ns
Rise time	t _r			-	24	48	
Turn-off delay time	t _{d(off)}	V _{GS} =	$V_{GS} = 10 \text{ V}, R_g = 9.1 \Omega$		34	68	
Fall time	t _f	1		-	18	36	
Gate input resistance	R_g	f = 1 MHz, open drain		-	0.85	-	Ω
Drain-Source Body Diode Characteristic	s						
Continuous source-drain diode current	Is	MOSFET symbol showing the integral reverse p - n junction diode		-	-	14.5	
Pulsed diode forward current	I _{SM}			-	-	28	A
Diode forward voltage	V _{SD}	T _J = 25 °C, I _S = 7.5 A, V _{GS} = 0 V		-	-	1.2	V
Reverse recovery time	t _{rr}			-	265	-	ns
Reverse recovery charge	Q _{rr}	T _J = 25 °C, I _F = I _{S = 7.5 A} , dl/dt = 100 A/ μ s, V _R = 25 V		-	3.2	-	μC
Reverse recovery current	I _{RRM}			_	23	_	A

- e. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} f. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

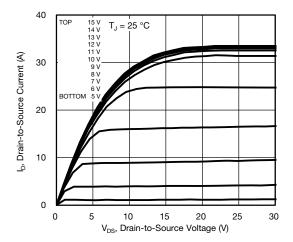


Fig. 1 - Typical Output Characteristics

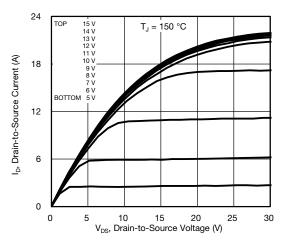


Fig. 2 - Typical Output Characteristics

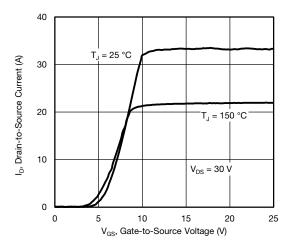


Fig. 3 - Typical Transfer Characteristics

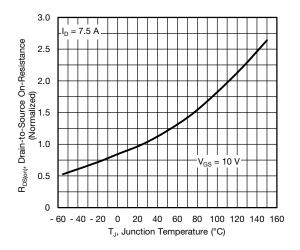


Fig. 4 - Normalized On-Resistance vs. Temperature

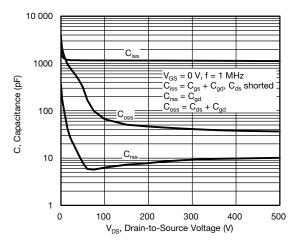


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

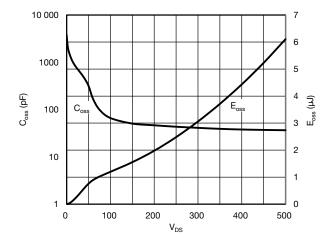


Fig. 6 - Coss and Eoss vs. VDS



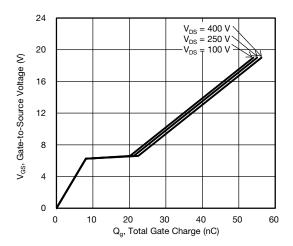


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

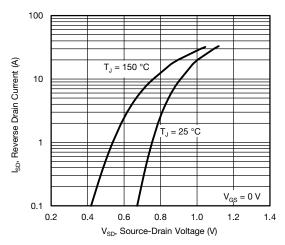


Fig. 8 - Typical Source-Drain Diode Forward Voltage

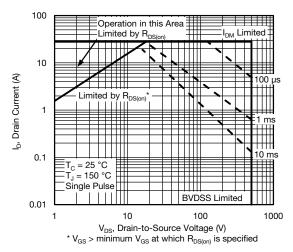


Fig. 9 - Maximum Safe Operating Area

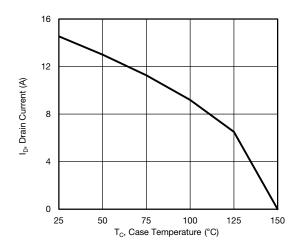


Fig. 10 - Maximum Drain Current vs. Case Temperature

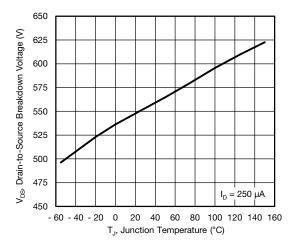


Fig. 11 - Temperature vs. Drain-to-Source Voltage



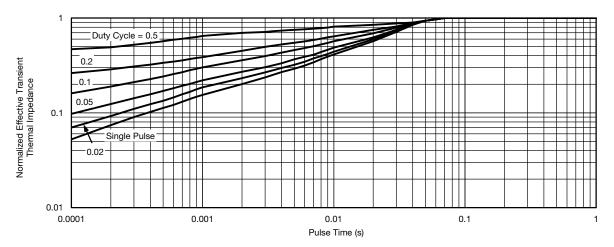


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

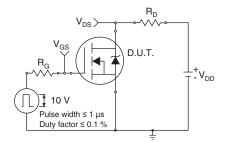


Fig. 13 - Switching Time Test Circuit

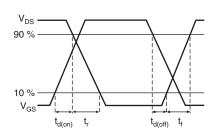


Fig. 14 - Switching Time Waveforms

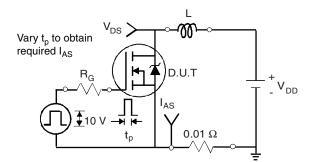


Fig. 15 - Unclamped Inductive Test Circuit

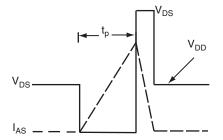


Fig. 16 - Unclamped Inductive Waveforms

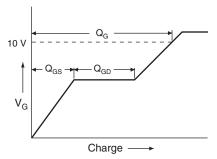


Fig. 17 - Basic Gate Charge Waveform

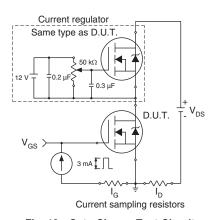
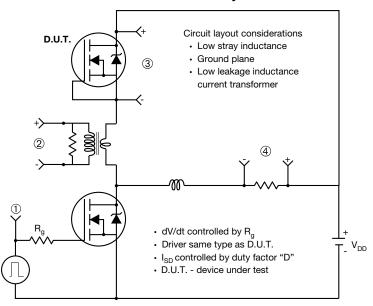


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



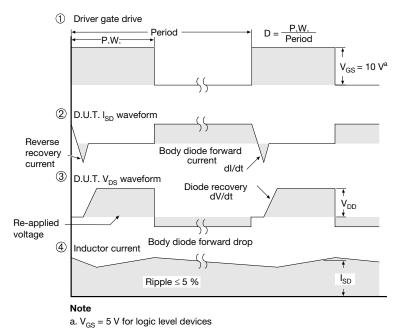


Fig. 19 - For N-Channel

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TO-220-1



DIM.	MILLIM	IETERS	INCHES		
	MIN.	MAX.	MIN.	MAX.	
Α	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
Е	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØΡ	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	

Note

DWG: 6031

• $M^* = 0.052$ inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM



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Vishay

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