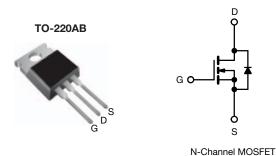
SiHP15N60E





E Series Power MOSFET

PRODUCT SUMMARY					
V _{DS} (V) at T _J max.	650				
R _{DS(on)} max. (Ω) at 25 °C	V _{GS} = 10 V 0.28				
Q _g max. (nC)	78				
Q _{gs} (nC)	9				
Q _{gd} (nC)	17				
Configuration	Single				



FEATURES

- Low figure-of-merit (FOM) $R_{\text{on}} \ x \ Q_{g}$
- Low input capacitance (Ciss)
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Renewable energy
 - Solar (PV inverters)

ORDERING INFORMATION				
Package	TO-220AB			
Lead (Pb)-free	SiHP15N60E-E3			
Lead (Pb)-free and Halogen-free	SiHP15N60E-GE3			

ABSOLUTE MAXIMUM RATINGS ($T_c = 25 \degree C$, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V _{DS}	600	V	
Gate-Source Voltage			V _{GS}	± 30	v	
Continuous Drain Current (T _J = 150 °C)	V _{GS} at 10 V	$T_{\rm C} = 25 \ ^{\circ}{\rm C}$ $T_{\rm C} = 100 \ ^{\circ}{\rm C}$	- I _D	15		
	V _{GS} at 10 V	T _C = 100 °C		9.6	A	
Pulsed Drain Current ^a			I _{DM}	39		
Linear Derating Factor				1.4	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	102	mJ	
Maximum Power Dissipation			PD	180	W	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	$V_{DS} = 0 V \text{ to } 80 \% V_{DS}$		d\//dt	70	V/ns	
Reverse Diode dV/dt ^d			dV/dt	7.7	v/fis	
Soldering Recommendations (Peak temperature) c for 10 s				300	°C	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.

b. V_{DD} = 50 V, starting T_J = 25 °C, L = 11.6 mH, R_g = 25 $\Omega,\,I_{AS}$ = 4.2 A.

c. 1.6 mm from case.

d. $I_{SD} \leq I_D, \, dI/dt$ = 100 A/µs, starting T_J = 25 °C.

1

Document Number: 91478



COMPLIANT HALOGEN

FREE



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THERMAL RESISTANCE RATINGS								
PARAMETER	SYMBOL	TYP.		MAX.		UNIT		
Maximum Junction-to-Ambient	R _{thJA}	- 62			0000			
Maximum Junction-to-Case (Drain)	R _{thJC}	- 0.7				°C/W		
SPECIFICATIONS (T _J = 25 °C, u	unless otherwi	se noted)						
PARAMETER	SYMBOL	1	T CONDIT	IONS	MIN.	TYP.	MAX.	UNIT
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} =	= 0 V, I _D =	250 µA	600	-	-	V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			I _D = 1 mA	-	0.71	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D =	250 µA	2	-	4	V
		$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA	
Gate-Source Leakage	IGSS		$V_{GS} = \pm 30$	V	-	-	± 1	μA
Zoro Cato Voltago Drain Current		V _{DS} =	= 600 V, V ₀	_{as} = 0 V	-	-	1	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 480 V	V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	10	μA
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V		I _D = 8 A	-	0.23	0.28	Ω
Forward Transconductance	9 _{fs}	V _{DS}	= 30 V, I _D	= 8 A	-	4.6	-	S
Dynamic								-
Input Capacitance	C _{iss}	$V_{GS} = 0 V,$ $V_{DS} = 100 V,$ f = 1 MHz		-	1350	-	-	
Output Capacitance	C _{oss}			-	70	-		
Reverse Transfer Capacitance	C _{rss}			-	5	-		
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	V_{DS} = 0 V to 480 V, V_{GS} = 0 V		-	53	-	pF	
Effective Output Capacitance, Time Related ^b	C _{o(tr)}			-	177	-		
Total Gate Charge	Qg	V _{GS} = 10 V I _D = 8 A, V _{DS} = 480 V		-	39	78	nC	
Gate-Source Charge	Q _{gs}			-	11	-		
Gate-Drain Charge	Q _{gd}				-	17	-	1
Turn-On Delay Time	t _{d(on)}				-	16	32	
Rise Time	t _r	Voo	– 480 V I-	- 8 A	-	26	52	1 20
Turn-Off Delay Time	t _{d(off)}	V_{DD} = 480 V, I_D = 8 A, V_{GS} = 10 V, R_g = 9.1 Ω		-	41	82	ns	
Fall Time	t _f			-	22	44		
Gate Input Resistance	R _g	f = 1 MHz, open drain		0.3	0.86	1.7	Ω	
Drain-Source Body Diode Characteristi	cs							
Continuous Source-Drain Diode Current	١ _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	15		
Pulsed Diode Forward Current	I _{SM}			-	-	60	A	
Diode Forward Voltage	V _{SD}	T _J = 25 °	$T_{J} = 25 \text{ °C}, I_{S} = 8 \text{ A}, V_{GS} = 0 \text{ V}$		-	1.0	1.2	V
Reverse Recovery Time	t _{rr}				-	302	604	ns
Reverse Recovery Charge	Q _{rr}	T _J = 25 °C, I _F = I _S = 8 A, dI/dt = 100 A/µs, V _B = 25 V		-	4.0	8	μC	
Reverse Recovery Current	I _{RRM}		του <i>Ρ</i> νμS,	vR = 23 v	-	24	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} . b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

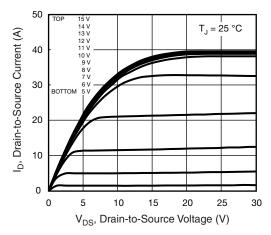


Fig. 1 - Typical Output Characteristics

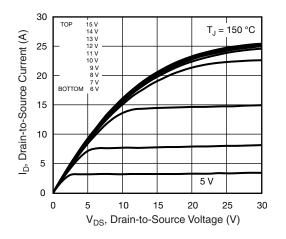


Fig. 2 - Typical Output Characteristics

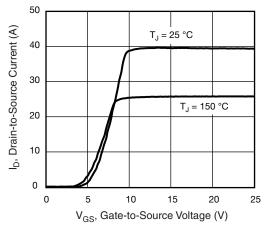


Fig. 3 - Typical Transfer Characteristics

S16-0799-Rev. H, 02-May-16

3 R_{DS(on)}, Drain-to-Source On Resistance (Normalized) 2.5 2 1.5 = 10 V /_{GS} 0.5 0 - 60 - 40 - 20 0 20 40 60 80 100 120 140 160 T_J, Junction Temperature (°C)

Fig. 4 - Normalized On-Resistance vs. Temperature

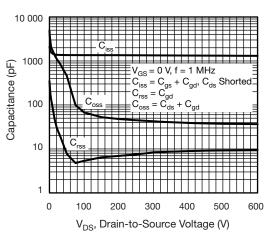


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

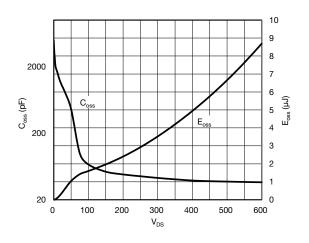


Fig. 6 - $C_{\rm oss}$ and $E_{\rm oss}$ vs. $V_{\rm DS}$

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SiHP15N60E

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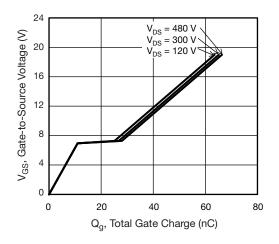


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

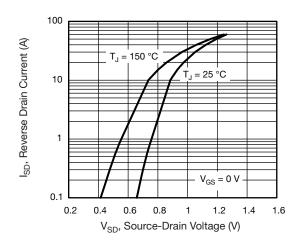


Fig. 8 - Typical Source-Drain Diode Forward Voltage

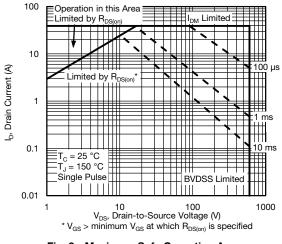


Fig. 9 - Maximum Safe Operating Area

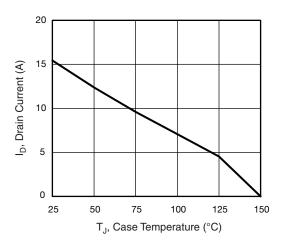


Fig. 10 - Maximum Drain Current vs. Case Temperature

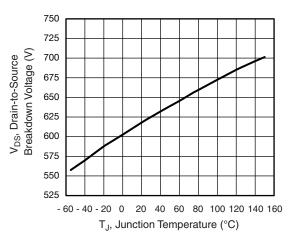
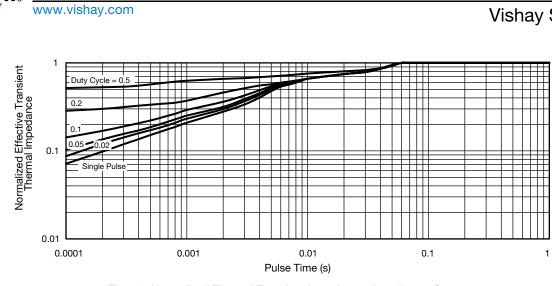


Fig. 11 - Temperature vs. Drain-to-Source Voltage

4

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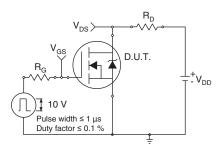


Fig. 13 - Switching Time Test Circuit

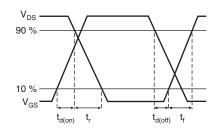


Fig. 14 - Switching Time Waveforms

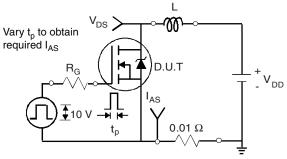


Fig. 15 - Unclamped Inductive Test Circuit

V_{DS} V_{DD} VDS I_{AS}

Fig. 16 - Unclamped Inductive Waveforms

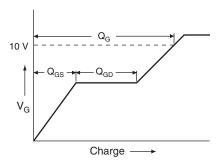


Fig. 17 - Basic Gate Charge Waveform

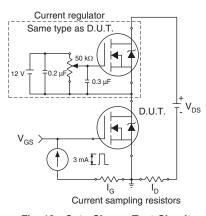


Fig. 18 - Gate Charge Test Circuit

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Peak Diode Recovery dV/dt Test Circuit

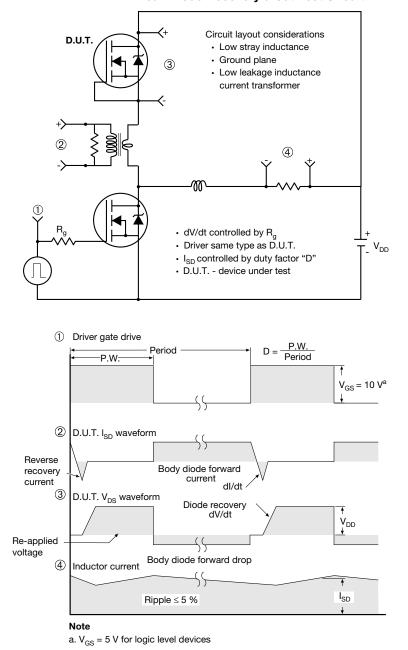


Fig. 19 - For N-Channel

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TO-220-1



DIM.	MILLIN	IETERS	INCHES		
DIN.	MIN.	MAX.	MIN.	MAX.	
А	4.24	4.65	0.167	0.183	
b	0.69	1.02	0.027	0.040	
b(1)	1.14	1.78	0.045	0.070	
С	0.36	0.61	0.014	0.024	
D	14.33	15.85	0.564	0.624	
E	9.96	10.52	0.392	0.414	
е	2.41	2.67	0.095	0.105	
e(1)	4.88	5.28	0.192	0.208	
F	1.14	1.40	0.045	0.055	
H(1)	6.10	6.71	0.240	0.264	
J(1)	2.41	2.92	0.095	0.115	
L	13.36	14.40	0.526	0.567	
L(1)	3.33	4.04	0.131	0.159	
ØР	3.53	3.94	0.139	0.155	
Q	2.54	3.00	0.100	0.118	
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031					

Note

- M^{\star} = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture						
ASE		Xi'an				
		IRF 9510 744K AB				

Revison: 14-Dec-15

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