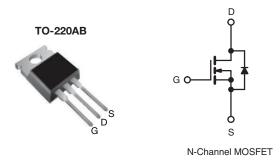


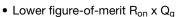
## **S Series Power MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> at T <sub>J</sub> max. (V)	650				
R <sub>DS(on)</sub> max. at 25 °C (Ω)	V <sub>GS</sub> = 10 V	0.190			
Q <sub>g</sub> max. (nC)	98				
Q <sub>gs</sub> (nC)	17				
Q <sub>gd</sub> (nC)	25				
Configuration	Single				



### **FEATURES**

- · Generation one
- High E<sub>AR</sub> capability



- 100 % avalanche tested
- Ultra low R<sub>on</sub>
- dV/dt ruggedness
- Ultra low gate charge (Qa)
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

### **APPLICATIONS**

- PFC power supply stages
- · Hard switching topologies
- · Solar inverters
- UPS
- Motor control
- Lighting
- Server telecom

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	SiHP22N60S-E3

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V <sub>DS</sub>	600		
Gate-Source Voltage			V <sub>GS</sub>	± 30	V	
Continuous Dunia Compant	V -140V	T <sub>C</sub> = 25 °C		22	А	
Continuous Drain Current	V <sub>GS</sub> at 10 V	$T_C = 25 ^{\circ}C$ $T_C = 100 ^{\circ}C$	I <sub>D</sub>	13		
Pulsed Drain Current <sup>a</sup>			I <sub>DM</sub>	65		
Linear Derating Factor		TO-220AB		2	W/°C	
Single Pulse Avalanche Energy b			E <sub>AS</sub>	690	1	
epetitive Avalanche Energy <sup>a</sup>			E <sub>AR</sub>	25	- mJ	
Maximum Power Dissipation		TO-220AB	P <sub>D</sub>	250	W	
Drain-Source Voltage Slope	T <sub>J</sub> = 125 °C		dV/dt	37	V/ns	
Reverse Diode dV/dt <sup>d</sup>			αν/αι	5.3	V/IIS	
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C	
Soldering Recommendations (Peak Temperature) c	for 10 s			300		

#### **Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b.  $V_{DD}$  = 50 V, starting  $T_J$  = 25 °C, L = 28.2 mH,  $R_g$  = 25  $\Omega$ ,  $I_{AS}$  = 7 A.
- c. 1.6 mm from case.
- d.  $I_{SD} \le I_D$ ,  $dI/dt = 100 \text{ A/}\mu\text{s}$ , starting  $T_J = 25 \,^{\circ}\text{C}$ .



# Vishay Siliconix

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	TO-220AB	R <sub>thJA</sub>	-	62	°C/W	
Maximum Junction-to-Case (Drain)	TO-220AB	$R_{thJC}$	-	0.5		

PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static		L					
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub>	600	_	_	V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Referenc	-	0.70	-	V/°C	
Gate-Source Threshold Voltage (N)	V <sub>GS(th)</sub>	V <sub>DS</sub> =	2.0	-	4.0	V	
		$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Gate-Source Leakage	I <sub>GSS</sub>	,	$V_{GS} = \pm 30 \text{ V}$		-	± 1	μΑ
7 0 1 1/1 5 1 0 1	I <sub>DSS</sub>	V <sub>DS</sub> =	600 V, V <sub>GS</sub> = 0 V	-	-	1	
Zero Gate Voltage Drain Current		V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150 °C		-	-	100	μA
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V		-	0.160	0.190	Ω
Forward Transconductance a	9fs	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 13 A		-	9.4	-	S
Dynamic							
Input Capacitance	C <sub>iss</sub>	$V_{GS} = 0 \text{ V},$ $V_{DS} = 25 \text{ V},$ f = 1.0  MHz		562	2810	5620	pF
Output Capacitance	C <sub>oss</sub>			296	1480	2960	
Reverse Transfer Capacitance	C <sub>rss</sub>			6.6	33	66	
Effective Output Capacitance (Time Related)	C <sub>oss eff.</sub> (TR) <sup>a</sup>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 0 V to 480 V	-	155	-	
Total Gate Charge	Q <sub>g</sub>			-	75	110	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	-	17	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>			-	25	-	1
Turn-On Delay Time	t <sub>d(on)</sub>			-	24	50	
Rise Time	t <sub>r</sub>	$V_{DD} = 380 \text{ V}, I_{D} = 22 \text{ A},$ $R_{g} = 9.1 \Omega, V_{GS} = 10 \text{ V}$		-	68	100	- ns
Turn-Off Delay Time	t <sub>d(off)</sub>			-	77	115	
Fall Time	t <sub>f</sub>			-	59	90	
Gate Input Resistance	R <sub>g</sub>	f = 1 MHz, open drain		0.13	0.65	1.3	Ω
Drain-Source Body Diode Characteristic	s						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode		-	-	22	А
Pulsed Diode Forward Current	I <sub>SM</sub>			-	-	88	
Diode Forward Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 22 A, V <sub>GS</sub> = 0 V		-	-	1.2	V
Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = I <sub>S</sub> , dI/dt = 100 A/µs, V <sub>R</sub> = 25 V		-	462	690	ns
Reverse Recovery Charge	$Q_{rr}$			-	8.3	16	μC
Reverse Recovery Current	I <sub>RRM</sub>			-	30	60	Α

## Note

a.  $C_{oss\ eff.}$  (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DS}$ .



### TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

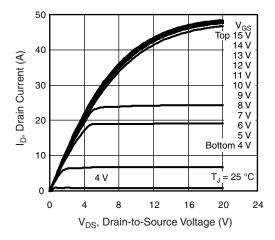


Fig. 1 - Typical Output Characteristics, T<sub>J</sub> = 25 °C

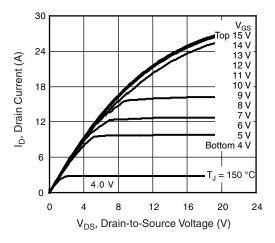


Fig. 2 - Typical Output Characteristics,  $T_J$  = 150 °C

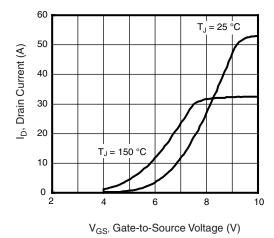


Fig. 3 - Typical Transfer Characteristics

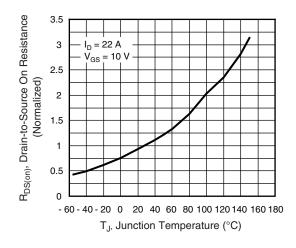


Fig. 4 - Normalized On-Resistance vs. Temperature

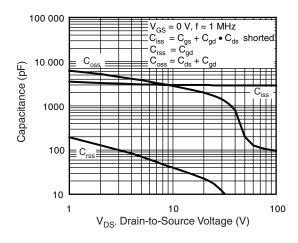


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

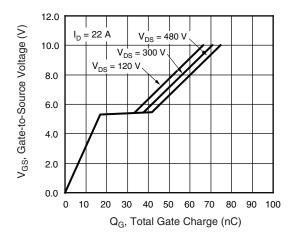


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



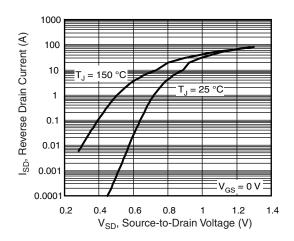


Fig. 7 - Typical Source-Drain Diode Forward Voltage

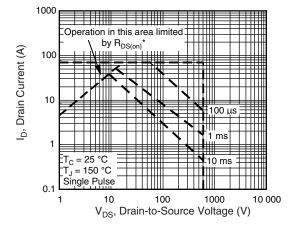


Fig. 8 - Maximum Safe Operating Area

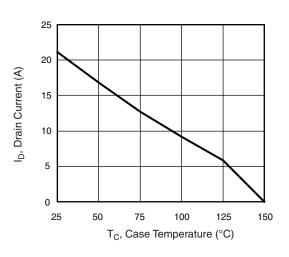


Fig. 9 - Maximum Drain Current vs. Case Temperature

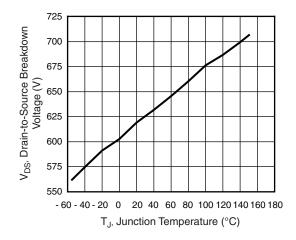


Fig. 10 - Drain-to-Source Breakdown Voltage

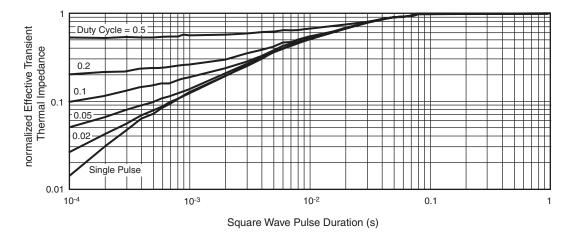


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case



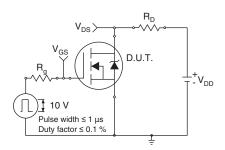


Fig. 12 - Switching Time Test Circuit

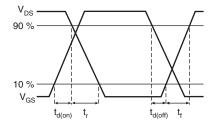


Fig. 13 - Switching Time Waveforms

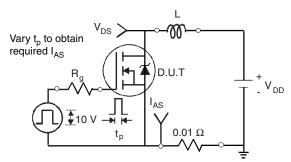


Fig. 14 - Unclamped Inductive Test Circuit

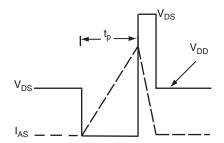


Fig. 15 - Unclamped Inductive Waveforms

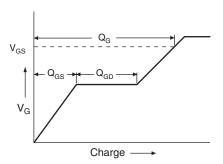


Fig. 16 - Basic Gate Charge Waveform

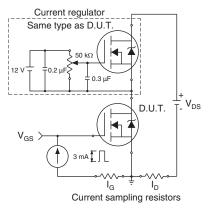
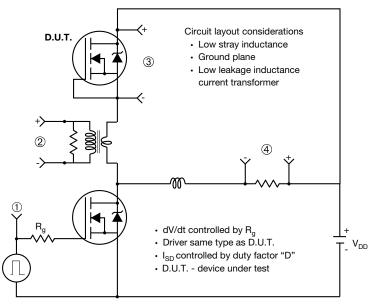


Fig. 17 - Gate Charge Test Circuit



### Peak Diode Recovery dV/dt Test Circuit



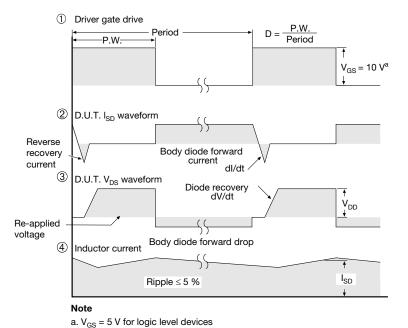


Fig. 18 - For N-Channel

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